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AN-9735

Design Guideline for LED Lamp Control Using Primary-Side Regulated Flyback Converter, FAN103 & FSEZ1317

Introduction

Many LED lamp systems use the flyback converter topology. In applications where precise output current regulation is required, current sensing in the secondary side is always necessary, which results in additional sensing loss. For power supply designers struggling to meet increasing regulatory pressures, the output current sensing is a daunting design challenge.

Primary-Side Regulation (PSR) for power supplies can be an optimal solution for compliance and cost in LED lamp systems. Primary-side regulation controls the output voltage and current precisely with information in the primary side of the LED lamp controller only. This removes the output current sensing loss and eliminates all secondary-feedback circuitry. This facilitates a higher efficiency power supply design without incurring tremendous costs. Fairchild Semiconductor PWM PSR controller FAN103 and Fairchild Power Switch (FPS™) (MOSFET + Controller, EZ-PSR) FSEZ1317 significantly simplify meeting tighter efficiency requirements with fewer external components.

This application note presents design considerations for LED lamp systems employing Fairchild Semiconductor components. It includes designing the transformer and output filter, selecting the components, and implementing constant-current control. The step-by-step procedure completes a power supply design. The design is verified through an experimental prototype converter using FSEZ1317. Figure 1 shows the typical application circuit for an LED lamp using FSEZ1317.

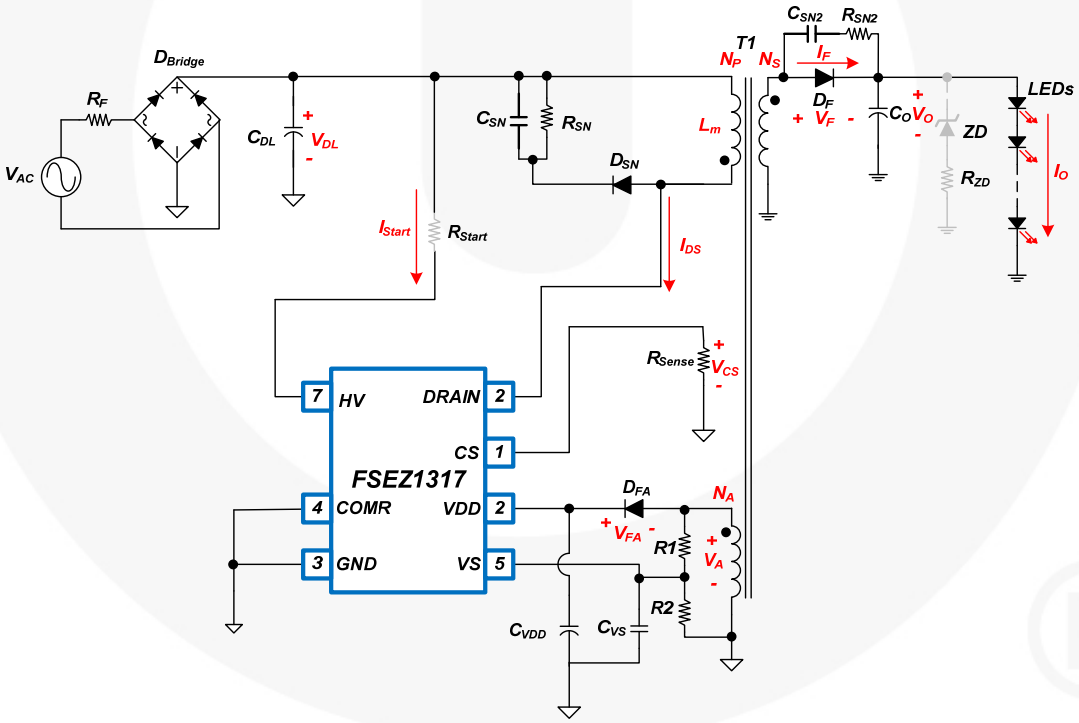

Figure 1. Typical Application Circuit

Operation Principle of Primary-Side Regulation

Figure 2 shows typical waveforms of a flyback converter. Generally, Discontinuous Conduction Mode (DCM) operation is preferred for primary-side regulation since it allows better output regulation. The key of primary-side regulation is how to obtain output voltage and current information without directly sensing them. Once these values are obtained, the control can be accomplished by the conventional feedback compensation method.

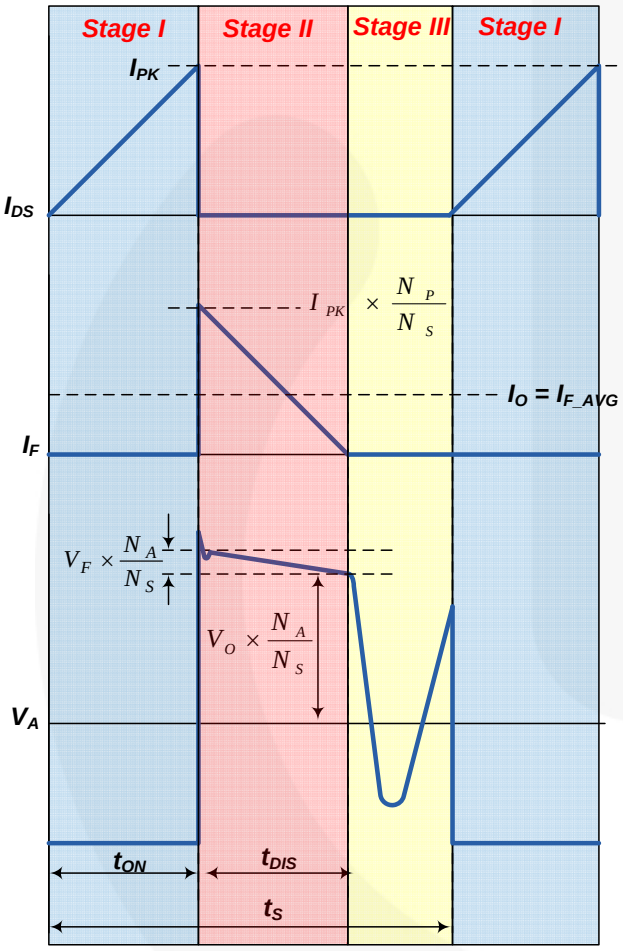

Figure 2. Key Waveforms of PSR Flyback Converter

The operation principles of DCM flyback converter are:

Stage I

During the MOSFET ON time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{DS}) increases linearly from zero to the peak value (I_{PK}). During this time, the energy is drawn from the input and stored in the inductor.

Stage II

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D_F) to be turned on. During the diode conduction time (t_{DIS}), the output voltage (V_O), together with diode forward-voltage drop (V_F), are applied across the secondary-side inductor and the diode current (I_F) decreases linearly from the peak value to zero. At the end of t_{DIS}, all the energy stored in the inductor has been delivered to the output.

Stage III

When the diode current reaches zero, the transformer auxiliary winding voltage (V_A) begins to oscillate by the resonance between the primary-side inductor (L_m) and the output capacitor of MOSFET.

Design Procedure

In this section, a design procedure is presented using the schematic in Figure 3 as a reference.

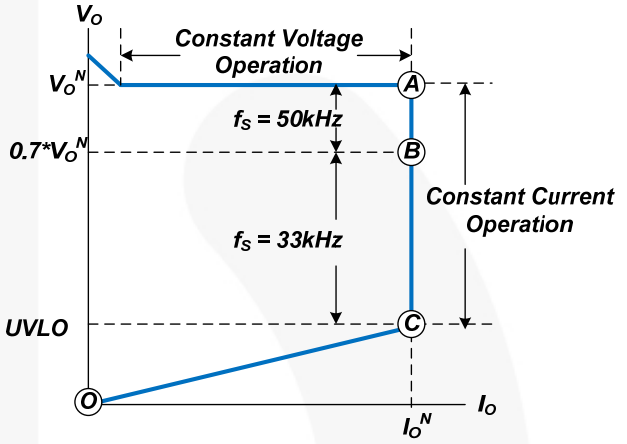

Figure 3. CV & CC Operation Area

[STEP-1] Estimate the Efficiencies

Figure 3 shows the CV & CC operation area. To optimize the power stage design, the efficiencies and input powers should be specified for operating point A (nominal output voltage and current), B (70% of nominal output voltage), and C (minimum output voltage).

1. Estimated overall efficiency (η) for operating points A, B, and C: The overall power conversion efficiency should be estimated to calculate the input power. If no reference data is available, set η = 0.7 ~ 0.75 for low-voltage output applications and η = 0.8 ~ 0.85 for high-voltage output applications.
2. Estimated primary-side efficiency (η_P) and secondary-side efficiency (η_S) for operating points A, B, and C. Figure 4 shows the definition of primary-side and secondary-side efficiencies, where the primary-side efficiency is for the power transfer from AC line input to the transformer primary side, while the secondary-side efficiency is for the power transfer from the transformer primary side to the power supply output.

The typical values for the primary-side and secondary-side efficiencies are given as:

$$\eta_P \cong \eta^{\frac{1}{3}}, \eta_S \cong \eta^{\frac{2}{3}}; V_O < 10V \quad (1)$$

$$\eta_P \cong \eta^{\frac{2}{3}}, \eta_S \cong \eta^{\frac{1}{3}}; V_O > 10V \quad (2)$$

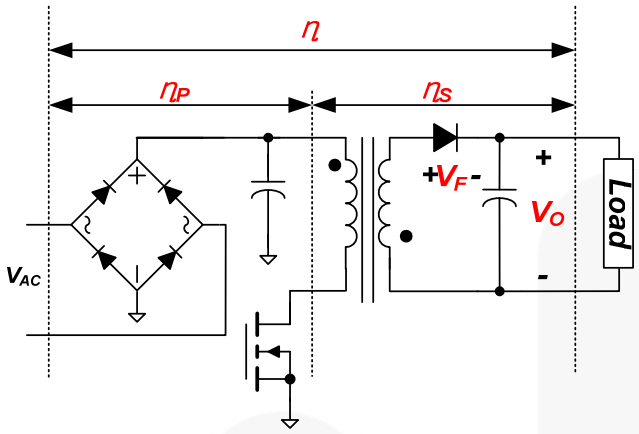

Figure 4. Primary- and Secondary-Side Efficiency

With the estimated overall efficiency, the input power at nominal output is given as:

$$P_{IN} = \frac{V_O^N \times I_O^N}{\eta} \quad (3)$$

where V_O^N and I_O^N are the nominal output voltage and current, respectively.

The input power of transformer at nominal output is given as:

$$P_{IN\_T} = \frac{V_O^N \times I_O^N}{\eta_S} \quad (4)$$

When the output voltage drops below 70% of its nominal value, the frequency is reduced to 33kHz to prevent CCM operation. Thus, the transformer should be designed for DCM both at 70% of nominal output voltage and minimum output voltage.

As output voltage reduces in CC Mode, the efficiency also drops. To optimize the transformer design, it is necessary to estimate the efficiencies properly at 70% of nominal output voltage and minimum output voltage conditions.

The overall efficiency at 70% of nominal output voltage (operating point B) can be approximated as:

$$\eta_{@B} \cong \eta \times \frac{0.7 \times V_O^N}{0.7 \times V_O^N + V_F} \times \frac{V_O^N + V_F}{V_O^N} \quad (5)$$

where V_F is diode forward-voltage drop.

The secondary-side efficiency at 70% of nominal output voltage (operating point B) can be approximated as:

$$\eta_{S@B} \cong \eta_S \times \frac{0.7 \times V_O^N}{0.7 \times V_O^N + V_F} \times \frac{V_O^N + V_F}{V_O^N} \quad (6)$$

Then, the power supply input power and transformer input power at 70% nominal output voltage (operating point B) are given as:

$$P_{IN@B} = \frac{0.7 \times V_O^N \times I_O^N}{\eta_{@B}} \quad (7)$$

$$P_{IN\_T@B} = \frac{0.7 \times V_O^N \times I_O^N}{\eta_{S@B}} \quad (8)$$

The overall efficiency at the minimum output voltage (operating point C) can be approximated as:

$$\eta_{@C} \cong \eta \times \frac{V_O^{\min}}{V_O^{\min} + V_F} \times \frac{V_O^N + V_F}{V_O^N} \quad (9)$$

where, Vo^{min} is the minimum output voltage.

The secondary-side efficiency at minimum output voltage (operating point C) can be approximated as:

$$\eta_{@C} \cong \eta_S \times \frac{V_O^{\min}}{V_O^{\min} + V_F} \times \frac{V_O^N + V_F}{V_O^N} \quad (10)$$

Then, the power supply input power and transformer input power at the minimum output voltage (operating point C) are given as:

$$P_{IN@C} = \frac{V_O^{\min} \times I_O^N}{\eta_{@C}} \quad (11)$$

$$P_{IN\_T@B} = \frac{V_O^{\min} \times I_O^N}{\eta_{S@C}} \quad (12)$$

[STEP-2] Determine the DC Link Capacitor (C_{DL}) and the DC Link Voltage Range

It is typical to select the DC link capacitor as 2-3μF per watt of input power for universal input range (90 ~ $265V_{RMS}$) and 1μF per watt of input power for European input range (195 ~ $265V_{RMS}$). With the DC link capacitor chosen, the minimum DC link voltage is obtained as:

$$V_{DL}^{\min} = \sqrt{2 \times (V_{LINE}^{\min})^2 - \frac{P_{IN}(1 - D_{ch})}{C_{DL} \times f_L}} \quad (13)$$

where V_{LINE}^{min} is the minimum line voltage, C_{DL} is the DC link capacitor, f_L is the line frequency, and D_{ch} is the DC link capacitor charging duty ratio defined as shown in Figure 5, which is typically about 0.2.

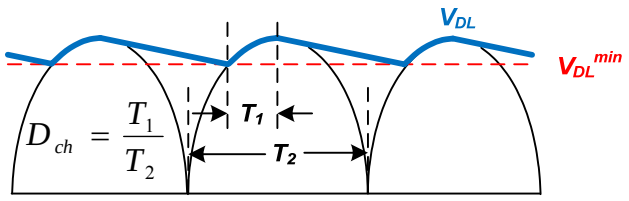

Figure 5. DC Link Voltage Waveforms

The maximum DC link voltage is given as:

$$V_{DL}^{max} = \sqrt{2} \times V_{LINE}^{max} \quad (14)$$

where V_{LINE}^{max} is the maximum line voltage.

The minimum input DC link voltage at 70% nominal output voltage are given as:

$$V_{DL@B}^{min} = \sqrt{2 \times (V_{LINE}^{min})^2 - \frac{P_{IN@B}(1-D_{ch})}{C_{DL} \times f_L}} \quad (15)$$

The minimum input DC link voltage at minimum output voltage are given as:

$$V_{DL@C}^{min} = \sqrt{2 \times (V_{LINE}^{min})^2 - \frac{P_{IN@C}(1-D_{ch})}{C_{DL} \times f_L}} \quad (16)$$

[STEP-3] Determine the Transformer Turns Ratio

Figure 6 shows the MOSFET drain-to-source voltage waveforms. When the MOSFET is turned off, the sum of the input voltage (V_{DL}) and the output voltage reflected to the primary is imposed across the MOSFET as:

$$V_{DS}^{nom} = V_{DL}^{max} + V_{RO} \quad (17)$$

where V_{RO} is reflected output voltage defined as:

$$V_{RO} = \frac{N_S}{N_P} \times (V_O + V_F) \quad (18)$$

where V_F is the diode forward voltage drop and N_P and N_S are number of turns for the primary side and secondary side, respectively.

When the MOSFET is turned on, the output voltage, together with input voltage reflected to the secondary, are imposed across the diode as:

$$V_F = V_O + \frac{N_S}{N_P} \times V_{DL}^{max} \quad (19)$$

As observed in Equations (5) and (6), increasing the transformer turns ratio (N_P/N_S) results in increased voltage of MOSFET, while it leads to reduced voltage stress of rectifier diode. Therefore, the transformer turns ratio (N_P/N_S) should be determined by the compromise between MOSFET and diode voltage stresses. When determining the transformer turns ratio, the voltage overshoot (V_{OS}) on drain voltage should be also considered. The maximum voltage stress of MOSFET is given as:

$$V_{DS}^{max} = V_{DL}^{max} + V_{RO} + V_{OS} \quad (20)$$

For reasonable snubber design, voltage overshoot (V_{OS}) is typically 1~1.5 times the reflected output voltage. It is also typical to have a margin of 15~20% of breakdown voltage for maximum MOSFET voltage stress.

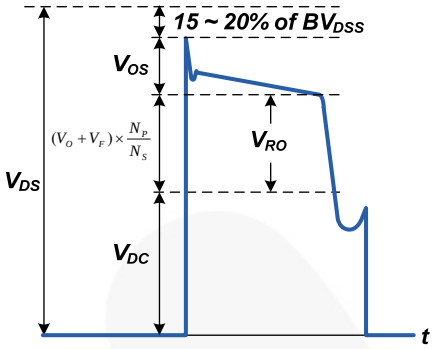

Figure 6. Voltage Stress of MOSFET

The transformer turns ratio between the auxiliary winding and secondary winding (N_A/N_S) should be determined by considering the permissible IC supply voltage (V_{DD}) range and minimum output voltage in constant current. When the LED operates in constant current, V_{DD} is changed, together with the output voltage, as seen Figure 7. The overshoot of auxiliary winding voltage caused by the leakage inductance also affects the V_{DD}. V_{DD} voltage at light-load condition, where the overshoot of auxiliary winding voltage is negligible, is given as:

$$VDD^{min1} = \frac{N_A}{N_S} \times (V_O + V_F) - V_{FA} \quad (21)$$

The actual V_{DD} voltage at heavy load is higher than Equation (21) due to the overshoot by the leakage inductance, which is proportional to the voltage overshoot of MOSFET drain-to-source voltage shown in Figure 7. Considering the effect of voltage overshoot, the V_{DD} voltages for nominal output voltage and minimum output voltage are given as:

$$VDD^{max} \cong \frac{N_A}{N_S} \times \left(V_O + V_F + \frac{N_S}{N_P} \times V_{OS} \right) - V_{FA} \quad (22)$$

$$VDD^{min2} \cong \frac{N_A}{N_S} \times \left(V_O^{min} + V_F + \frac{N_S}{N_P} \times V_{OS} \right) - V_{FA} \quad (23)$$

where V_{FA} is the diode forward-voltage drop of auxiliary winding diode.

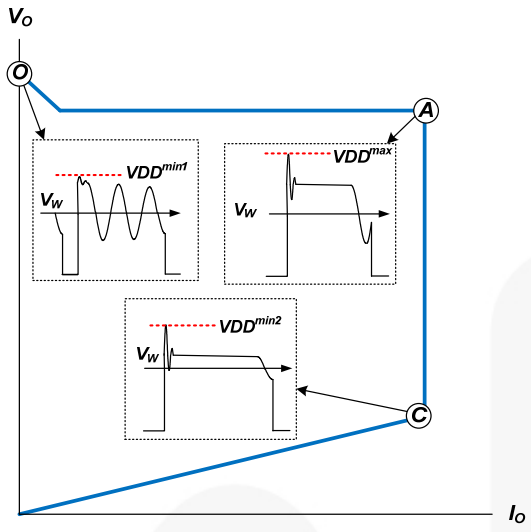

Figure 7. V_{DD} and Winding Voltage

[STEP-4] Design the Transformer

Figure 8 shows the definition of MOSFET conduction time (t_{ON}), diode conduction time (t_{DIS}), and non-conduction time (t_{OFF}). The sum of MOSFET conduction time and diode conduction time at 70% of nominal output voltage is obtained as:

$$t_{ON@B} + t_{DIS@B} = t_{ON@B}\left(1 + \frac{N_S}{N_P} \times \frac{V_{DL@B}^{\min}}{0.7 \times V_O + V_F}\right) \quad (24)$$

The first step in transformer design is to determine how much non-conduction time (t_{OFF}) is allowed in DCM operation.

Once the t_{OFF} is determined, by considering the frequency variation caused by frequency hopping and its own tolerance, the MOSFET conduction time is obtained as:

$$t_{ON@B} = \frac{\frac{1}{f_S} - t_{OFF@B}}{1 + \frac{N_S}{N_P} \times \frac{V_{DL@B}^{\min}}{0.7 \times V_O + V_F}} \quad (25)$$

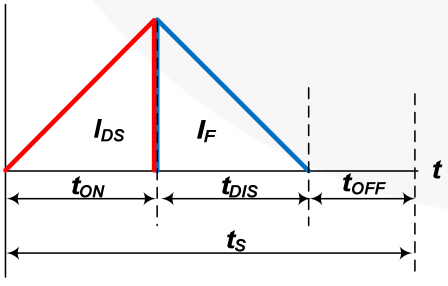

Figure 8. Definition of t_{ON}, t_{DIS}, and t_{OFF}

Transformer primary-side inductance can be calculated as:

$$L_m = \frac{(V_{DL@B}^{\min} \times t_{ON@B})^2 \times f_S}{2 \times P_{IN\_T@B}} \quad (26)$$

The maximum peak-drain current can be obtained at the nominal output condition as:

$$I_{DS}^{PK} = \sqrt{\frac{2 \times P_{IN\_T}}{L_m \times f_S}} \quad (27)$$

The MOSFET conduction time at the nominal output condition is obtained as:

$$t_{ON} = I_{DS}^{PK} \times \frac{L_m}{V_{DL}^{\min}} \quad (28)$$

The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P^{\min} = \frac{L_m \times I_{DS}^{PK}}{B_{sat} \times A_e} \quad (29)$$

where A_e is the cross-sectional area of the core in m^2 and B_{sat} is the saturation flux density in Tesla.

Figure 9 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{sat}) decreases as the temperature rises, the high-temperature characteristics should be considered when it comes to charger in enclosed case. If there is no reference data, use B_{sat} =0.25~0.3T.

Once the turns ratio is obtained, determine the proper integer for N_S so that the resulting N_P is larger than $N_P^{\min}$ obtained from Equation (29).

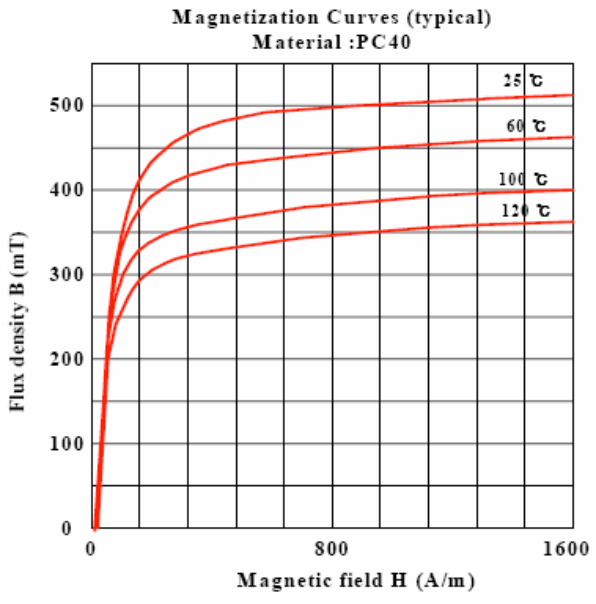

Figure 9. Typical B-H Curves of Ferrite Core (TDK/PC40)

DCM operation at minimum output voltage should be also checked. The MOSFET conduction time at minimum output voltage is given as:

$$t_{ON@C} = \frac{1}{V_{DL@C}^{\min}} \times \sqrt{\frac{2 \times P_{IN\_T@C} \times L_m}{f_{SR}}} \quad (30)$$

where f_{SR} is the reduced switching frequency to prevent CCM operation.

Then, the non-conduction time at minimum output voltage is given as:

$$t_{OFF@C} = \frac{1}{f_{SR}} - t_{ON@C}\left(1 + \frac{N_P}{N_S} \times \frac{V_{DL@C}^{\min}}{V_O^{\min} + V_F}\right) \quad (31)$$

The non-conduction time should be larger than 3μs (10% of the switching period), considering the tolerance of the switching frequency.

[STEP-5] Calculate the Voltage and Current of the Switching Devices

Primary-Side MOSFET

The voltage stress of the MOSFET was discussed when determining the turns ratio in STEP-3. Assuming that drain-voltage overshoot is the same as the reflected output voltage, maximum drain voltage is given as:

$$V_{DS}^{\max} = V_{DL}^{\max} + V_{RO} + V_{OS} \quad (32)$$

The RMS current though the MOSFET is given as:

$$I_{DS}^{rms} = I_{DS}^{PK} \times \sqrt{\frac{t_{ON} \times f_S}{3}} \quad (33)$$

Secondary-Side diode

The maximum reverse voltage and the RMS current of the rectifier diode are obtained, respectively, as:

$$V_F = V_O^N + \frac{N_S}{N_P} \times V_{DL}^{\max} \quad (34)$$

$$I_F^{rms} = I_{DS}^{rms} \times \sqrt{\frac{V_{DL}^{\min}}{V_{RO}}} \times \frac{N_P}{N_S} \quad (35)$$

[STEP-6] Output Voltage and Current Setting

The nominal output current is determined by the sensing resistor value and transformer turns ratio as:

$$R_{Sense} = \frac{N_P}{N_S \times I_O^N \times 8.5} \quad (37)$$

The voltage divider R_1 and R_2 should be determined such that V_S is 2.5V at the end of diode current conduction time, as shown in Figure 8.

$$\frac{R_1}{R_2} = \frac{V_O^N}{V_{ref}} \times \frac{N_A}{N_S} - 1 \quad (38)$$

Select 1% tolerance resistor for better output regulation.

It is recommended to place a bypass capacitor of 22~68pF closely between the VS pin and the GND pin to bypass the switching noise and keep the accuracy of the sampled voltage for CV regulation. The value of the capacitor affects the load regulation and constant-current regulation. Figure 10 illustrates the measured waveform on the VS pin with a different VS capacitor. If a higher value VS capacitor is used, the charging time becomes longer and the sampled voltage is higher than the actual value.

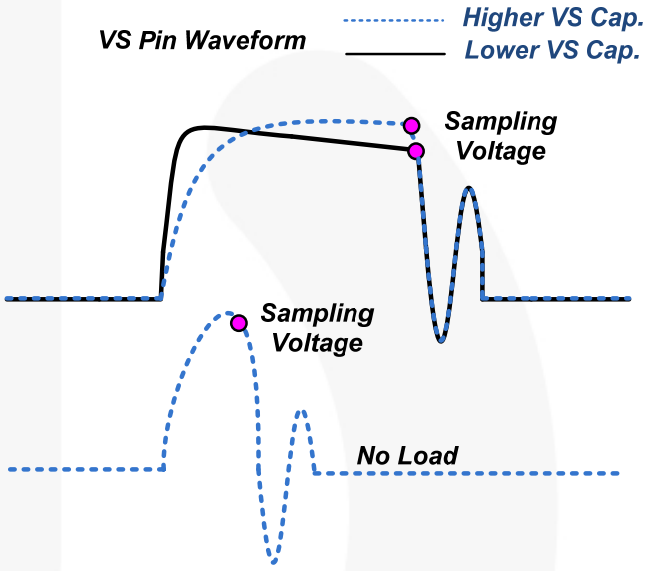

Figure 10. Effect on Sampling Voltage with Different VS Capacitor

[STEP-7] Determine the Output Filter Stage

The peak to peak ripple of capacitor current is given as:

$$\Delta I_{CO} = \frac{N_P}{N_S} \times I_{DS}^{PK} \quad (39)$$

The voltage ripple on the output is given by:

$$\Delta V_O = \frac{\Delta I_{CO} \times t_{DIS}}{2 \times C_O} \times \left(\frac{\Delta I_{CO} - I_O^N}{\Delta I_{CO}}\right)^2 + \Delta I_{CO} \times R_C \quad (40)$$

Sometimes it is impossible to meet the ripple specification with a single output capacitor (C_O) due to the high ESR (R_C) of the electrolytic capacitor. Additional LC filter stages (post filter) can be used. When using the post filters, do not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10 ~ 1/5 of the switching frequency.

[STEP-8] Cable Voltage-Drop Compensation

When the load is far away from output, the output voltage needs to compensate for voltage drop. FAN103 and FSEZ1317 have cable voltage-drop compensation that can be programmed by a resistor on the COMR pin, as shown in Table 1. If the COMR is not used, such as for LED bulb, it needs be to connected to GND.

Table 1. Cable Compensation

% of Voltage Drop Compensation	COMR Resistor
7%	Open
6%	900kΩ
5%	380kΩ
4%	230kΩ
3%	180kΩ
2%	145kΩ
1%	100kΩ
0%	45kΩ

[STEP-9] Design RCD Snubber in Primary Side

When the power MOSFET is turned off, there is a high-voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and, eventually, failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber circuit and MOSFET drain-voltage waveform are shown in Figure 6. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode (D_{SN}) once the MOSFET drain voltage exceeds the voltage of cathode of D_{SN}. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The snubber capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable for these reasons.

The snubber capacitor voltage at full-load condition (V_{SN}) is given as:

$$V_{SN} = V_{RO} + V_{OS} \tag{41}$$

The power dissipated in the snubber network is obtained as:

$$P_{SN} = \frac{V_{SN}^{\ 2}}{R_{SN}} = \frac{1}{2} \times L_{lk} \times (I_{DS}^{\ PK})^2 \times \frac{V_{SN}}{V_{SN} - V_{OS}} \times f_S \tag{42}$$

where I_{DS}^{PK} is peak-drain current at full load, L_{lk} is the leakage inductance, V_{SN} is the snubber capacitor voltage at full load, and R_{SN} is the snubber resistor.

The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted. Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \times R_{SN} \times f_S} \tag{43}$$

In general, 5~20% ripple of the selected capacitor voltage is reasonable.

In the snubber design in this section, neither the lossy discharge of the inductor nor stray capacitance is considered. In the actual converter, the loss in the snubber network is less than the designed value due to this effect.

Design Example Using FSFR1317

Table 2. Cable Compensation

Application	Device	Input	Output
LED Bulb	FSEZ1317MY	$90V_{AC}$ ~ $265V_{AC}$ (50 ~ 60Hz)	4.2W (12V/0.35A)

Description		Symbol	Value	Unit
System Specifications				
Input	Minimum Line Input Voltage	V_{LINE}^{min}	90	V_{AC}
	Maximum Line Input Voltage	V_{LINE}^{max}	265	V_{AC}
	Line Frequency	f_L	60	Hz
	Setting Output Voltage	V_O	12	V
	Output Voltage at Point B	$V_{O@B}$	8.40	V
	Minimum Output Voltage	V_O^{min}	3	V
	Normal Output Current	I_O^N	0.35	A
	Output Diode Voltage Drop	V_F	0.55	V
	Normal Switching Frequency	f_S	50	kHz
	Switching Frequency between Point B and Point C	f_{SR}	33	kHz
Estimated Efficiency				
Input	Efficiency	η	0.75	W
Output	Secondary-Side Efficiency	η_S	0.91	
	Input Power	P_{IN}	5.60	
	Input Power of Transformer	P_{IN_T}	4.62	
	Efficiency at Point B	$\eta_{@B}$	0.74	
	Secondary-Side Efficiency at Point B	$\eta_{S@B}$	0.89	
	Input Power at Point B	$P_{IN@B}$	3.99	
	Input Power of Transformer at Point B	$P_{IN\_T@B}$	3.30	
	Efficiency at Point C	$\eta_{@C}$	0.66	
	Secondary-Side Efficiency at Point C	$\eta_{S@C}$	0.80	
	Input Power at Point C	$P_{IN@C}$	1.58	
	Input Power of Transformer at Point C	$P_{IN\_T@C}$	1.31	
Determine DC Link Capacitor & DC Link Voltage Range				
Input	DC Link Capacitor	C_{DL}	9.40	µF
Output	Minimum DC Link Voltage	V_{DL}^{min}	90.87	V
	Maximum DC Link Voltage	V_{DL}^{max}	374.77	
	Minimum DC Link Voltage at Point B	$V_{DL@B}^{min}$	102.64	
	Minimum DC Link Voltage at Point C	$V_{DL@C}^{min}$	118.12	
Determine the Transformer Turn Ratio				
Input	Rectifier Output Voltage	V_{RO}	70.0	V
	Maximum V_{DD}	VDD^{max}	24.0	
	Minimum V_{DD}	VDD^{min}	5.5	
	V_{DD} Ripple in Burst Mode	VDD_{ripple}	2.5	
	V_{DD} Diode Drop Voltage	V_{FA}	0.70	
	N_A/N_S Ratio	N_A/N_s	0.80	
Output	MOSFET Overshoot Voltage	V_{OS}	70.00	
	N_P/N_S Ratio	N_P/N_S	5.58	
	Minimum N_A/N_S Ratio 1	N_A/N_S^{min1}	0.69	
	Minimum N_A/N_S Ratio 2	N_A/N_S^{min2}	0.39	
	Determine Minimum N_A/N_S Ratio	N_A/N_s^{min}	0.69	
	Determine Maximum N_A/N_S Ratio	N_A/N_s^{max}	0.98	

Description		Symbol	Value	Unit
Transformer Design				
Input	Non Conduction Time at Point B	$t_{OFF@B}$	5.00	µs
	Transformer Core Cross-Sectional Area	A_e	20.10	mm^2
	Maximum Flux Density	B_{sat}	0.30	T
	Determine Secondary-Side Turns	N_S	20	Turns
Output	MOSFET Conduction Time at Point B	$t_{ON@B}$	4.91	µs
	Transformer Primary-Side Inductance	L_m	1.92	mH
	Peak Drain Current	I_{DS}^{PK}	0.31	A
	Minimum Primary-Side Turns	N_p^{min}	98.93	Turns
	Determine Primary-Side Turns	N_p	112	Turns
	Determine Auxillary Winding Turns	N_A	16	Turns
	Final N_P/N_S Ratio	N_P/N_S	5.60	
	Final N_A/N_S Ratio	N_A/N_s	0.80	
	MOSFET Conduction Time	t_{ON}	6.57	µs
	Inductor Discharge Time	t_{DIS}	8.49	µs
	Non-Conduction Time	t_{OFF}	4.95	µs
	MOSFET Conduction Time at Point C	$t_{ON@C}$	3.31	µs
	Inductor Discharge Time at Point C	$t_{DIS@C}$	19.65	µs
	Non Conduction Time at Point C	$t_{OFF@C}$	7.35	µs
Selection Switching Device				
Output	MOSFET Maximum Drain-Source Voltage	V_{DS}^{max}	514.77	V
	MOSFET RMS Current	I_{DS}^{rms}	0.10	A
	Maximum Diode Voltage	V_F	78.92	V
	Maximum Diode RMS Current	I_F	0.65	A
Setting Output Voltage & Current				
Input	VS Low-Side Resistor	R2	33.00	KΩ
	Current-Sensing Resistor 1	R_{sense1}	3.9	Ω
	Current-Sensing Resistor 2	R_{sense2}	3.6	Ω
	Real VS High-Side Resistor	$R1\_{real}$	100	KΩ
Output	VS High-Side Resistor	R1	93.72	KΩ
	Current-Sensing Resistor	R_{sense}	1.92	Ω
	Real Output Voltage Setting	VO	11.34	V
	Real Current-Sensing Resistor	RS	1.872	Ω
	Real Output Current Setting	IO	0.36	A
Design RCD Snubber Stage				
Input	Leakage Inductance of Primary Side	L_{lk}	50	µH
	Rectifier Output Voltage	V_{RO}	70	V
	MOSFET Overshoot Voltage	V_{OS}	70	V
Output	Snubber Voltage	V_{SN}	141	V
	Snubber Capacitor Ripple Voltage	ΔV_{SN}	28.11	V
	Resonance Time	t_S	0.22	µs
	Power Dissipation in Snubber Resistor	P_{SN}	0.24	W
	Snubber Resistor	R_{SN}	82.26	KΩ
	Snubber Capacitor	C_{SN}	1.22	nF

Design Summary using FSFR1317

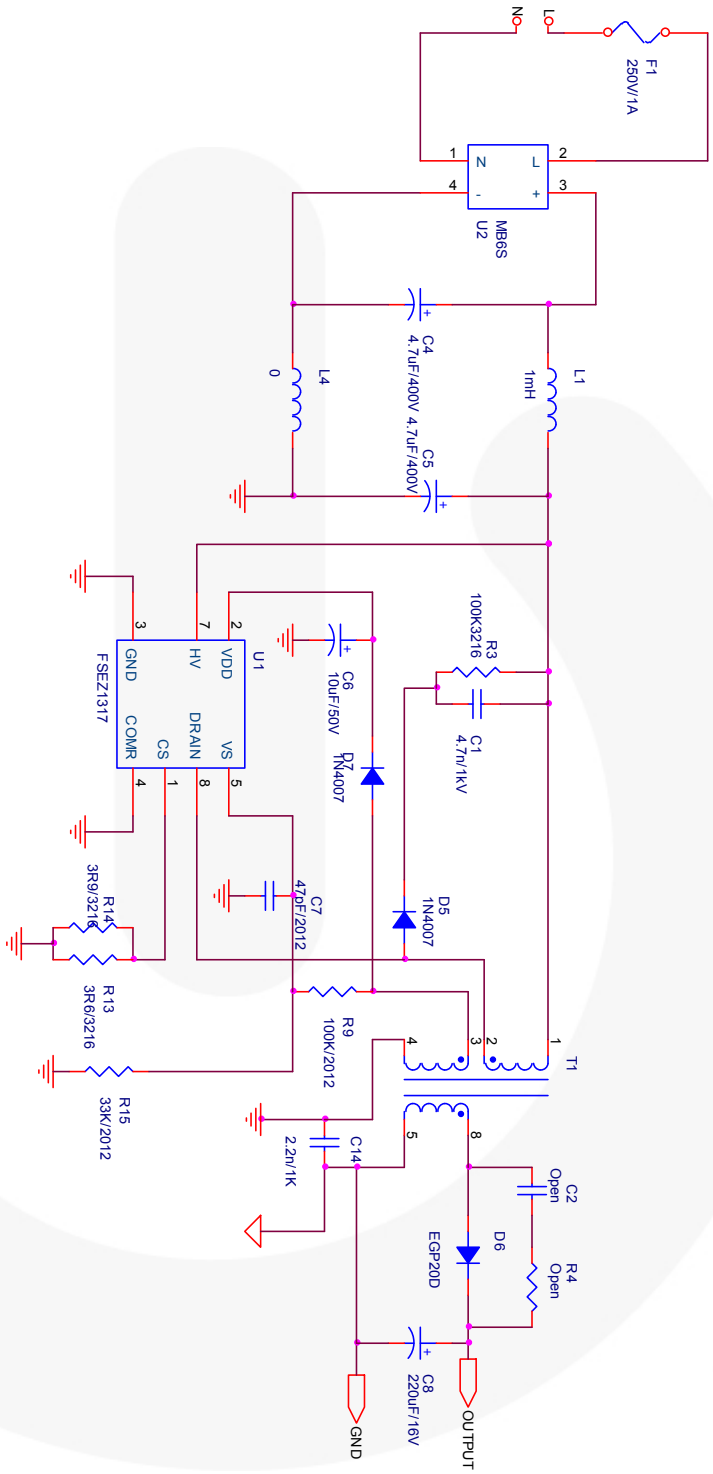

Figure 11. Schematic for LED Bulb

Transformer for LED Bulb

Core : EE-16 (Material: PC-40)
Bobbin : 8-Pin

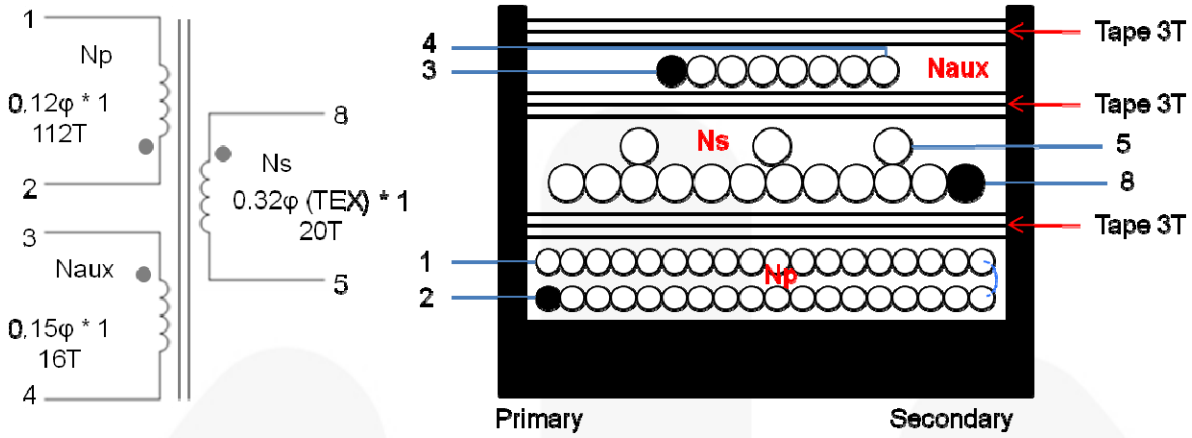

Figure 12.Transformer Specifications and Construction

Table 3. Winding Specifications

No.	Winding	Pin (S → F)	Wire	Turns	Winding Method
1	Np	2 → 1	0.12φ×1	112 Ts	Solenoid winding
2	Insulation: Polyester Tape t = 0.025mm, 3 Layer				
3	Ns	8 → 5	0.32φ(TEX)×1	20 Ts	Solenoid winding
4	Insulation: Polyester Tape t = 0.025mm, 3 Layer				
5	Naux	3 → 4	0.15φ×1	16 Ts	Solenoid winding
6	Insulation: Polyester Tape t = 0.025mm, 3 Layer				

Table 4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1 – 2	1.90mH ±10%	1kHz, 1V

Related Datasheets

FSEZ1317 — Primary- Side Regulation PWM with Power MOSFET Integrated Datasheet

FAN103 — Primary-Side Regulation PWM Controller Datasheet

AN-8033 — Design and Application of Primary-Side Regulation (PSR) PWM Controller