ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

AN-9080

Motion SPM® 5 Series Version 2 User's Guide

Table of Contents

1. Introduction

1.1. About this Application Note

This application note is about Motion SPM® 5 Series Version 2 products. It should be used in conjunction with the datasheet, reference designs, and related application notes listed in . This note focuses on the difference between Version 2 and the previous versions of SPM parts, with emphasis on new IC functions

1.2. Design Concept

The key design objective of the SPM 5 series is to provide a compact and reliable inverter solution for small power motor drive applications. Ongoing efforts have improved the performance, quality, and power rating of SPM 5 series products and the Version 2 products are the latest results of these enhancements. The new features include temperature-sensing capability, built-in bootstrap diodes, and upgraded ruggedness. Two higher power rating devices based on super-junction MOSFET technology are added to cover higher power rating applications without significantly increasing cost.

The MOSFETs in SPM 5 series are specially processed to reduce the amount of body-diode reverse recovery charge to minimize the switching loss and enable fast switching operations. Softness of the reverse-recovery characteristics is managed through advanced MOSFET design with optimized gate resistor selections to contain Electromagnetic Interference (EMI) noise within a reasonable range.

SPM 5 series has six fast-recovery MOSFETs (FRFET®) and three high-voltage half-bridge gate drive ICs. These MOSFETs and HVICs are not available as discrete parts. An FRFET-based power module has much better ruggedness and a larger safe operation area (SOA) than IGBT-based module or Silicon-On-Insulator modules.

The FRFET-based power module has a big advantage in light-load efficiency over IGBT-based because the voltage drop across the transistor decreases linearly as current decrease, whereas IGBT V_{ce} saturation voltage stays at the threshold level. Some applications require continuous operation at light load except short transients and improving the efficiency in the light-load condition is the key to saving energy. Refrigerators, water circulation pumps, and some fans are good examples.

The temperature-sensing function of version 2 products is implemented in the HVIC to enhance system reliability. An analog voltage proportional to the temperature of the HVIC is provided for monitoring the module temperature and necessary protections against over-temperature situations.

Three internal bootstrap diodes with resistive characteristics reduce the number of external components and make the PCB design more compact, beneficial when designing an inverter built inside the motor.

1.3. Features

The detailed features and integrated functions are:

- Variety of products with different voltage and power ratings: 250/500/600 V 3-phase FRFET inverter ,including HVICs
- Three divided negative DC-link terminals for leg current sensing
- HVIC for gate driving of FRFET, under-voltage protection, and thermal sensing functions
- 3.3/5 V Schmitt trigger input with active HIGH logic
- Built-in bootstrap diodes
- Single-grounded power supply and optocoupler-less interface due to built-in HVIC
- Minimized standby current of HVIC for energy regulation
- Packages; DIP, SMD, Double-DIP, Zigzag-DIP
- Isolation voltage rating of 1500 V_{RMS} for 1 minute
- Moisture Sensitive Level 3 (MSL3) for SMD package

2. Product Selections

2.1. Ordering Information

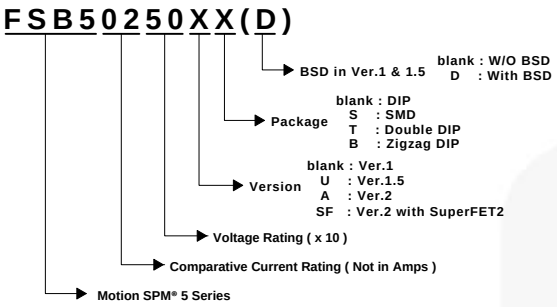


Figure 1. Ordering Information

2.2. Product Line-up

Table 1 shows the basic line up without package variations.

Table 1. Product Offerings

Part Number	BV_{DSS} [V]	I_{DRMS} [A_{rms}]	I_{D25} [A]	$R_{DS(on)}$ (Typ.) [Ω]	$R_{DS(on)}$ (Max.) [Ω]	$R_{\theta JC}$ (Max.) [°C/W]
FSB50325A	250	0.9	1.7	1.1	1.7	10.2
FSB50825A	250	1.9	3.6	0.33	0.45	8.8
FSB50250A	500	0.6	1.2	2.5	3.8	9.3
FSB50450A	500	0.8	1.5	1.9	2.4	8.9
FSB50550A	500	1.1	2.0	1.0	1.4	8.6
FSB50260SF	600	0.92	1.7	2.0	2.4	9.8
FSB50660SF	600	1.6	3.1	0.60	0.70	8.8
FSB50760SF	600	1.9	3.6	0.46	0.53	8.6

Fairchild's online loss and temperature simulation tool, Motion Control Design Tool, available at: (*http://www.fairchildsemi.com/support/design-tools/motion-control-design-tool/*), is recommended to select the best SPM product by power rating for the desired application.

2.3. SPM 5 Version Comparison

As can be seen from Table 2, version s "V2" products have at least the same or lower R_{DS_max} compared with the predecessors; lower R_{DS_max} values than older version are in red. Old version products were not released at the same time, and, therefore, there are differences even within the same version products. V2 products are being released at the same time with consistent features. V2 products are more rugged than previous versions in many respects.

- VCC-COM and VB-VS surge noise immunity level increased about 50%. In other words, when a single-surge pulse comes in between these pins, V2 products endure 50% higher surge voltage without malfunction.
- Destruction level against surge pulses consecutively coming in between V_b and V_S improved significantly.
- Problems associated with intermittent latch-on/off due to manufacturing issue have been resolved. Previous version products have been updated accordingly.

V_{CC} quiescent current increased due to the TSU function. It does not have much effect on selecting the bootstrap capacitor value, but stand-by power is increased by about 2.1 mW. There is no change in quiescent current of V_{BS}.

Table 2. SPM 5 Version Comparison

		V1	V1.5	V2
Silicon Technology		**CFET**	**UniFET™**	**UniFET™ / SuperFET® 2**
Line-Up & $R_{DS(on)max}$	60 V	FSB52006: 80 mΩ Max.		
	250 V	FSB50325: 1.8 Ω Max.		FSB50325A: 1.7 Ω Max.
			FSB50825U: 0.45 Ω Max.	FSB50825A: 0.45 Ω Max.
	500 V	FSB50250: 4.0 Ω Max.	FSB50250U: 4.2 Ω Max.	FSB50250A: 3.8 Ω Max.
		FSB50450: 2.4 Ω Max.	FSB50450U: 2.4 Ω Max.	FSB50450A: 2.4 Ω Max.
		FSB50550: 1.7 Ω Max.	FSB50550U: 1.4 Ω Max.	FSB50550A: 1.4 Ω Max.
	600 V			FSB50260SF: 2.4 Ω Max
				FSB50660SF: 0.7 Ω Max.
				FSB50760SF: 0.53 Ω Max.
Package		Transfer molded package without substrate		
V_S-Output		Out-Bonding, except 50325TD	Out-Bonding except TD-Version	Inner Bonding
Bootstrap Diode		Not included except 50325TD	Not included except D-Version	Included
Thermal Sensing		Not available	Not available	Available

3. Package

3.1. Internal Circuit Diagram

Major differences between Version 2 and previous versions are red in the internal circuit diagram in Figure 2. Though some old versions also have these features, Version 2 widely adopts these features. Main differences are V_{ts}, internal connections between VS and sources of high-side FRFETs, and internal bootstrap diodes. The Vts pin is from V-phase HVIC only and sends out the temperature sensing signal.

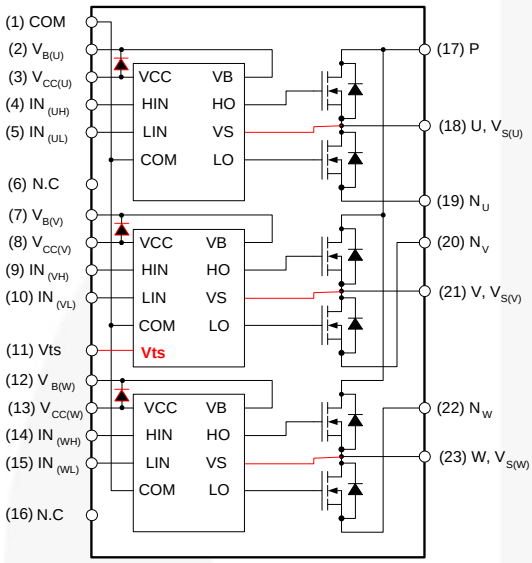


Figure 2. Internal Circuit Diagram of Motion SPM 5 Series Version 2 Products

3.2. Pin Description

Figure 3 shows the locations of pins and the names of double-DIP package. Note that Vb pins have longer leads to accommodate further creepage distance on the PCB. Figure 4 in the later section illustrates the internal layout of the module in more detail.

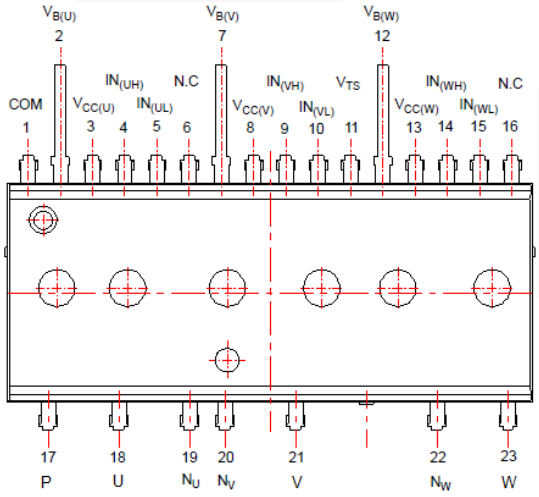


Figure 3. Pin Numbers and Names

Table 3. Pin Descriptions

Pin #	Name	Pin Description
1	COM	IC common supply ground
2	VB(U)	Bias voltage for U-phase high-side MOSFET driving
3	VCC(U)	Bias voltage for U-phase IC and low-side MOSFET driving
4	IN(UH)	Input for U-phase high-side gate signal
5	IN(UL)	Input for U-phase low-side gate signal
6	NC	No connection
7	VB(V)	Bias voltage for V-phase high-side MOSFET driving
8	VCC(V)	Bias voltage for V-phase IC and low-side MOSFET driving
9	IN(VH)	Input for V-phase high-side gate signal
10	IN(VL)	Input for V-phase low-side gate signal
11	VTS	Analog voltage output proportional to IC temperature
12	VB(W)	Bias voltage for W-phase high-side MOSFET driving
13	$V_{CC(W)}$	Bias voltage for W-phase IC and low-side MOSFET driving
14	$IN_{(WH)}$	Input for W-phase high-side gate signal
15	$IN_{(WL)}$	Input for W-phase low-side gate signal
16	NC	No connection
17	P	Positive DC-link input
18	U, $V_{S(U)}$	Output for U-phase and bias voltage ground for high-side FET driving
19	N_U	Source of U-phase low-side MOSFET
20	N_V	Source of V-phase low-side MOSFET
21	V, $V_{S(V)}$	Output for V-phase and bias voltage ground for high-side MOSFET driving
22	N_W	Source of W-phase low-side MOSFET
23	W, $V_{S(W)}$	Output for W-phase and bias voltage ground for high-side MOSFET driving

High-Side Bias Voltage Pins for Driving the High-Side MOSFET / High-Side Bias Voltage Ground Pins for Driving the High-Side MOSFET

Pins: $V_{B(U)} - U, V_{S(U)}$, $V_{B(V)} - V$, $V_{S(V)}$, $V_{B(W)} - W$, $V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the high-side MOSFETs.
- The advantage of the bootstrap scheme is that no separate external power supplies are required to drive the high-side MOSFETs.
- Each bootstrap capacitor is generally charged from the V_{CC} supply during the on-state of the corresponding low-side MOSFET.

- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality filter capacitor with low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) should be mounted very close to these pins.

Low-Side Bias Voltage Pin / High-Side Bias Voltage Pin

Pin: $V_{CC(U)}$, $V_{CC(V)}$, $V_{CC(W)}$

- These are control supply pins for the built-in ICs.
- These three pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality filter capacitor with low ESR and ESL should be mounted very close between these pins and the COM pins.

Low-Side Common Supply Ground Pin

Pin: COM

- The common (COM) pin connects to the control ground for the internal ICs.
- **Important!** To prevent switching noises caused by parasitic inductance from interfering with operations of the module, the main power current should not flow through this pin.

Signal Input Pins

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These pins control the operation of the MOSFETs.
- These pins are activated by voltage input signals. The terminals are internally connected to the Schmitt trigger circuit.
- The signal logic of these pins is active HIGH; the MOSFET turns ON when sufficient logic voltage is applied to the associated input pin.
- The wiring of each input needs to be short to protect the module against noise influences.
- An RC filter can be used to mitigate signal oscillations or any noise that traces of input signals may pick up.

Analog Temperature Sensing Output Pin

Pin: Vts

- This indicates the temperature of the V-phase HVIC with analog voltage. HVIC itself creates some power loss, but mainly heat generated from the MOSFETs increases the temperature of the HVIC.
- Vts versus temperature characteristics is illustrated in Figure 16.

Positive DC-Link Pin

Pin: P

- This is a DC-link positive power supply pin of the inverter.
- This pin is internally connected to the drains of the high-side MOSFETs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin and the negative DC-link. Figure 35 shows more details. Typically metal film capacitors are recommended.

Negative DC-Link Pins

Pins: N_U, N_V, N_W

- These are DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the source of low-side MOSFET in each phase.

Inverter Power Output Pin

Pins: U, V, W

- Inverter output pins to be connected to the inverter load, such as an electrical motor.

3.3. Package Structure

Figure 4 shows the internal package structure, including the lead frame and bonding wires. This design has been revised several times to further improve the manufacturability and the reliability for customers.

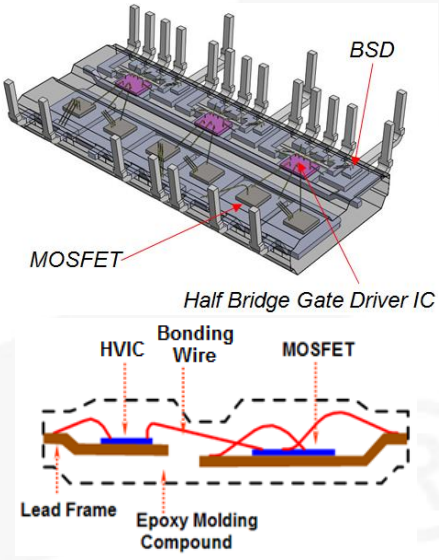


Figure 4. Package Structure

3.4. Packages

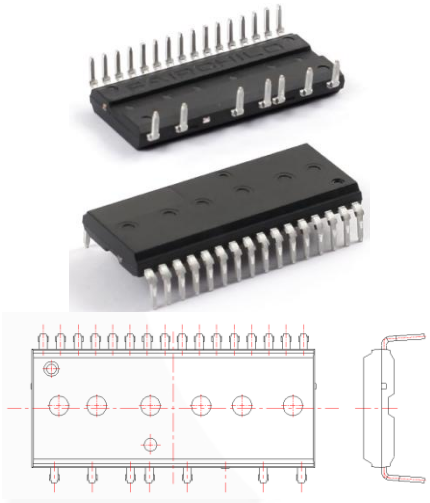


Figure 5. DIP Package

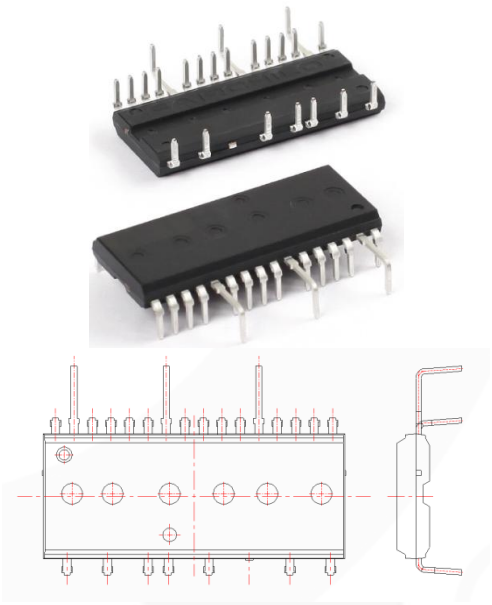


Figure 7. Double DIP 1 Package

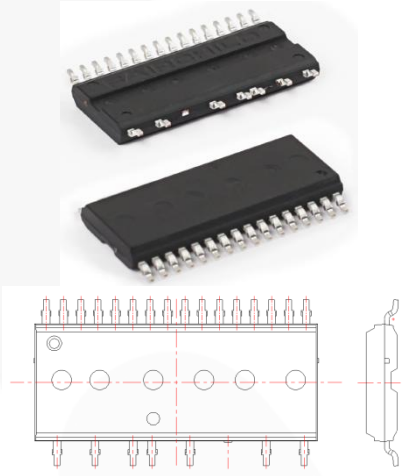


Figure 6. SMD Package

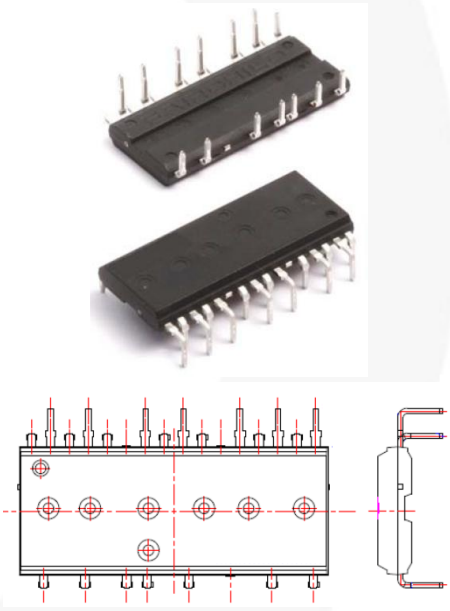
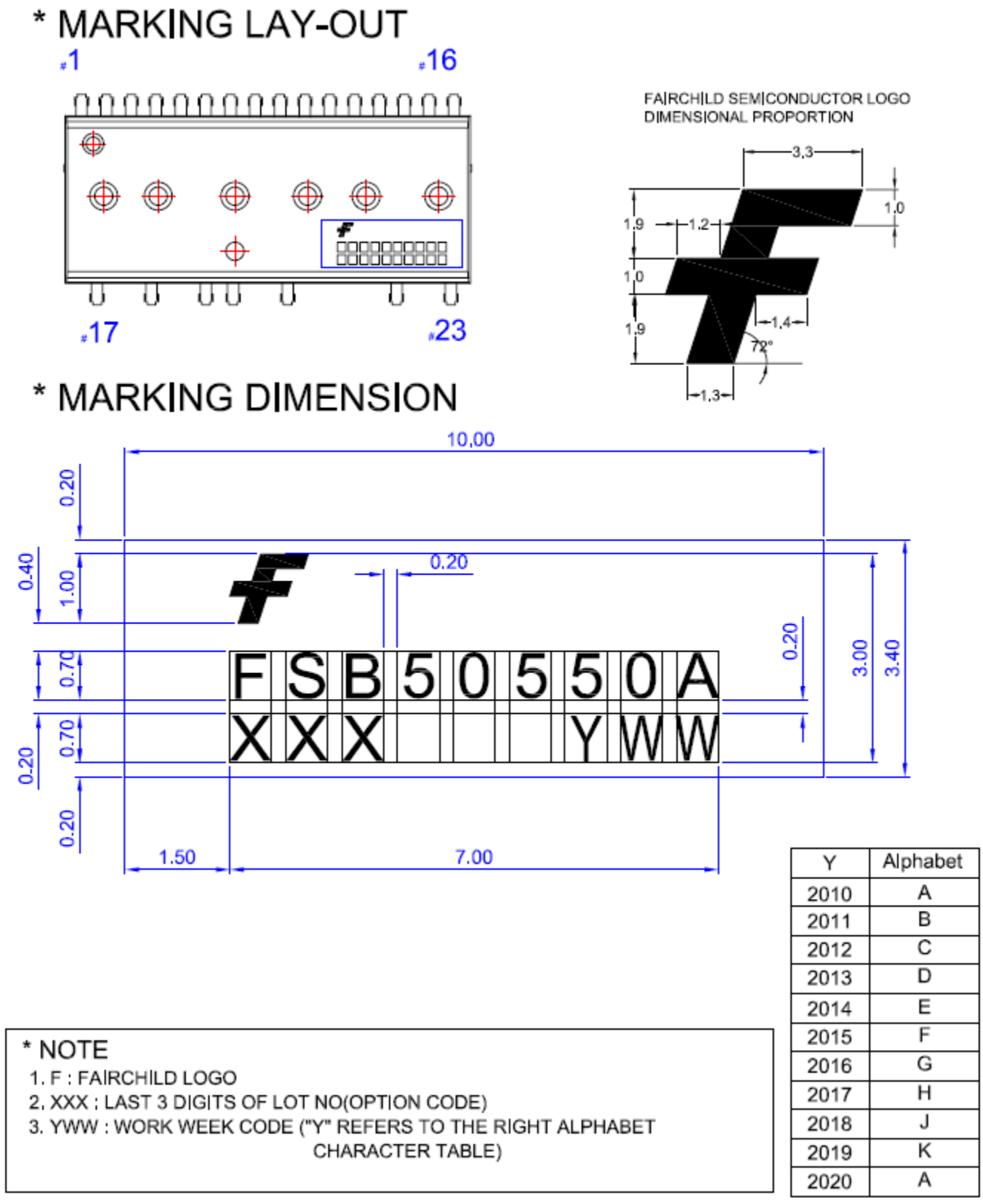


Figure 8. Zigzag DIP Package

Notes:

1. *For more detail regarding the package dimension and land pattern recommendation, please refer to each datasheet.*
2. Zigzag DIP package is only available for custom products.

3.5. Marking Specifications

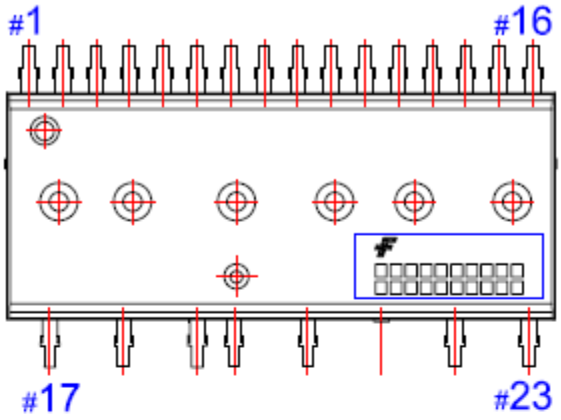


Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

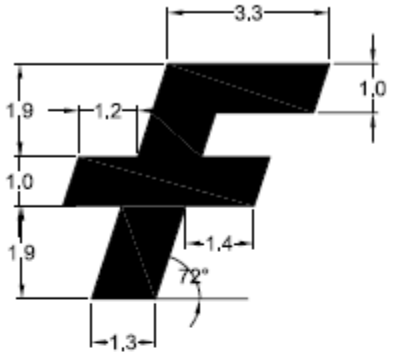
* NOTE
1. F : FAIRCHILD LOGO
2. XXX ; LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

Figure 9. Marking of DIP Package

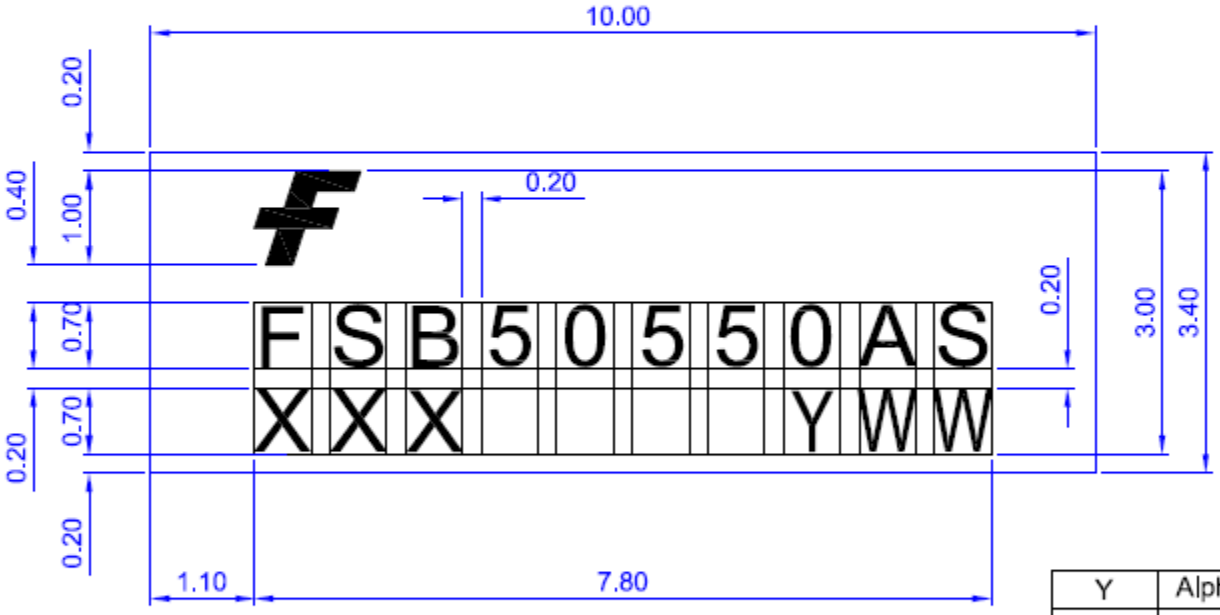
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION

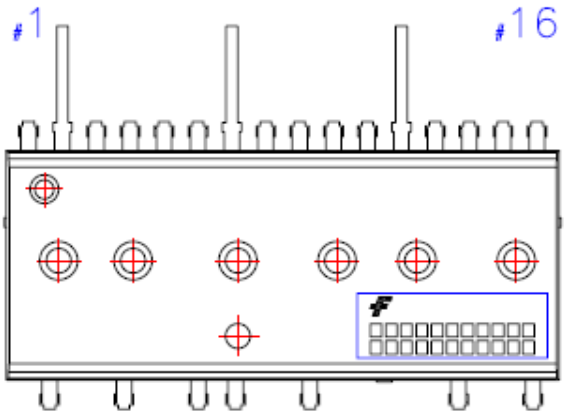


Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

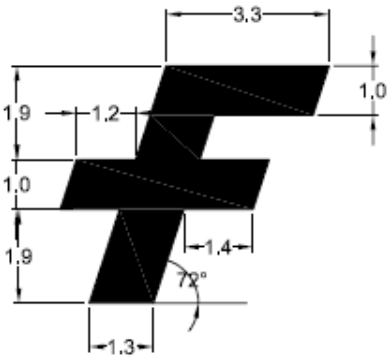
* NOTE
1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

Figure 10. Marking of SMD Package

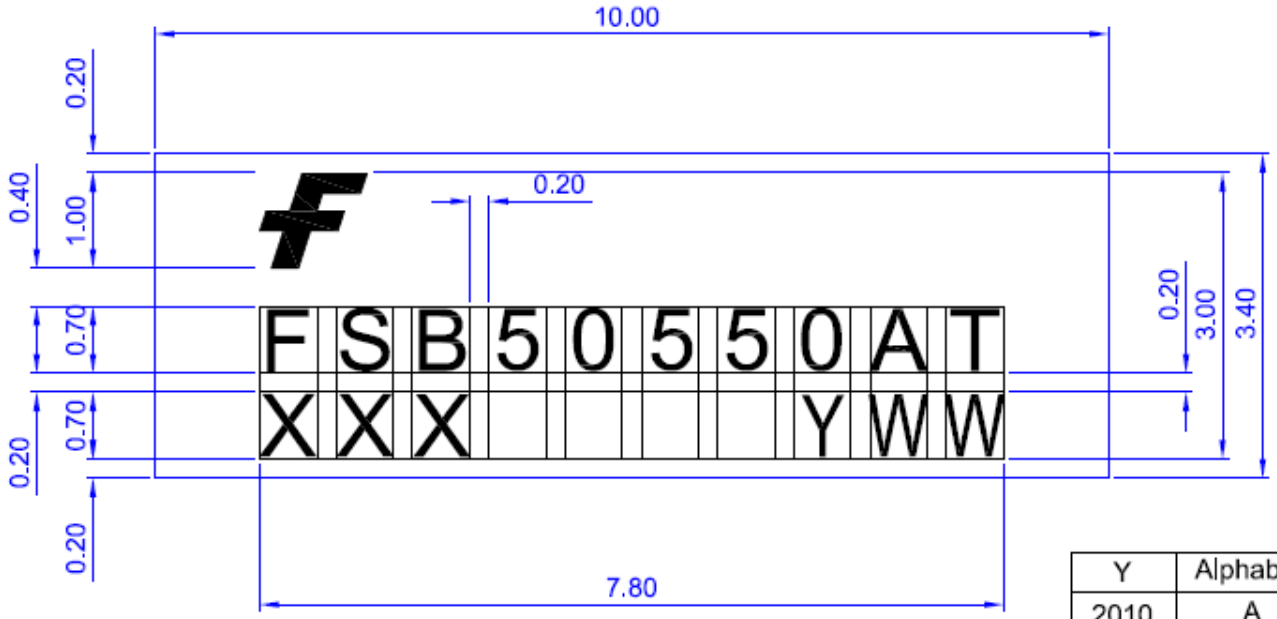
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION

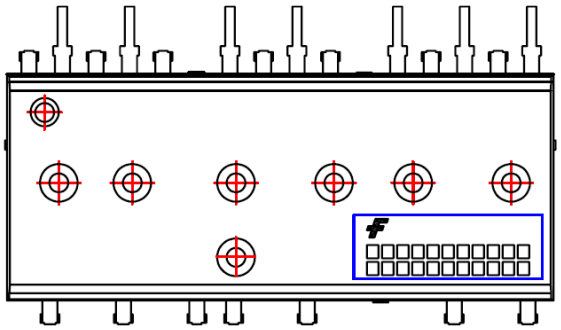


Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

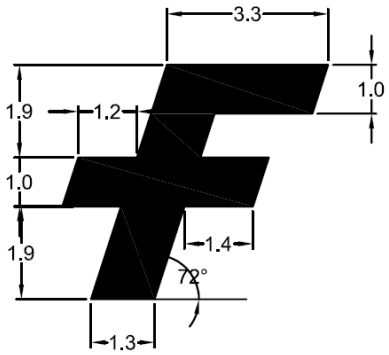
* NOTE
1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

Figure 11. Marking of Double-DIP Package

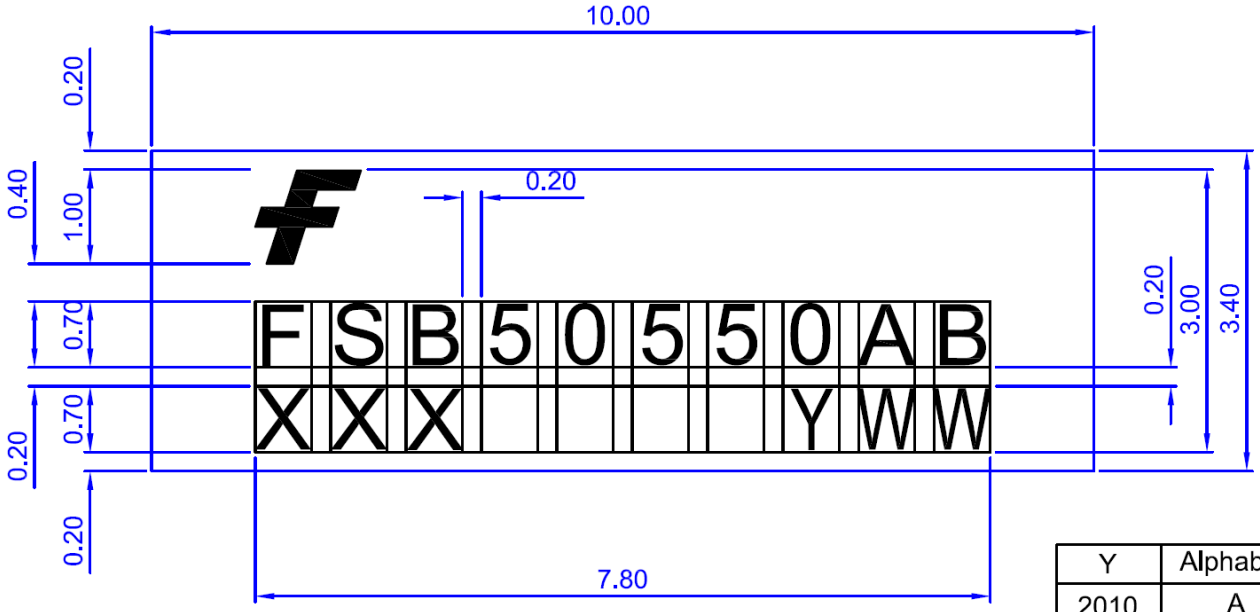
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION



Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE
1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

Figure 12. Marking of Zigzag DIP Package

4. Integrated Functions and Protection Circuit

4.1. Internal Structure of HVIC

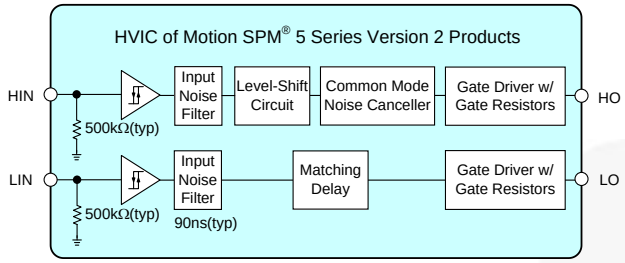


Figure 13. Internal Block Diagram of HVIC

Figure 13 shows the block diagram of the internal structure of the HVIC inside Motion SPM 5 Series V2 products. Gate signal input pins have internal 500 kΩ (typical) pull-down resistors. The weak pull-down reduces standby power consumption. If there is any concern for malfunction due to noise associated with layout, additional pull-down resistors of 4.7 kΩ, for example, are recommended close to the module input pins. RC filters can be used instead of pull-downs to reduce noise and narrow pulses as well. Keep in mind that this filter introduces some distortion of PWM volt-second because the ON/OFF threshold levels are not symmetrical within the supplied voltage.

4.2. Circuit of Input Signal ($V_{IN(H)}$, $V_{IN(L)}$)

Figure 14 shows an example of PWM input interface circuit from the microcontroller (MCU) to Motion SPM 5 Series products. The input logic is active HIGH and, because there are built-in pull-down resistors of 500 kΩ, external pull-down resistors are not typically needed.

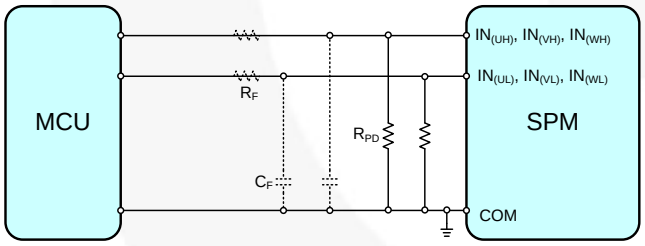


Figure 14. Recommended MCU I/O Interface Circuit

The maximum rating voltages of the input pins are shown in Table 4. The RC coupling at each input shown dotted in Figure 14 may change depending on the PWM control scheme used in the application and the wiring impedance of the application PCB layout.

Table 4. Maximum Ratings of Input Pins

Item	Symbol	Condition	Rating (V)
Control Supply Voltage	V_{CC}	Applied between V_{CC} – COM	20
Input Signal Voltage	V_{IN}	Applied between $IN_{(xH)}$ – COM, $IN_{(xL)}$ – COM	-0.3 ~ V_{CC} + 0.3

Motion SPM 5 Series products employ active-HIGH input logic. This removes the sequence restriction between the control supply and the input signal during power supply startup or shutdown. In addition, pull-down resistors are built into each input circuit. Therefore, external pull-down resistors are not typically needed and the number of external components is smaller as a result. The input noise filter inside the HVIC suppresses short pulse noise and prevents the MOSFET from malfunction and excessive switching loss. Furthermore, by lowering the turn-on and turn-off threshold voltages of the input signal, as shown in Table 5, a direct connection to 3.3 V-class MCU or DSP is possible.

Table 5. Input Threshold Voltage Ratings (at V_{CC}=15 V, T_J=25°C)

Item	Symbol	Condition	Min.	Max.
On Threshold Voltage	V_{IH}	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ – COM		2.9 V
Off Threshold Voltage	V_{IL}	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	0.8 V	

As shown in Figure 13, the input signal integrates a 500 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM® input, attention should be paid to the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100 Ω and C=1 nF can be used for the parts shown dotted in Figure 14.

4.3. Functions vs. Control Supply Voltage

Control and gate drive power for SPM 5 Series V2 products is normally provided by a single 15 V DC supply connected to the module V_{CC} and COM terminals. For proper operation, this voltage should be regulated to 15 V ±10% and its current supply should be larger than 10 mA for SPM 5 Series V2 product, excluding other circuitry. Table 6 describes the behavior of the SPM parts for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high-frequency decoupling capacitor connected right at the pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous signals. To avoid these problems, the maximum ripple on the supply should be less than ±1 V/μs. In addition, it may be necessary to connect a 20 V/1 W Zener diode (for example, 1N4747A) across the control supply to prevent surge destruction under severe conditions.

It is very important that all control circuits and power supplies should be referred to COM terminal of the module and not to the N power terminal. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout. The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high-side gate drives.

When control supply voltage (V_{CC} and V_{BS}) falls below Under-Voltage Lockout (UVLO) level, HVIC turns off the MOSFETs while disregarding gate control input signals.

Table 6. Control Voltage Range vs. Operations

Control Voltage Range [V]	Function Operations
0 ~ 4	Control IC does not operate. UVLO and fault output do not operate. dv/dt noise on the main P-N supply might trigger the MOSFETs.
4 ~ 10	Control IC starts to operate. As the UVLO is set, gates of MOSFETs are pulled down regardless of control input signals.
10 ~ 13.5	UVLO is cleared. MOSFETs operate in accordance with the control gate input. Because driving voltage is below the recommended range, $R_{DS(on)}$ and the switching loss is higher than under normal conditions.
13.5 ~ 16.5 for V_{CC} 13.5 ~ 16.5 for V_{BS}	**Normal operation. This is the recommended operating condition.**
16.5 ~ 20 for V_{CC} 16.5 ~ 20 for V_{BS}	MOSFETs still operate. Because driving voltage is above the recommended range, MOSFETs switch faster and system noise may increase. The peak of short-circuit current may increase as well.
Over 20	Control circuit in the module might be damaged.

4.4. Under-Voltage Lockout (UVLO)

The half-bridge HVIC has under-voltage lockout function to protect MOSFETs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 15.

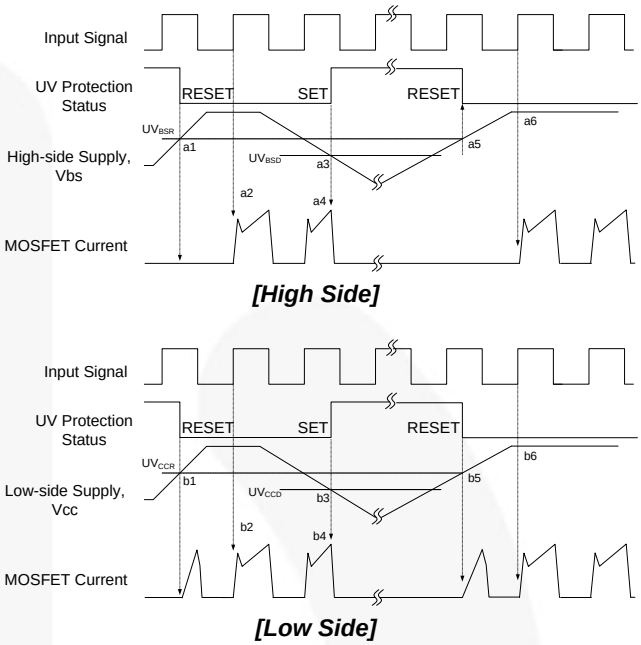


Figure 15. Timing Chart of Under-Voltage Protection

a1: Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuit starts to operate when next input comes in.

a2: Normal operation: MOSFET turns on and carries current.

a3: Under-voltage detection (UV_{BSD}).

a4: MOSFET turns off regardless of control input condition, but there is no fault output signal because the SPM 5 series does not have an FO pin.

a5: Under-voltage lockout cleared (UV_{BSR}).

a6: Normal operation: MOSFET turns on and carries current.

b1: Control supply voltage rises: After the voltage rises UV_{CCR}, the circuit starts to operate immediately.

b2: Normal operation: MOSFET turns on and carries current.

b3: Under-voltage detection (U_{VCCD}).

b4: MOSFET turns off regardless of control input condition, but there is no fault output signal because SPM 5 series does not have FO pin.

b5: Under-voltage lockout cleared (UV_{CCR}).

b6: Normal operation: MOSFET turns on and carries current.

5. New Parameter Design Guidance

5.1. Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the T_{jmax} specified on the datasheet and the T_{jmax} at which power devices are destroyed, attention should be paid to ensure the junction temperature stays well below the T_{jmax}. One of the inconveniences in using previous versions of SPM 5 Series products was lack of temperature monitoring or protection feature inside the module. An NTC had to be mounted on the heat sink or very close to the module if over-temperature protection was required in the application.

Thermal Sensing Unit (TSU) uses the technology based on the temperature dependency of transistor V_{be}; V_{be} decreases 2 mV as temperature increases 1ºC.

The TSU analog voltage output reflects the temperature of the HVIC in Motion SPM 5 Series products. The relationship between V_{ts} output and HVIC temperature is shown in Figure 16. It does not have any self-protection function and, therefore, it should be used appropriately based on application requirement. Note that there is a time lag from MOSFET temperature to HVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition, such as load step changes. Even though TSU has limitations, it is definitely useful in enhancing the system reliability.

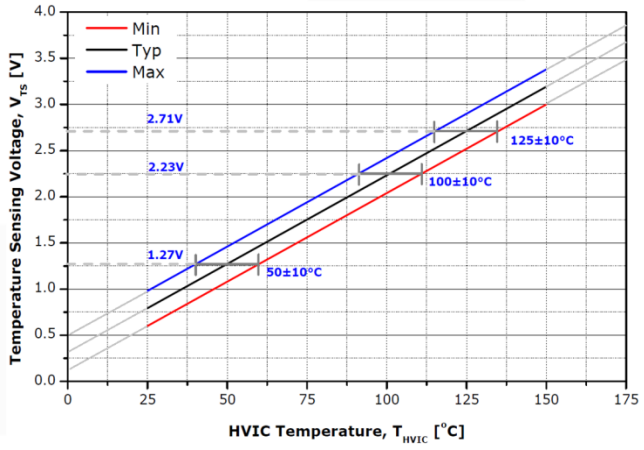


Figure 16. Temperature vs. V_{ts}

The relationship between V_{ts} and V-phase HVIC temperature can be expressed as the following equation:

$$V_{TS}\,[V] = 0.0192 * T_{HVIC}\,[^{o}C] + 0.31 \pm 0.19 \qquad (1)$$

The maximum variation of V_{ts} due to process variation is ±0.19 V, which is equivalent ±10ºC. This amount is constant, regardless of the temperature because the slopes of three lines in Figure 16 are identical. If the ambient temperature information is available, for example, through NTC in the system, V_{ts} can be measured to adjust the offset before the motor starts to operate.

As temperature decreases further below 0ºC, V_{ts} decreases linearly until it reaches zero volts. If the temperature of HVIC increases above 150ºC, which is above the maximum operating temperature, V_{ts} increases (theoretically) up to 5.2 V until it gets clamped by the internal Zener diode.

Figure 17 shows the equivalent circuit diagram of TSU inside the IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but if the maximum input range of analog-to-digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the analog-to-digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between VTS and COM (ground) to make the V_{ts} more stable. If V_{CC} is not supplied for any reason, V_{ts} is longer available.

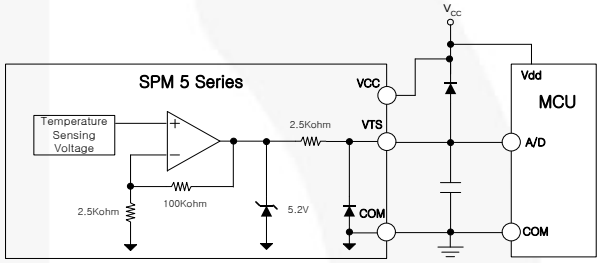


Figure 17. Internal Block Diagram, TSU Interface Circuit

Figure 18 shows the sourcing capability of VTS pin at 25 ºC and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to VTS pin should be minimized to maintain the accurate voltage output level without degradation.

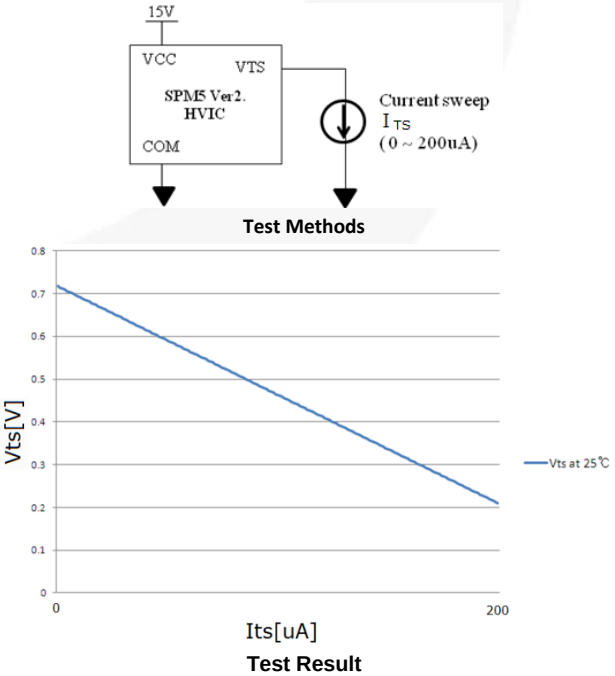


Figure 18. Load Variation of V_{ts}

Figure 19 shows that the V-phase HVIC temperature inferred from V_{TS} follows closely the case temperature, T_C, with some lag. The amount of loss in a single MOSFET in a given operating condition can be calculated by Fairchild's online loss and temperature simulation tool, available at: http://www.fairchildsemi.com/support/design-tools/motion-control-design-tool/. By using the loss from this simulation and the thermal resistance value on the datasheet, together with TSU, the junction temperature can be estimated and controlled to stay below the target junction temperature.

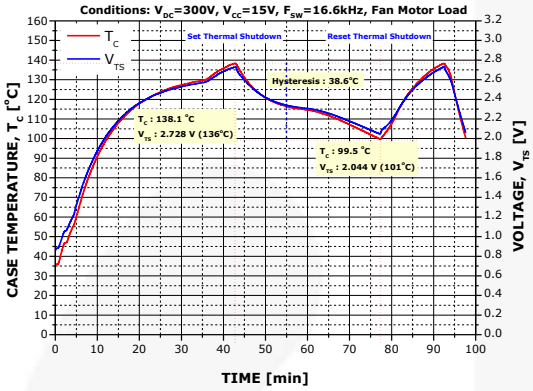


Figure 19. OTP Test in Real Application

Figure 20 is an example of over-temperature protection circuit using the V_{ts} signal. A comparator with hysteresis is used to create a low active OT signal that can be read by a microprocessor. Based on this signal, the microprocessor can disable or enable PWM output. Calculate the resistor values to make the upper threshold level 100ºC and the lower threshold level 80ºC so that the comparator output voltage V_O matches the waveform in Figure 21.

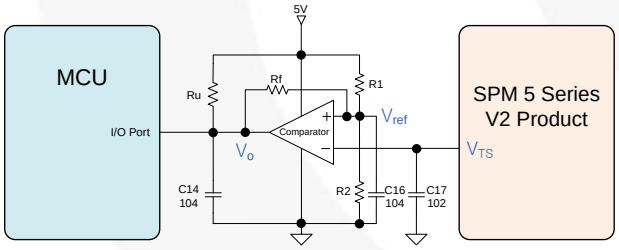


Figure 20. Example of OTP Using TSU

When the temperature is below 80ºC; V_O, the open-collector output of the comparator, should stay HIGH. To make V_O transition to LOW at 100ºC, V_{REF} needs to go below 2.230 V, which is V_{TS} voltage at 100ºC.

$$\frac{1}{\frac{1}{R_1}+\frac{1}{R_u+R_f}} = R_1' \qquad \frac{R_2}{R_1'+R_2}\times 5 = V_{ref} \le 2.230V \tag{2}$$

When the temperature is above 100ºC, V_O should stay LOW. To make V_O transition to HIGH at 80ºC, V_{REF} needs to be higher than 1.846 V, which is V_{TS} voltage at 80ºC.

$$\frac{1}{\frac{1}{R_f}+\frac{1}{R_2}} = R_2' \qquad \frac{R_2'}{R_1+R_2'}\times 5 = V_{ref} \ge 1.846V \tag{3}$$

There are four variables with two equations and, therefore, set both variables as desired. R_u, the pull-up resistor for V_O, can be chosen to be 10 kΩ. R2 can be 1 kΩ, considering V_{REF} is below one half of the supply voltage, which is 5 V in this example, and R1 needs to be bigger than R2. A Microsoft® Excel® Solver can be used to get the answer of R1=1364 Ω and R_f= 3952 Ω. Close standard resistor values would be 1.37 kΩ and 3.92 kΩ. These two resistor values result in V_{TS_off} of 2.225 V, which is 99.7°C and V_{TS_on} of 1.839 V, which is 79.6°C.

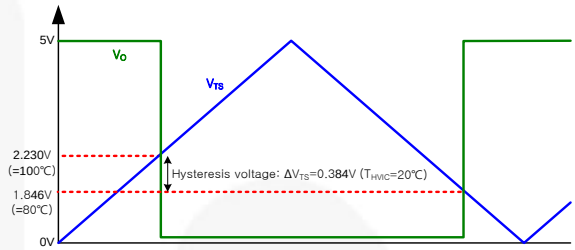


Figure 21. Comparator Output with Hysteresis Using TSU

5.2. Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between VB (U, V, W) and VS (U, V, W), provides the supply to the HVIC within Motion SPM 5 Series V2 products. This supply must be in the range of 13.5 V~16.5 V to ensure that the HVIC can fully drive the high-side MOSFET. The SPM5 V2 products include under-voltage lockout protection for V_{BS} to ensure that the HVIC does not drive the high-side MOSFET if the V_{BS} voltage drops below the specific voltage shown on the datasheet. This function prevents the MOSFET from operating in a high-dissipation mode.

The V_{BS} floating supply can be generated in a number of ways, including the bootstrap method shown in Figure 22. This method is simple and inexpensive; however, the duty cycle and on-time are limited by the need to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of bootstrap diode, resistor, and capacitor, as shown in Figure 22.

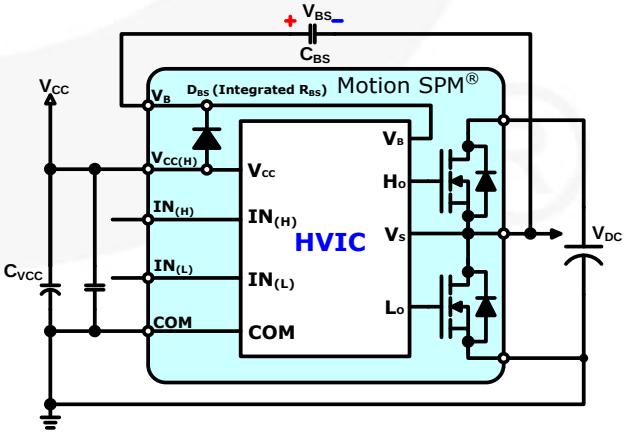


Figure 22. Bootstrap Circuit for the Supply Voltage (V_{BS}) of HVIC

The current flow path of the bootstrap circuit is show in Figure 23. When V_S is pulled down to ground (either through the low-side power device or the load), the bootstrap capacitor, C_{BS}, is charged through the bootstrap diode (DBS) and the resistor from the V_{CC} supply. The bootstrap resistor is not included in Figure 23 because the bootstrap diode in SPM 5 Series version 2 products has resistive characteristics.

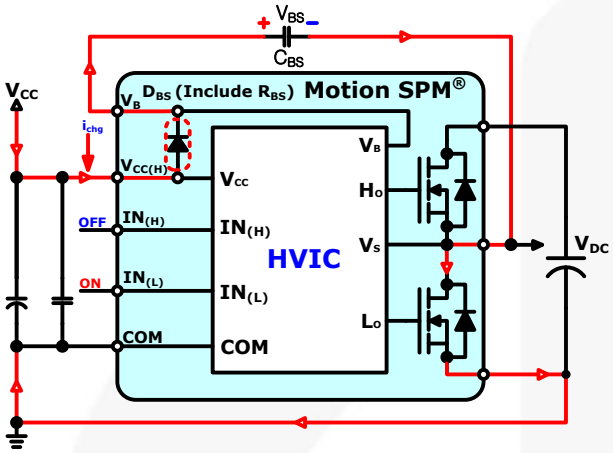


Figure 23. Bootstrap Circuit Charging Path

Built-in Bootstrap Diode

When the high-side MOSFET or body diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage, so a diode with withstand voltage of more than 500 V is required. It is important that this diode has a recovery time of less than 100 ns characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the V_{CC} supply. The bootstrap resistor is necessary to slow down the dV_{BS}/dt and limit initial charging current (I_{charge}) of the bootstrap capacitor.

Figure 24 shows the built-in bootstrap diodes of SPM5 V2 products' special V_F characteristics to be used without additional bootstrap resistors. Therefore, only external bootstrap capacitors are needed to make a bootstrap circuit.

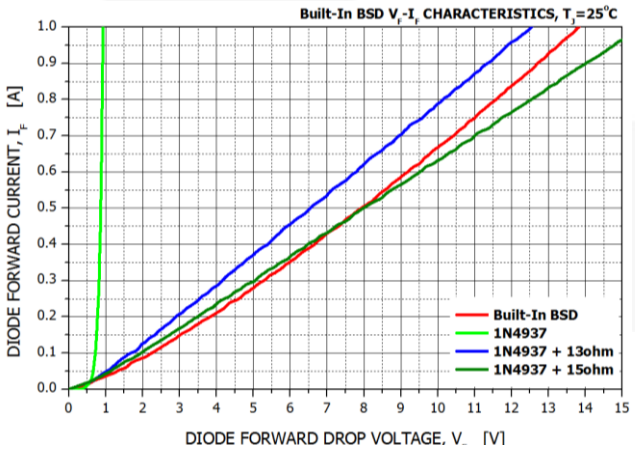


Figure 24. V-I Characteristics of Bootstrap Diode in SPM5 V2 Products

The characteristics of the built-in bootstrap diode in the SPM5 V2 products are:

- Fast recovery diode: 600 V / 0.5 A
- Typical t_{rr}: 80 ns
- Resistive characteristic: equivalent resistor: ~15 Ω

Table 7 shows the forward-voltage drop and reverse-recovery characteristics of the bootstrap diode.

Table 7. Bootstrap Diode Specifications

Symbol	Parameter	Condition	Typ.
V_F	Forward-Drop Voltage	I_F=0.1 A, T_C=25°C	2.5 V
t_{rr}	Reverse-Recovery Time	I_F=0.1 A, T_C=25°C	80 ns

Table 8. Bootstrap Diode Absolute Max. Ratings

Symbol	Parameter	Condition	Rating
V_{RRMB}	Maximum Repetitive Reverse Voltage		600 V
I_{FB}(3)	Forward Current	T_C=25°C	0.5 A
I_{FPB}(3)	Forward Current (Peak)	T_C=25°C, Under 1 ms Pulse Width	1.5 A

Note:

3. Calculated values or design parameters.

Initial Charging of Bootstrap Capacitor

Adequate on-time of the low-side MOSFET to fully charge the bootstrap capacitor is required before normal operation of PWM starts. Figure 25 shows an example of initial bootstrap charging sequence. Once V_{CC} establishes, V_{BS} must be charged by turning on low-side MOSFETs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals.

The capacitance of V_{CC} should be sufficient to supply necessary charge to V_{BS} capacitance of all three phases. If normal PWM operations start before V_{BS} reaches the under-voltage lockout reset level, high-side MOSFETs do not switch accordingly without creating any fault signal. This may lead to a failure of motor start in some applications.

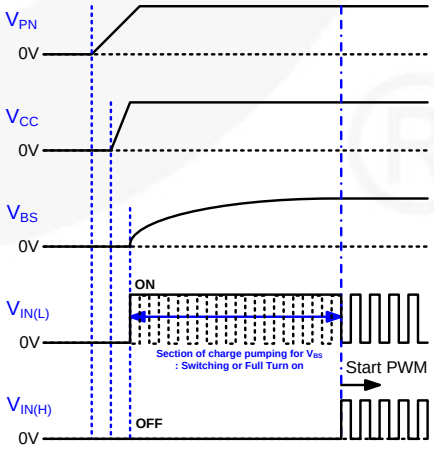


Figure 25. Timing Chart of Initial Bootstrap Charging

If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level. In that case, a sequential charging among three phases is more appropriate.

The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BS} \bullet (R_{BS} + R_{DS\_ON}) \bullet \frac{1}{\delta} \bullet \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}}\right) \quad (4)$$

where:

V_F: forward-voltage drop across the bootstrap diode;
$V_{BS(min)}$: minimum value of the bootstrap capacitor;
V_{LS}: voltage drop across the low-side MOSFET or load; and
δ: duty ratio of PWM (0 – 1).

V_F is actually not a constant and varies depending on the amount of bootstrap charging current. V_{LS} changes by the magnitude and direction of the phase output current in normal operation. R_{DS_ON} drop by bootstrap charging current must be considered because phase output current can be assumed to zero at initial charging. V_{LS} can be regarded as zero and R_{DS_ON} needs to be part of RC time constant. In that case, V_F needs to set as approximately 1 V, which is the value of a non-resistive diode, and R_{BS} needs to be 15 Ω.

Figure 26 and Figure 27 show real waveforms of the initial bootstrap capacitor charging. Figure 26 is with 1 µF capacitor and Figure 27 is with 47 µF capacitor to demonstrate two extreme cases. In Figure 26, bootstrap voltage charges to 13 V in 25 µs, but in Figure 27 it takes several ms at 50% duty. The initial peak current values are about 1 A, which can be expected from Figure 24.

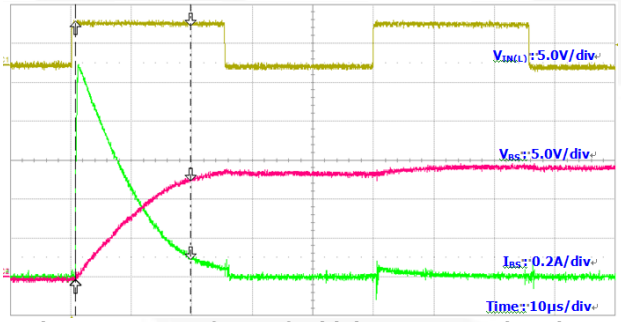


Figure 26. Waveform of Initial Bootstrap Charging (Conditions: V_{DC}=300 V, V_{CC}=15 V, C_{BS}=1 µF, LS MOSFET Turn-on Time=25 µs)

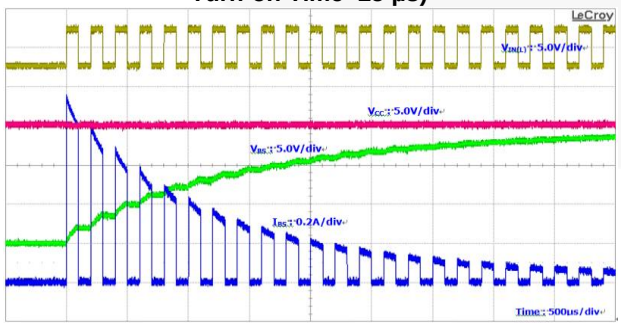


Figure 27. Waveform of Initial Bootstrap Charging (Conditions: V_{DC}=300 V, V_{CC}=15 V, C_{BS}=47 µF, LS MOSFET Turn-on Time=100 µs)

Selection of Bootstrap Capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} \quad (5)$$

where:

Δt: maximum on pulse width of high-side MOSFET;
ΔV_{BS}: allowable discharge voltage (voltage ripple) of the C_{BS}; and
I_{Leak}: maximum discharge current of the C_{BS}, including:

- Gate charge for turning the HS MOSFET on
- Quiescent current to the HS circuit in the HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (can be ignored for non-electrolytic capacitors)
- Bootstrap diode reverse-recovery charge.

Practically, 1 mA of I_{Leak} is recommended for Motion SPM®5 Series V2 products. By considering dispersion and reliability, the capacitance is generally selected to be twice the calculated one. The C_{BS} is only charged when the high-side MOSFET is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side MOSFET must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, there is an inherent minimum on-time for the low-side MOSFET (or off-time of the high-side MOSFET).

Bootstrap Capacitance Calculation Examples

Examples of bootstrap capacitance calculation:

I_{Leak} = 1.0 mA (recommended value)

ΔV_{BS} = 0.1 V (recommended value)

Δt = Maximum on pulse width of high-side MOSFET = 0.2 ms. (depends on user system)

$$C_{BS\_min} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} = \frac{1mA \times 0.2ms}{0.1V} = 2.0 \times 10^{-6} \quad (6)$$

→ More than two times → 4.7 µF.

Note:

4. This capacitance value can be changed according to the switching frequency, the type of capacitor used, and recommended V_{BS} voltage of 13.5~16.5 V (from datasheet). The above result is a calculation example and should be changed according to the actual control method and lifetime of component.

Figure 28 shows bootstrap capacitance value versus switching frequency with maximum discharge current of 2 mA.

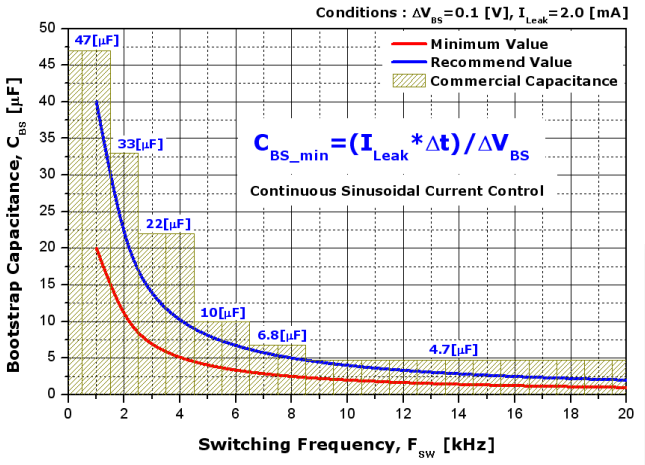


Figure 28. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

5.3. Minimum Pulse Width

As shown in Figure 29, there are input noise filters of 90 ns time constant inside the HVIC. It screens out pulses narrower than the filter time constant. Additional propagation delay in level-shifters and other circuits, together with gate charging time, prevent SPM 5 products from responding to an input pulse narrower than ~120 ns.

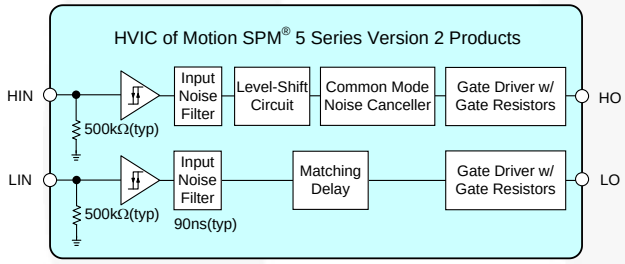


Figure 29. Internal Structure of Signal Input Pins

Figure 30 shows definitions of t_{on_pw} and t_{off_pw} illustrated in Figure 31. t_{on_pw} is the minimum pulse width of PWM ON signal required to make V_{DS} decrease to zero, as shown on the left side of Figure 30. t_{off_pw} is the minimum pulse width of PWM OFF signal required to make I_D decrease to zero.

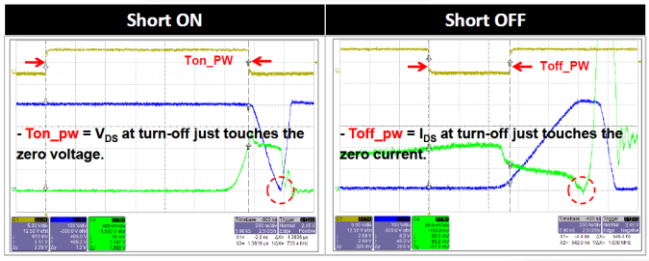


Figure 30. Definition of t_{on_pw} and t_{off_pw}

Figure 31 shows variations of t_{on_pw} and t_{off_pw} as the I_D and T_J of FSB50450A changes. As I_D increases, t_{on_pw} increases, but t_{off_pw} does not change much. As T_J increases, t_{on_pw} decreases, but t_{off_pw} does not vary much.

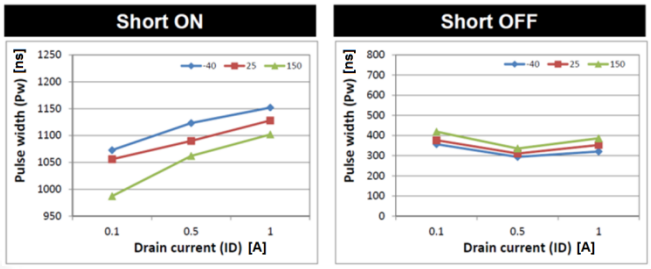


Figure 31. t_{on_pw} and t_{off_pw} vs. I_D and T_J of FSB50450A

It is not included in this graph; but as V_{CC} increases, t_{on_pw} decreases and t_{off_pw} increases.

5.4. Short-Circuit SOA

SPM 5 Series products have MOSFETs and endure longer than IGBT-based modules when short-circuit situations occur. Figure 32 is the test circuit used to measure short-circuit withstanding time and the definitions of the terms used in the measurement. The low-side MOSFET is shorted with a wire and the high-side device is turned on.

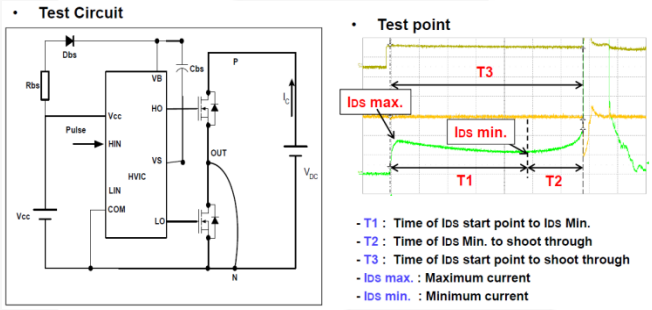
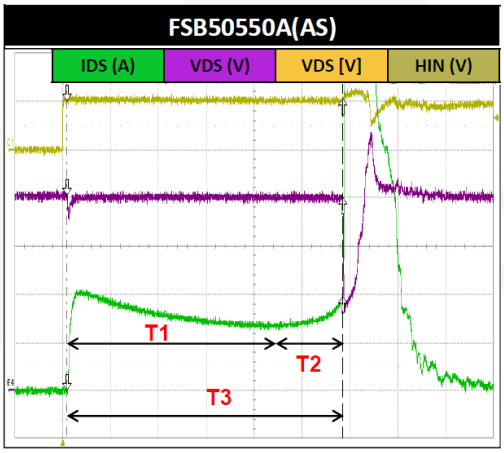


Figure 32. Short Circuit Withstanding Time Test

Figure 33 is a waveform of FSB50550A at a short-circuit condition of V_{DC}=400 V, V_{CC}=V_{BS}=20 V, T_J=150°C. Even in this type of extreme condition, FSB50550A demonstrates its ability to endure short-circuit conditions several times longer than IGBT modules.



Product	Current		Time [us]		
	Min. [A]	Max. [A]	T1	T2	T3
FSB50550A	13.77	20.23	26.48	9.22	35.70

Figure 33. SCWT of FSB50550A at Worst Condition

6. Application Example

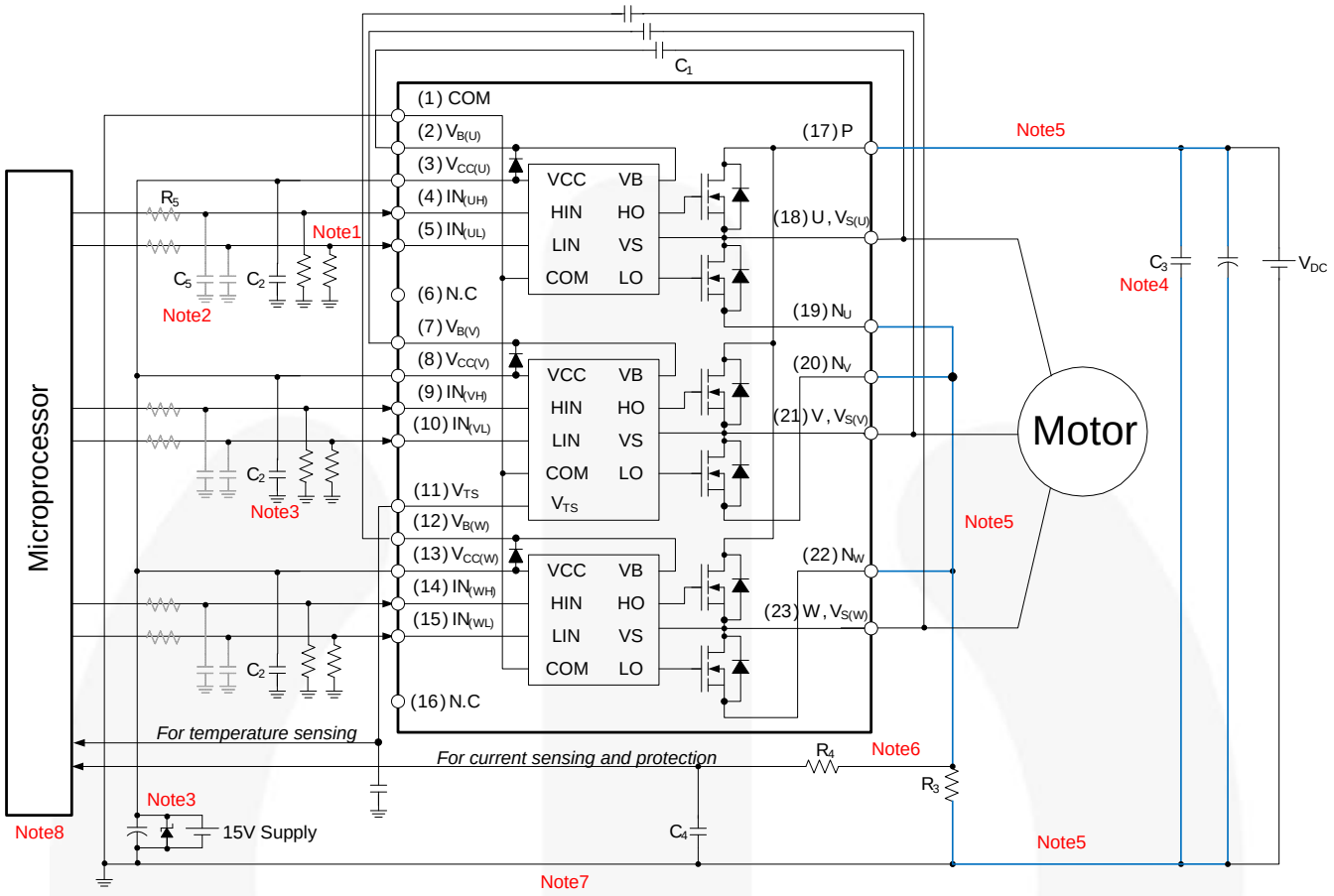


Figure 34. Example of Application Circuit

Notes:

1. Gate signal inputs are active-HIGH with 500 kΩ internal pull-down resistors. However, an additional 4.7 kΩ pull-down resistor is recommended for each gate signal input to prevent malfunction induced by switching noise.
2. Shorter traces are desirable between the microprocessor and the power module. If necessary, RC filters can be employed on gate signals to suppress noise coupled from power traces and remove very narrow pulses. RC values should be selected for input signals to be compatible with the turn-on and turn-off threshold voltages. Keep in mind that this RC filter may alter the timing of PWM and the resulting volt-second.
3. Each HVIC needs to have a 1 µF cermaic capacitor close to V_{CC} pin and possibly to the COM pin to supply instantaneous power. An electrolytic capacitor of 10 µF is required to supply stable V_{CC} voltage to the module. A Zener diode can be used in parallel to ensure V_{CC} does not increase beyond a certain voltage at surge events.
4. A high-frequency non-inductive capacitor, C3, of around 0.1~0.22 µF/600 V should be placed very close to the module and between P and the ground side of the shunt resistor, R3.
5. PCB traces for the main power paths between DC bus capacitors and the module should be as short as possible to minimize the noise associated with the parasitic inductance. These traces are colored in blue.
6. The current feedback trace should be connected directly from the shunt resistor (Kelvin connection) to get a clean and undistorted signal.
7. The power ground and the signal ground need to be connected at a single point to prevent switching noise on the power side from interfering with control signals.
8. Relays are commonly used in all home appliances electrical equipment and should be kept a sufficient distance from the microprocessor to avoid electromagnetic interference.

6.1. Recommended Wiring of Shunt Resistor

External current-sensing resistors are applied to detect phase current. A longer pattern between the shunt resistor and SPM pins cause large surge voltages that might damage built-in ICs and distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistor and SPM pins should be as short as possible. Parasitic impedance between the shunt resistor and the power module pins should be less than 10 nH, which results from a trace in 3 mm width, 20 mm length, and 1 oz thickness.

6.2. Snubber Capacitor

As shown in Figure 35, snubber capacitors should be carefully located to suppress surge voltages effectively. A 0.1~0.22 µF snubber capacitor is generally a recommended.

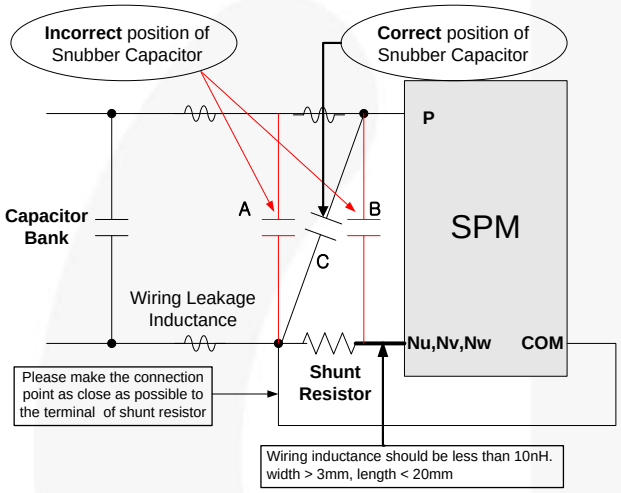


Figure 35. Recommended Wiring of Shunt Resistor and Snubber Capacitor

If the snubber capacitor is installed in location A in Figure 35, it cannot suppress the surge voltage effectively due to parasitic impedance of the traces between the capacitor and the module. If the capacitor is installed in location B, surge suppression is more effective because the snubber capacitor is connected right at the module power pins. However, in case a single shunt resistor is used for phase current reconstruction or over-current protection, the voltage across the shunt resistor cannot correctly reflect the DC bus current information consumed by the module and, therefore, the current feedback signal is distorted. The C position is a reasonable compromise with better suppression than location A, without impacting the current sensing signal accuracy. For this reason, location C is generally used.

6.3. PCB Layout Guidance

Figure 36 shows an example of PCB layout for a fan application. This “donut” shape of the board facilitates the inclusion of the board within the motor frame. The compact size of Motion SPM 5 Series is the key to overcome the mechanical challenge in this type of design. More detailed guidelines can be found in Fairchild reference designs RD-FSB50450A and RD-FSB50760SF.

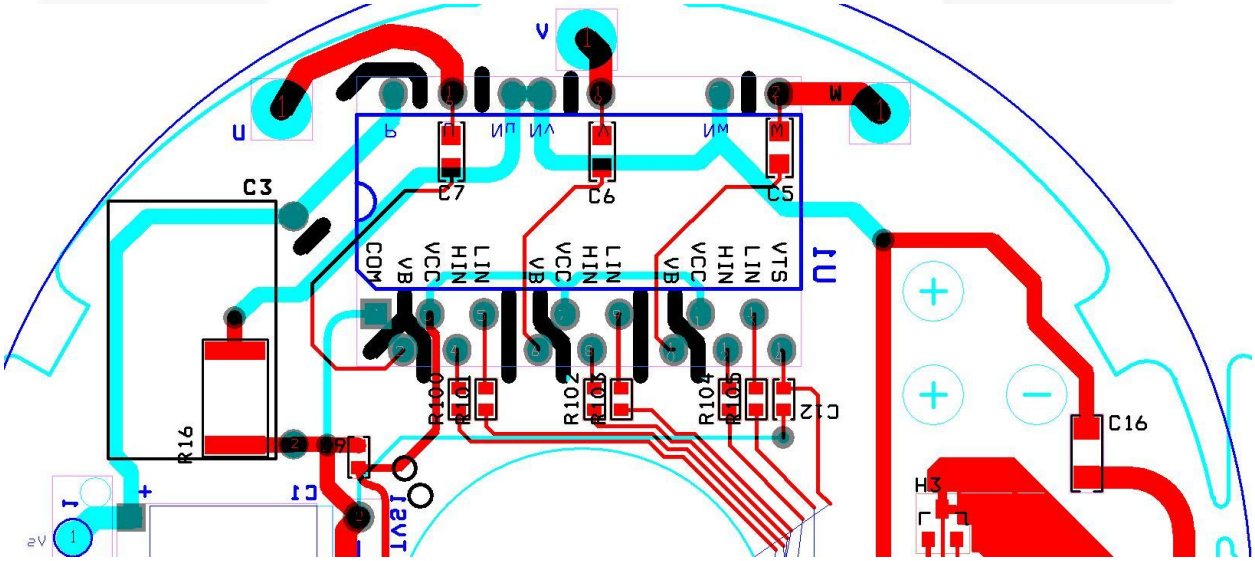


Figure 36. PCB Layout Example

6.4. Heat Sink Mounting

Recommended Cooling Method

Motion SPM 5 Series does not have screw holes for mounting a heat sink on top of the module because it is a very compact device aiming for small power applications. However, if it is desired to extend the power capability of the module by attaching a heat sink, this section introduces several methods. Temperature rise of power semiconductors is coming from the non-ideal aspects of switching devices; such as IGBT, MOSFET, and diode. When the switching device turns on, the forward-voltage drop results in conduction loss and the finite rise and fall time of current and voltage during the switching period create switching loss. These power losses make the junction temperature, as well as the case temperature, rise and the thermal resistance of each package plays an important role, as shown in the formula:

$$\mathbf{T_J\text{-}T_C = (Power\ loss) \times (Thermal\ Resistance\ between\ Junction\text{-}to\text{-}Case)} \quad (7)$$

Therefore, to decrease the case temperature and increase the SOA area, total thermal resistance and power losses must be minimized. Heat-sink, one of the most popular cooling methods of power devices, decreases the thermal resistance between the package case and the ambient. A heat-sink can improve the thermal performance by spreading the heat to the ambient more effectively. Anything with comparably high thermal conductivity can be used as a heat-sink. For example, even a PCB pattern can be a heat-sink if it has enough cooling areas. DIP without stand-offs and SMD products can benefit from this cooling area contacting the bottom-side of the module on the PCB. Thicker and wider patterns of power pins are useful in a similar fashion. Figure 37 shows a typical test board for Motion SPM 5 Series without cooling area. Figure 38 shows a test board with cooling area on the PCB surfacing the bottom side of the module and with wider traces for power pins.

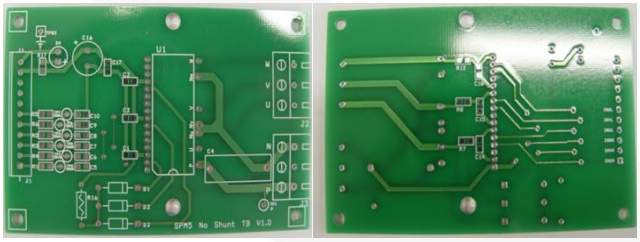


Figure 37. Test Board without Cooling Area

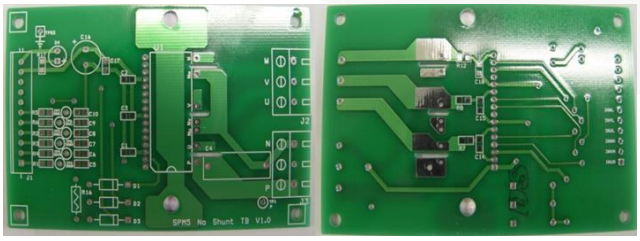


Figure 38. Test Board with Cooling Area of Copper Plane Under the Module and Thick Power Pins

Because Motion SPM 5 Series does not have screw holes, flatness of the top surface is not specified on the datasheet. But because of its compact size, warpage is below several tens of µm. Special methods are required to install a heat sink, as shown in Figure 39.

Adhesive material with high thermal conductivity, such as Loctite® 384, can be used to fix the heat sink on the top surface, as shown in Figure 39(a).

Another way to mount a heat sink is to use screws throughout the PCB and the heat sink as shown in Figure 39(b). SPM 5 products should be soldered first. Excessive torque may bend the PCB.

Fairchild has developed a special metal strip that fits in the slit on the bottom side of SPM5 package, as shown in Figure 39(c). The heat sink can be mounted on the module first before the soldering process.

A heat sink with leads can be used, as shown in Figure 39(d). Keep good contact between the top surface of the module and the heat sink during the soldering process.

Using the chassis for heat-sink, as shown in Figure 39(e), can be an effective solution for built-in applications. But it is difficult to maintain mechanical accuracy in assembly and flexible thermal interface material is often used to fill the gap between module and the chassis.

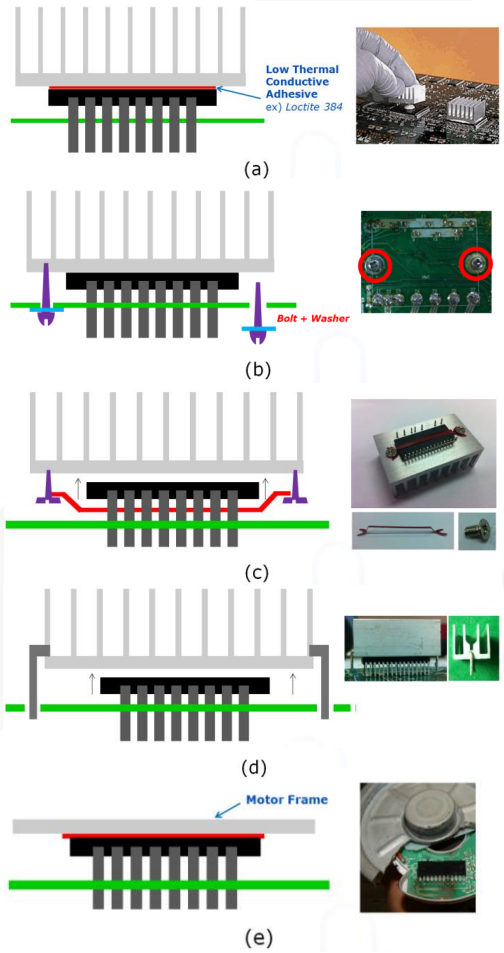


Figure 39. Heat Sink Installation Methods

Silicon Thermal Compound

Silicone thermal compound, also called thermal grease, should be applied between the heat sink and the flat surface of the SPM 5 Series to fill microscopic air gaps due to imperfect flatness that ultimately reduce the contact thermal resistance. Thermal conductivity of thermal compound is about 0.5 – 10 W/(mK) and far greater than that of air (0.024), but far smaller than that of metal (Aluminum 220, Copper 390). It should not be used too much; a uniform layer of 100 ~ 200 μm thickness is desired.

6.5. System Performance

A fan motor for an air-conditioner indoor unit has been tested to provide comparison data between Motion SPM 5 Series V2 and competitive products.

Figure 40 illustrates the power loss of single power device, such as MOSFET or IGBT. FSB50450A (Motion SPM 5 Series V2 – 500 V / 1.5 A) shows the lowest conduction loss and switching loss compared to competitive products in the same operating conditions. This lowest power loss with Motion SPM 5 Series V2 means better energy efficiency in the system.

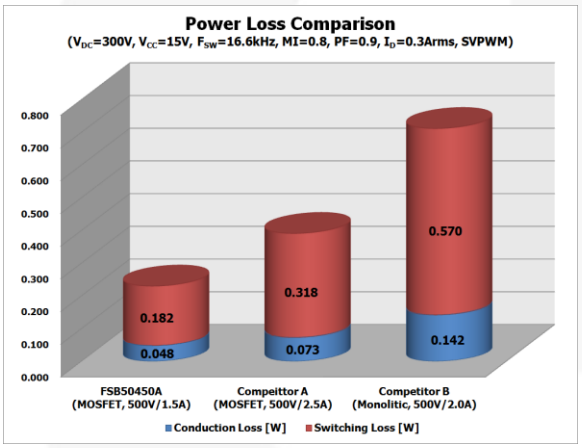


Figure 40. Power Loss Comparison

Figure 41 shows the test bench setup and the case temperature comparison result. FSB50450A shows outstanding thermal performance compared to its competition in the same operating conditions.

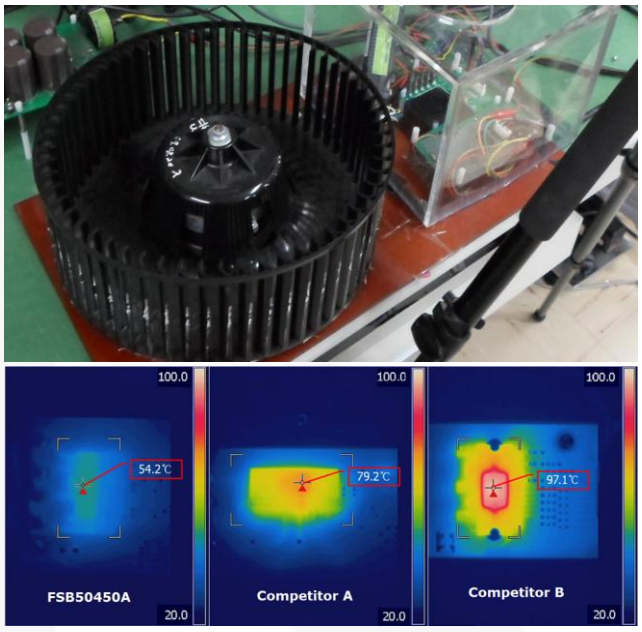


Figure 41. Case Temperature Comparison of SPM 5 Series V2 and Competition (Test Conditions: V_{DC}=300 V, V_{CC}=15 V, f_{SW}=16.6 kHz, I_D=0.3 A_{rms}, T_A=25°C, SVPWM, Dead Time=2.6 μs, 124 W Fan Motor with Blade for Air Conditioner)

7. Handling Guide and Packing Information

7.1. Handling Precautions

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can adversely affect the packaging (by nullifying the effect of the antistatic agent). Place the devices in special conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them, or giving them uneven stress can cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes can cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or snowy day.

Storage

1. Avoid locations where devices might be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow.)
2. Do not place the device cartons upside down. Stack the cartons on top of one another in an uprighrt position only. Do not place cartons on their sides.
3. The storage area temperature should be maintained within a range of 5°C to 35°C, with humidity kept within the range from 40% to 75%.
4. Do not store devices in the presence of harmful (especially corrosive) gases or in dusty conditions.
5. Use storage areas with minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation, resulting in lead oxidation or corrosion, which degrades lead solderability.
6. When repacking devices, use antistatic containers. Unused devices should be stored less than one month.
7. Do not allow external forces or loads to be applied to the devices while they are in storage.

Environment

1. When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment.
2. Be aware of the risk of moisture absorption by the products after unpacking moisture-proof packaging.
3. Be sure that all equipment, jigs, and tools in the working area are grounded to earth.
4. Place a conductive mat over the floor of the work area or take other appropriate measures, so that the floor surface is grounded to earth and is protected against electrostatic electricity.
5. Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.
6. Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.
7. Install antistatic mats on storage shelf surfaces.
8. For transport and temporary storage of devices, use containers that are made of antistatic materials or materials that dissipate static electricity.
9. Make sure cart surfaces that come into contact with device packaging are made of materials that conduct static electricity and are grounded to the floor surface with a grounding chain.
10. Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).
11. Operators must wear a wrist strap grounded to earth through a resistor of about 1 MΩ.
12. If tweezers are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.
13. When storing device-mounted circuit boards, use a board container or bag protected against static charge. Keep them separated from each other and do not stack them directly on top of one another to prevent static charge / discharge due to friction.
14. Ensure that articles (such as clip boards) that are brought into static electricity control areas are constructed of antistatic materials as much as possible.
15. In cases where the human body comes into direct contact with a device, be sure finger cots or gloves protected against static electricity are worn at all times.

Electrical Shock

A device undergoing electrical measurement poses the danger of electrical shock. Do not touch the device unless sure that the power to the measuring instrument is off.

Circuit Board Coating

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas, or dust is present), circuit boards can be coated for protection. However, before doing so, carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size, board thickness, and the effects that components have on one another; makes it practically impossible to predict the thermal and mechanical stresses to which the semiconductor devices are subjected.

7.2. Packing Specifications

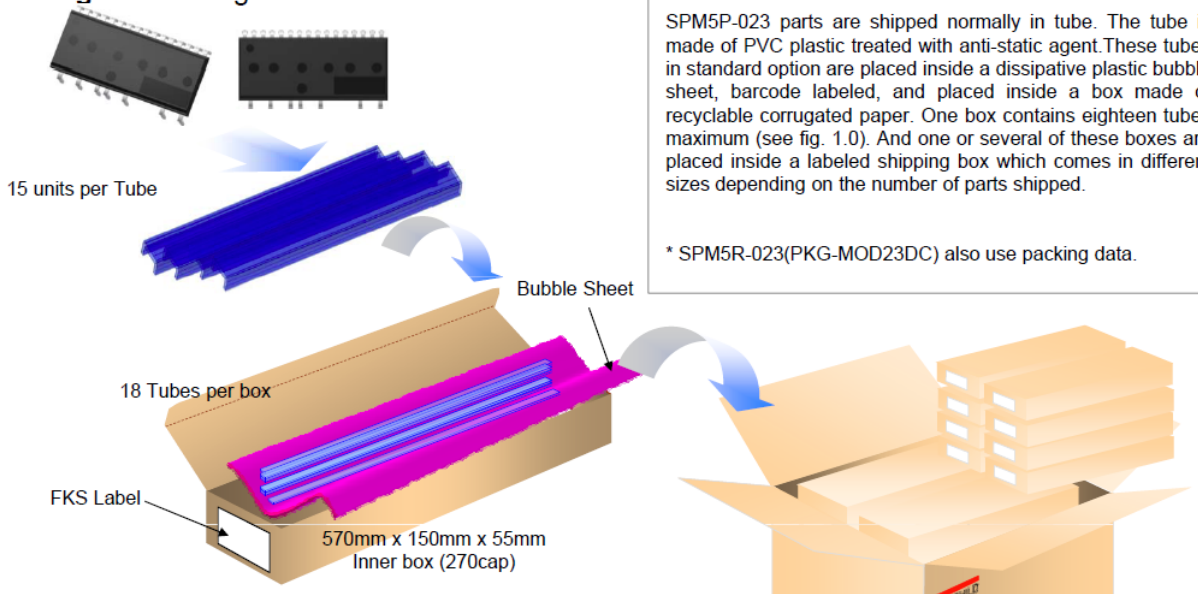
Motion SPM 5 Series products are normally shipped in tube. The SMD package is shipped in tape. More detailed information can be found in Figure 42 for DIP package, in Figure 43 and Figure 44 for SMD package, in Figure 45 for Double-DIP package, and in Figure 46 for Zigzag-DIP package. Please ignore internal package names shown in these figures.

SPM5P-023 Tube Packing Configuration: Figure 1.0

Packaging Description:

SPM5P-023 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains eighteen tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

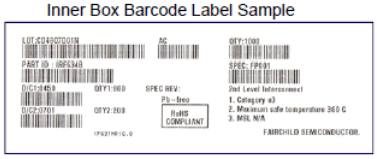
* SPM5R-023(PKG-MOD23DC) also use packing data.



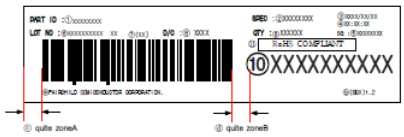
SPM5P-023 Packaging Configuration : Figure 2.0

SPM5P-023 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	15
Inner Box Dimension (mm)	570x150x55
Max qty per Box	270
Outer Box Dimension (mm)	590x330x245
Max qty per Box	2160
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

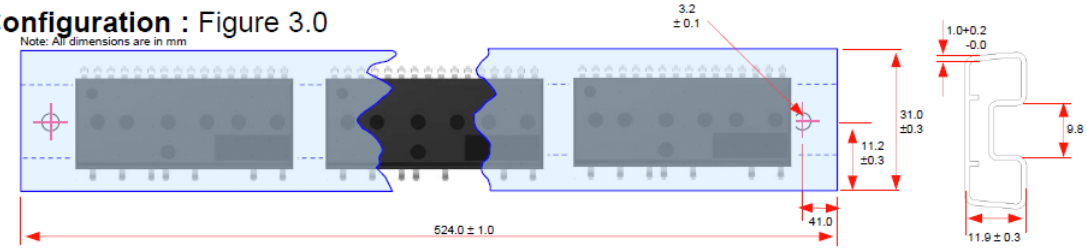


Outer Box Barcode Label Sample



SPM5P-023 Tube Configuration : Figure 3.0

Note: All dimensions are in mm



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD23DCREV2

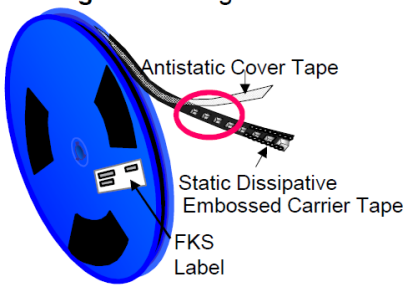
Figure 42. Packing Information for DIP Package

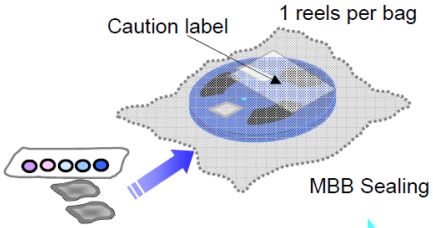
Packaging Description:

SPM5H-023 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multi-layer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 650units per 13" or 330mm diameter reel. The reels are dark blue or black in color and is made of polystyrene plastic (anti-static coated). This and some other options are further described in the Packaging Information table.These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

* SPM5Q-023(PKG-MOD23DG) also use packing data

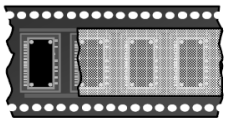
SPM5H-023 Packaging Configuration: Figure 1.0





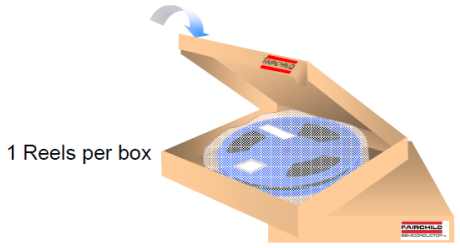
Inserting 2 Desiccants (2 x 25g) and Humidity Indicator Card

TM

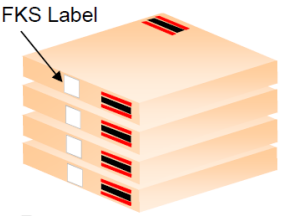


SPM5H-023 Packaging Information	
Packaging Option	Standard ™
Packaging type	TNR
Qty per Reel/Tube/Bag	450
Reel Size	13" Dia
Inner Box Dimension (mm)	339x352x68
Max qty per Box	450
Outer Box Dimension (mm)	390x370x310
Max qty per Box	1800
Weight per unit (gm)	
Weight per Reel(kg)	-
Note/Comments	

SPM5D-023 Unit Orientation

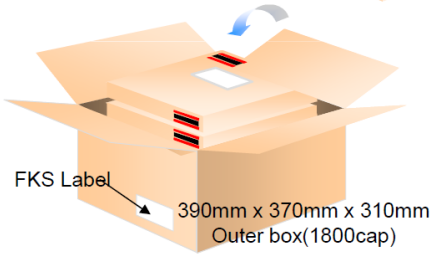


339mm x 352mm x 68mm
Inner box(450cap)



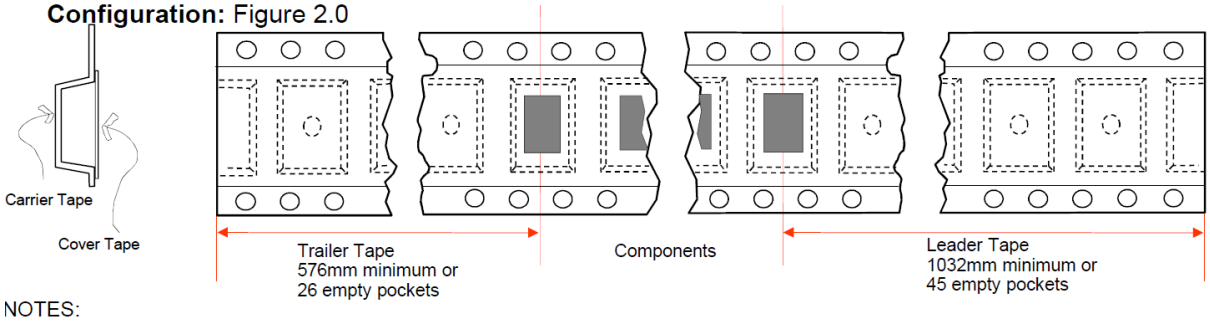
Inner Box Barcode Label Sample

Outer Box Barcode Label Sample



390mm x 370mm x 310mm
Outer box(1800cap)

SPM5H-023 Tape Leader and Trailer Configuration: Figure 2.0



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

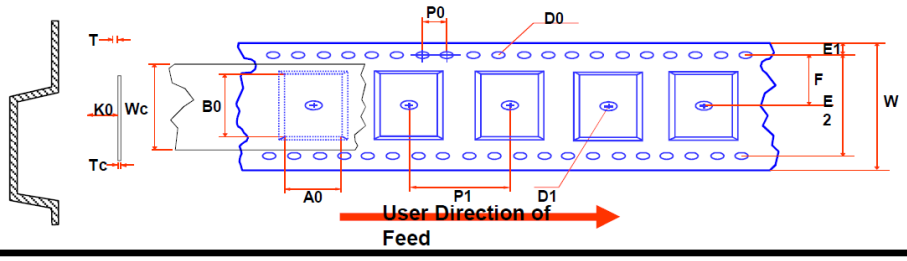
B : DRAWING FIEL NAME : PKG-MOD23DGREV1

Figure 43. Packing Information for SMD Package

SPM5H-023 Tape and Reel Data, continued

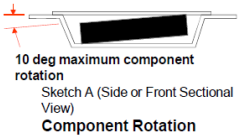
SPM5D-023 Embossed Carrier Tape

Configuration: Figure 3.0

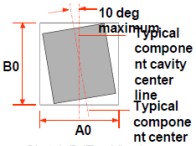


Dimensions are in millimeter														
PKG Type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SPM5D-023 TM (24mm)	17.20 +/-0.10	29.20 +/-0.10	44.0 +/-0.3	1.50 +0.10 /-0.00	2.00 min	1.75 +/-0.10	40.40 +/-0.10	20.20 +/-0.15	24.0 +/-0.1	4.0 +/-0.1	3.90 +/-0.10	0.30 +/-0.05	37.50 +/-0.1	0.06 max

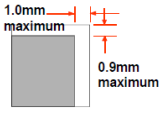
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



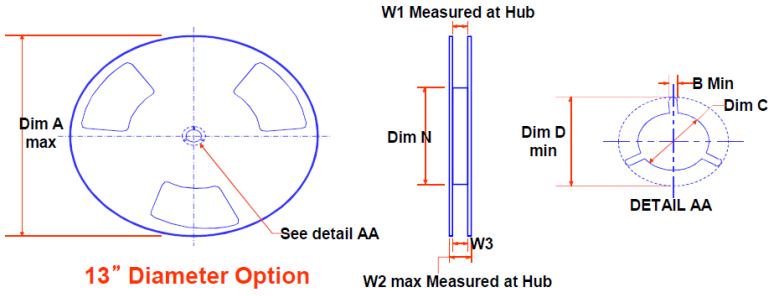
Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SPM5H-023 Reel

Configuration: Figure 4.0



13" Diameter Option

Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
44mm	13" Dia	13.00 330	0.059 1.5	0.512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	1.748 +0.079/-0.000 44.4 +2/0	1.984 50.4	1.866 – 1.728 47.4 – 43.9

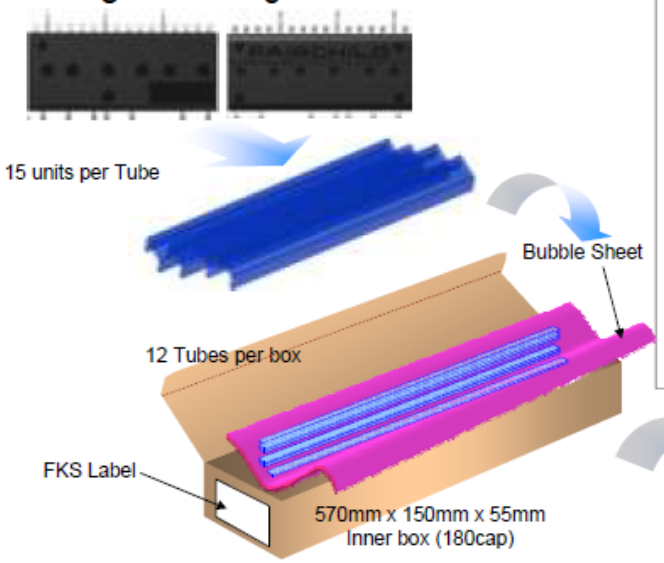
NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD23DGREV1

Figure 44. Packing Information for SMD Package (Continued)

SPM5G-023 Tube Packing Configuration: Figure 1.0

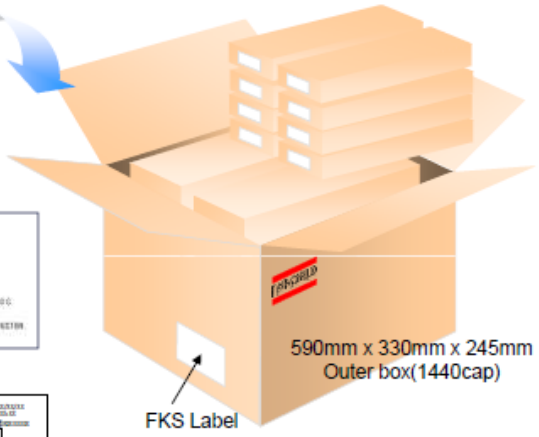


Packaging Description:

SPM5G-023 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains twelve tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

*

SPM5N-023(PKG-MOD23DF) also use packing data

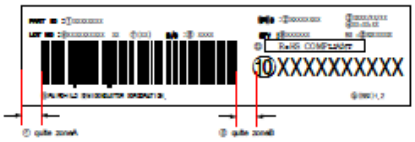


SPM5G-023 Packaging Configuration : Figure 2.0

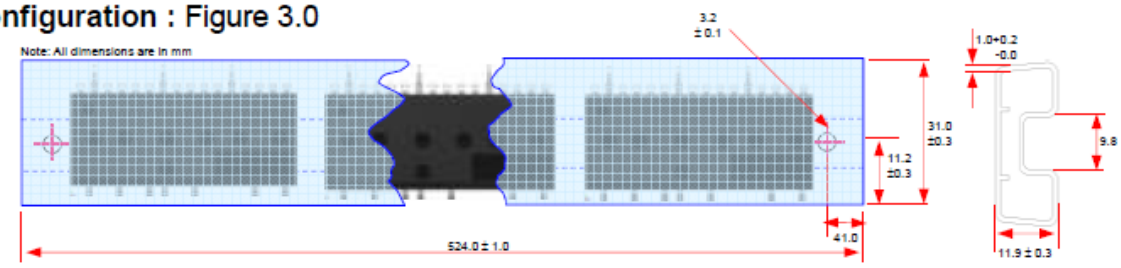
SPM5G-023 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	15
Inner Box Dimension (mm)	570x150x55
Max qty per Box	180
Outer Box Dimension (mm)	590x330x245
Max qty per Box	1440
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

Outer Box Barcode Label Sample



SPM5G-023Tube Configuration : Figure 3.0



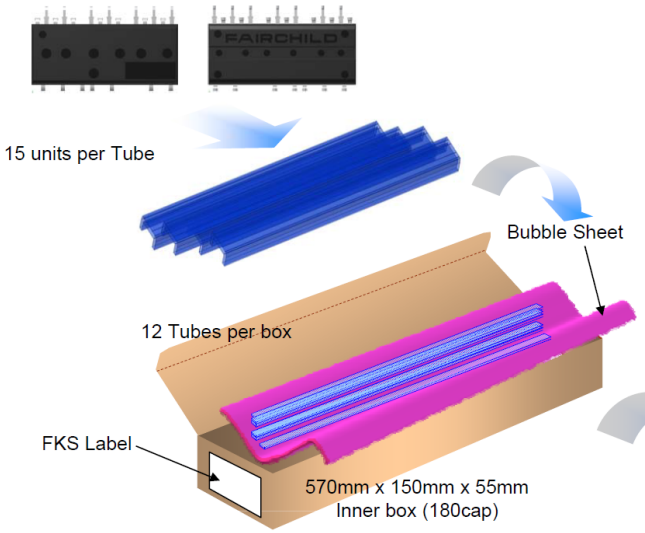
NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD23DFREV1

Figure 45. Packing Information for Double-DIP Package

SPM5T-021 Tube Packing Configuration: Figure 1.0



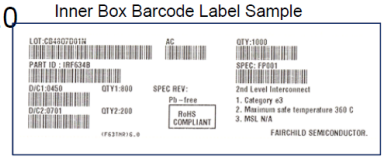
Packaging Description:

SPM5T-021 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains twelve tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

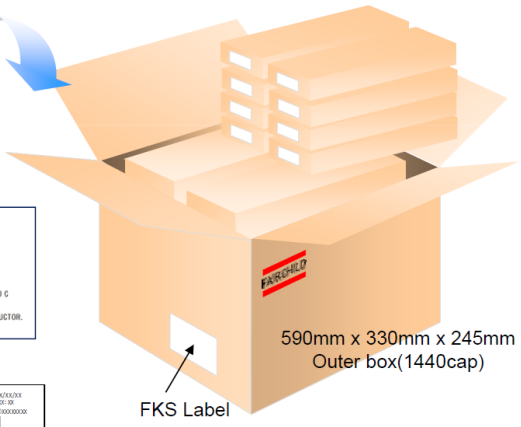
SPM5T-021 Packaging Configuration : Figure 2.0

SPM5T-023 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	15
Inner Box Dimension (mm)	570x150x55
Max qty per Box	180
Outer Box Dimension (mm)	590x330x245
Max qty per Box	1440
Weight per unit (gm)	-
Note/Comments	

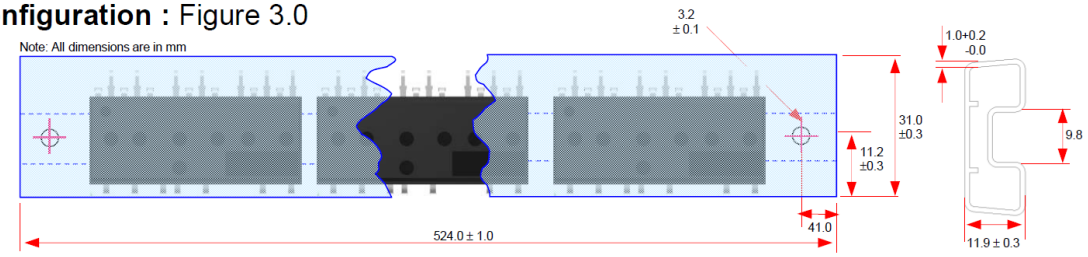
Inner Box Barcode Label Sample



Outer Box Barcode Label Sample



SPM5T-021 Tube Configuration : Figure 3.0



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD21DAREV2

Figure 46. Packing Information for Zigzag-DIP Package

8. Related Resources

AN-9760: PCB Design Guidance for SPM®

AN-9082: Motion SPM® 5 Series Thermal Performance Information by Contact Pressure

AN-9042: Motion SPM® 5 Series V1 User's Guide

RD-FSB50450A (Reference Design)

RD-402 FSB50760SF (Reference Design)

FSB50260SF(T) — Motion SPM® 5 SuperFET® Series

FSB50660SF(T) — Motion SPM® 5 SuperFET® Series

FSB50760SF(T) — Motion SPM® 5 SuperFET® Series

FSB50450AS — Motion SPM® 5 Series

FSB50825AS — Motion SPM® 5 Series

FSB50250A(T) — Motion SPM® 5 Series

FSB50250AS — Motion SPM® 5 Series

FSB50325A(T) — Motion SPM® 5 Series

FSB50450A — Motion SPM® 5 Series

FSB50550A(T) — Motion SPM® 5 Series

FSB50550AS — Motion SPM® 5 Series

SPM® Module Design Guide

Motion Control Design Tool

FCM8201 — 3-Phase Sinusoidal Brushless DC Motor Controller

FCM8202 — 3-Phase Sinusoidal Brushless DC Motor Controller

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative