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# Application Note AN-9056

## Using Fairchild Semiconductor Dual Cool™ MOSFETs

Dennis Lang

### INTRODUCTION

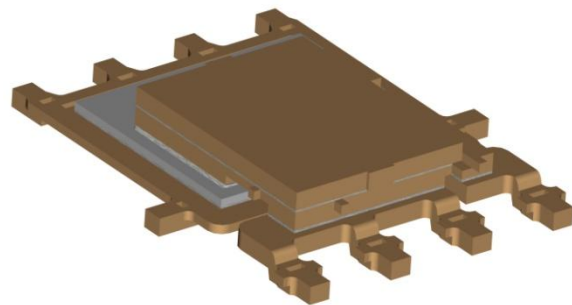
Pursuing a strategy of power density leadership, Fairchild Semiconductor has released a new power specific packaging technology, Dual Cool™, to meet the rigors of escalating demand for more improved thermal management in electronics designs. This technology creates a direct heat path from both the drain and source sides of the vertical MOSFET die structure through the addition of a heat slug to the top of the package. This structure allows for supplemental cooling on the top of the package with a heat sink system in addition to the direct conduction path in to the printed circuit board.

This application note will describe the package construction, address thermal characterization challenges and offer some systemic examples utilizing heat sinks.

### PACKAGE CONSTRUCTION

Dual Cool package construction is an evolutionary concept based on contemporary customer packaging form factor preferences, and incorporating new features to meet future performance expectations. The package design team chose to keep the very popular Power33 and Power56 lead geometries and pin outs allowing customers to add heat sinkable performance to existing PCB pad designs. Customers currently using a heat sink on the surface of a PowerQFN package will find this a very useful feature. Dual Cool uses 4 mils thin silicon as the core package design constraint. This represents half the thickness of the typical MOSFET which traditionally used 8 mils thick silicon dice. By reducing the die thickness to 4 mils, thermal and electrical performance are improved by reducing the parasitic resistance

created by the bulk resistance from the doped silicon area electrons flow through to get from the trench structure at the top of the wafer to the drain lead frame connection at the bottom. The top and bottom surfaces of the die are plated with solderable metal to permit solder attachment of the drain lead frame on the bottom, and the source and gate clips on the top. To improve the heat transfer path from the die to the top of the package for use with a heat sink, a heat slug is soldered to the source clip and exposed on the top of the package to interface with a heat sink.



**Figure 1: Solid model illustrating Dual Cool package construction.**

Solder attachment of the silicon to the lead frames, with optimized copper clips additionally reduces electrical and thermal parasitics. The  $\Theta_{JC}$ , that is, the thermal resistance from the junction to the case has two important values with this package type, the junction to case thermal resistance to the drain tab as well as the top heat slug. The datasheet offers these values for each specific product type. These numbers are a measure of the two efficient heat paths out of the component, giving the designer options for

managing the heat loads created by high power density for designs.

## CHALLENGE FOR BOARD DESIGNERS

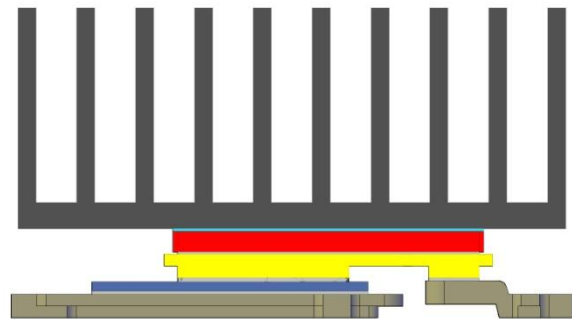
The majority of consumer electronics designers use FR-4 board material for their designs. FR-4 employs a resin system that has a glass transition temperature (Tg) typically in the range of 115-125°C. This is the lowest Tg material in most consumer electronics products, thus setting the limit for temperatures in operation. Reaching the glass transition temperature can see a radical transition of FR-4 material properties, including a four-fold increase in the out of plane (or Z-axis) coefficient of thermal expansion (CTE). The exponential increase in CTE results in multiplied stresses on board to component solder joints, and plated through holes in the PCB. High aspect ratio plated through holes, relatively small holes to large board thicknesses, lead to boards that are particularly sensitive to temperature excursions above Tg. To avoid this scenario many designers strive to limit their board temperatures at 100°C, creating safety factor in the design. With the long term reliability of their products directly related to thermal management, designers need effective tools to characterize their designs.

## TEST METHODOLOGY

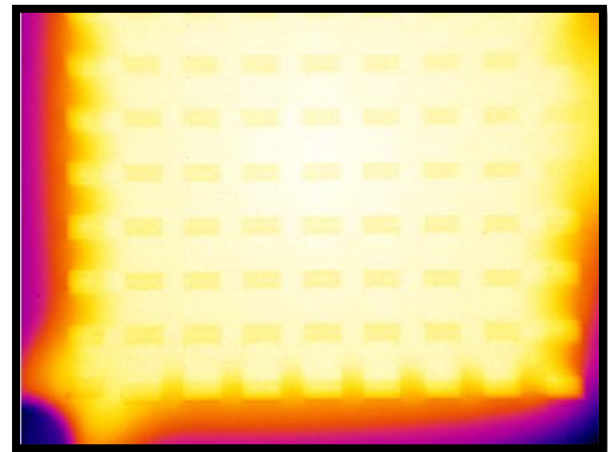
This device presents a challenge for thermal characterization on an end user's board. An increasingly popular way for power designers to characterize their designs is using infrared thermographs. This technique works well with normal PowerQFN devices as the plastic mold compound is semi-transparent to infrared, presents a relatively consistent case emissivity of approximately 0.92, and with thin ( $\leq 1.0\text{mm}$ ) plastic molded components, the camera often yields temperatures within 5-10% of junction temperature. By allowing for the particulars of using an infrared camera, the designer can quickly and precisely determine the important

temperatures in a system without a heat sink during design optimization and verification. When power packages of any kind are used with a heat sink, a challenge is presented to the

engineer or technician who would opt to use this method. The heat sink is not transparent to infrared, preventing the camera from capturing accurate temperatures of the device junction.



**Figure 2: Cross section of Dual Cool and heat sink assembly.**



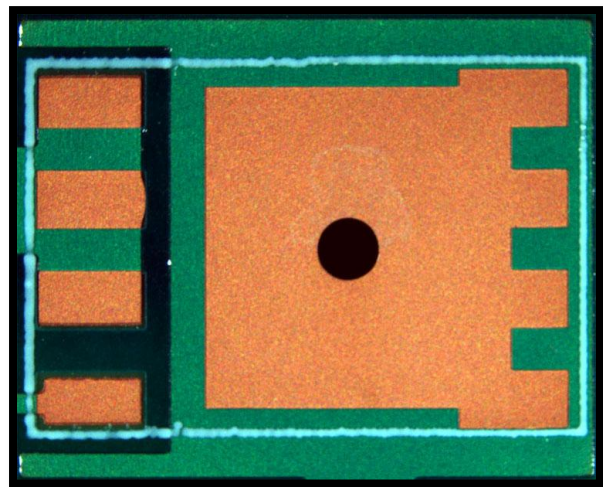
**Figure 3: Thermograph of Dual Cool with heat sink in operation.**

To measure the temperature of various devices under test, a method for attaching a thermocouple to the drain pad was devised. This method should be as close to the die as possible to assure that surrounding components, airflow, and other factors do not affect thermocouple readings. Attempts to correlate temperature to a

location on the surface copper layer near the component proved untenable. Heat transfer is a non-linear function over distance and varying load and environmental conditions may render a correlation incorrect over the range of use conditions the board is characterized across. To address these concerns, it is desirable to locate the thermocouple as near the silicon die as possible.

An unplated via can be drilled in the drain pad of verification boards for insertion of a thermocouple to touch the drain lead of the device. This via should not be plated, otherwise, during SMT processing, solder will wick down the copper and foul the opening for the thermocouple. The via should be kept as small as possible, but be large enough to use the thermocouple size desired. The boards used in this experiment had a 28 mils diameter hole drilled. The boards designed for this study were all single layer. If the board to be tested is multilayer, it is a good idea to create a keep out in the copper planes of all layers for the drilled hole to assure there is no shorting of layers through the thermocouple wire.

As the Dual Cool package was designed to duplicate the industry standard PCB pad for 3.3x3.3mm and 5x6mm PowerQFNs, the same footprint and PCB design was used to directly compare wire bonded, clip bonded and Dual Cool products at thermal steady state. The board was constructed of lead free rated, 62 mils thick FR-4 material.



**Figure 4: Power56 PCB pad with unplated hole for thermocouple.**

It may occur to the designer that this hole could reduce thermal or electrical performance. As up to 25% voiding is acceptable in the device this was not considered a problematic concern for a

verification board. Of more concern is the ability of the thermocouple wires to act as a heat sink

and remove enough heat from the board to under-predict temperatures during operation in the end application. This leads to the first reported experiment, attempting to address the question, can larger thermocouples change the results of the experiment?

## **DEVICES CHOSEN FOR ALL EXPERIMENTS**

The devices used in this experiment were meant to be as similar as possible, to make the differences in thermal performance attributable to the package technologies exclusively. Compared in this paper will be components with traditional bond wires used to make the gate and source connections, a clip-bonded product, using soldered copper clips to make the gate and source connections, and the Dual Cool package described in detail previously. All three components used employ 4 mil thick die. The die used in the chosen Dual Cool and clip

bonded parts are the exact same die, there are no differences. The die used for the wirebonded part was approximately half the area of the Dual Cool and clip. This part was chosen as the largest die available with the 4 mil thickness and employing wire bonding. It is not an ideal comparison, but in previous steady state thermal testing it has been found for wirebonded parts that die size does not make for dramatic differences. The trends in the data are comparable and representative of differences as seen in applications.

### THERMOCOUPLE SIZE EXPERIMENT

Early data taken using a thermocouple attached to the drain pad seemed to be better than expected. Infrared thermographs from the thermal camera were found not to match the temperatures seen at the thermocouple, even accounting for the junction to case thermal resistance. It was realized that the

thermocouple itself, in certain use conditions, actually could act as a heat sink. There is also the concern of the thermocouple not being properly attached to the board, and not touching the back of the device, and this should always be carefully checked. The intrinsic diode of the MOSFET was used to heat the device for testing. To test if the thermocouple was a factor, a worst case scenario was chosen, "minimum pad" quantity of 2 ounce thick copper on the test coupon, and no airflow. The devices were tested using 36 gauge K-type thermocouples,

the same units were then



**Figure 5: A 36 gauge thermocouple with polyimide tape as suggested for testing.**

retested with 28 gauge thermocouples. To set the power levels units were tested with 36 gauge thermocouples, and current was increased until the thermocouple read approximately 100C. The current level was maintained for the retest with the larger thermocouple.

### RESULTS

All three device types were tested with the two sizes of thermocouple. The wire bonded Power56 was found to have a 10% lower  $\Theta_{JA}$  with the 28 gauge thermocouple than the 36 gauge thermocouple. The clip bonded and Dual Cool components were found to run about 5% cooler with the larger thermocouple. The data

suggests it is important to use a smaller thermocouple for these types of data gathering, and a 36 gauge thermocouple is recommended due to having less impact on the data, as well as allowing for a smaller hole to be drilled in the pad for interfacing the thermocouple with the drain pad. All subsequent data was collected using 36 gauge thermocouples.

### THERMAL PERFORMANCE WITHOUT A HEAT SINK EXPERIMENT



With initial experiments optimizing data taking, thermal comparisons over a range of factors were conducted to determine the benefits of the various interconnect technologies when used in different applications. The devices in all runs were mounted in the vertical position inside a wind tunnel. The mounted components all had a thin layer of Krylon® high temperature black spray paint applied to ensure a constant emissivity for the infrared camera. Ambient temperature inside the laboratory was measured to be 21.4°C. The first data was taken on the units without a heat sink. The boards were constructed using 2 ounce copper, in two areas. There were boards constructed with a “minimum pad” which represented a pad 5x7mm, or approximately the minimum outline necessary for the footprint for soldering the component to the PCB. The second copper layout used 1in<sup>2</sup> of copper area, the majority connected to the drain. This represents a common thermal board used in characterizing MOSFETs by many vendors. Runs were also completed with and without airflow. The airflow chosen was 200 feet per minute (FPM) as measured by a hot wire anemometer near the device under test (DUT). This was a full factorial experiment, all possible combinations with the three device types, the different board types and with and without airflow. All devices were tested by using the intrinsic diode of the MOSFET to heat the die, and the current adjusted until the thermocouple measured approximately 100°C. All testing was performed at steady state.

## RESULTS

On the minimum pad without airflow, it was found that no part performed significantly better. On the minimum pad with 200 FPM of airflow, the results did start to change. The wire bonded and clip bonded components did perform the same, but the Dual Cool performed slightly better, with a junction to ambient thermal resistance approximately 7% lower. Testing the

three components on 1 in<sup>2</sup> of PCB copper without airflow yielded the same result as the minimum pad, no appreciable difference between the three package types. The airflow was set to 200 FPM and the three 1in<sup>2</sup> boards tested again. The result was the same, with airflow, all 3 devices performed similarly.

## DISCUSSION

There were no unexpected results in this test. Without a heat sink, the prime heat transfer mechanism is through the drain pad into the PCB. The three component types are similar. The one difference noted was the Dual Cool on minimum pad with airflow, performing demonstrably better. With the minimum pad the component covers the majority of the copper on the PCB, and the heat transfer to forced convection airflow comes from the package surfaces and the small amount of heat transferred through the fibers and resin of the FR-4. In this thermally inefficient system, the airflow across the copper drain tab on the surface of the Dual Cool component delivers an improvement in performance. To put this improvement in perspective, limiting the board temperature to 100°C, the wire bonded part 1.41W could be dissipated in operation. The improvement in the Dual Cool would allow for 1.51W to be dissipated to reach 100°C.

## THERMAL TESTING WITH HEAT SINK EXPERIMENT

Next is testing conditions with a heat sink. As the *raison d'être* for Dual Cool, this group of tests should show significant differences. Tests

were performed using the same boards and units employed in testing without a heat sink. All combinations with minimum and 1in<sup>2</sup> copper coverage, with and without 200 FPM of airflow were tested. Aavid Thermalloy part number 10-6327-01 was chosen for the heat sink in these

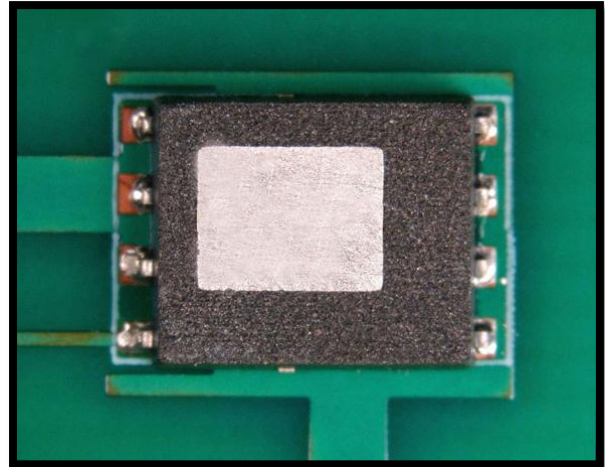
runs. This heat sink uses push-pin style attachment, and measures 28.5x28.5mm square and 10.0mm high. A thermal pad or grease should always be used for best performance. It is not recommended to use Dual Cool without some type of thermal interface material. Using grease or a thermal pad makes the connection of the heat sink to the component more efficient. Surface irregularities make mounting a heat sink without an interface material an inefficient system. The heat slug on top of the Dual Cool package is an active source. If the application is switching, or there is concern with coupling to the heat sink, an interface material that is an electrical isolator should be chosen. If electrical isolation is not a concern, there is interface materials loaded with conductive materials such as metals or carbon that provide a significantly better conductive heat transfer path due to typically lower thermal resistivities of conductive materials.

All combinations tested here used Bergquist's 20 mils thick GP1500 Gap Pad®. This pad isolates the heat sink from the exposed heat slug on the Dual Cool, which is active source area. In switching applications it is advisable to isolate the heat sink from this area due to EMI considerations.

## RESULTS

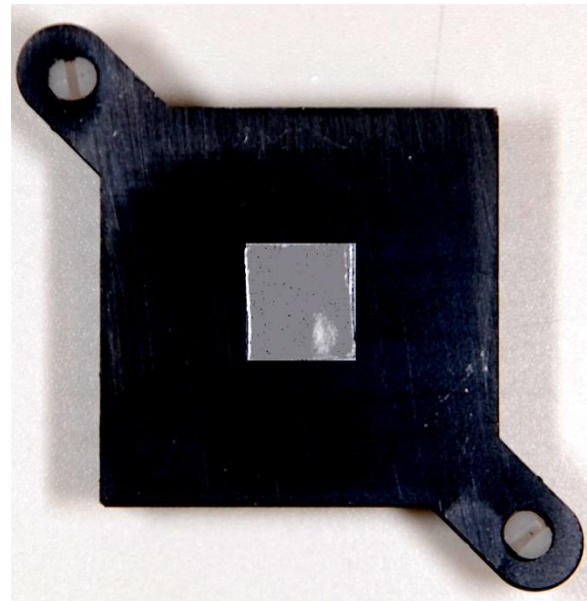
The first combination tested, minimum pad, no air flow showed the strong performance of Dual Cool. The clip bonded FDMS7650 showed a 9% improvement from the wire bonded component,

but the Dual Cool showed a 35% improvement in junction to ambient thermal resistance over the wire bonded component.



**Figure 6: Power 56 Dual Cool with top-side metal heat slug.**

Next the combination of 1 in<sup>2</sup> copper, with heat sink and no airflow was tested. This combination showed no meaningful difference between the three combinations. Next up was



**Figure 7: Heat sink with thermal interface pad applied.**

the most striking test, the minimum pad with 200 FPM of airflow. The clip bonded component performed 19% better than the wire bonded,

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however, the Dual Cool was 57% better than the wire bonded component. Testing with 1 in<sup>2</sup> of copper, the clip bonded component was 13% improved over the wire bonded, and the Dual Cool was 29% improved over the wire bonded.

### DISCUSSION

This testing showed the real benefits of the improved heat conduction path through the copper slug in the top of the package to the heat sink. With a minimum pad and no airflow, the theoretical power dissipation capability rises from 2.59W with the wire bonded component, to 3.5W with the Dual Cool. The 1 in<sup>2</sup> run with no airflow might have been a surprising result. As mentioned previously, all units were mounted vertically, where the buoyancy effects allow natural convection to improve heat transfer from the 1 in<sup>2</sup> copper area to the ambient air. It is believed if this test was repeated with the component parallel to the floor, or possibly a different heat sink, there would have been a larger difference favoring Dual Cool as in the other conditions. The largest difference in the testing was predictably found with the minimum pad, heat sink and 200 FPM airflow combination. The wire bonded component could dissipate 3.7W, where the Dual Cool could dissipate 5.8W, nearly 57% more power, while maintaining the board at 100°C. With a 1 in<sup>2</sup> pad and 200 FPM of airflow, the clip bonded component was 13% improved over wire bonded, and Dual Cool was 26% superior to the wire bonded component.

### THERMAL GREASE REPLACES GAP PAD® EXPERIMENT

There is a group of computer builders that attempt to improve the thermal performance of the heat sinks used on processors and memory chips by replacing the pad used to interface with the heat sink with thermal grease. It was

decided to test if using a thermal grease product favored among "overclockers", performance

could be improved. Antec® Silver Thermal Compound replaced the Gap Pad® and the experiment with the minimum pad, heat sink and 200 FPM was repeated. This combination proved to be most sensitive to the thermal path through the heat sink, leading to its selection.

### DISCUSSION

The thermal grease provided an across the board improvement over the Gap Pad®. It was found for the wire bonded units that performance improved 10% over the gap pad, for the clip bonded 12%, and for Dual Cool performance improved 21% over the Gap Pad®. This would represent a theoretical improvement in allowable dissipated power from 5.8W with the gap pad to 7.0W with the grease. For best performance the grease is the best, but grease is more difficult to dispense, rework and does not have the electrical isolation properties of the pad. The application will deem if these trade-offs are worth making.

### LARGE HEAT SINK EXPERIMENT

For the final test, a larger heat sink was applied to the minimum pad units. The heat sink chosen was Aavid Thermalloy part number 10-L4LB-03. This heat sink measures approximately 41.4x45x11.7mm, more than doubling the area. 200 FPM of airflow was applied to the units and data taken. The improvement was relatively consistent across the three package types, with a 10% performance improvement over the same heat sink tested with the same power and ambient conditions.

### USING TOP SIDE COPPER PAD AS AN ELECTRICAL CONNECTION

Engineers will always find creative ways to use products which the original product designers do not anticipate. Dual Cool will be no different! As the top heat slug is active source area metal, designers may desire to solder to this pad. The



plating chemistry of the thermal pad matches that of the leads, pure tin plating. However, this lead does not receive JESD22-B102 Solderability Testing to guarantee solderability. Thus at this time Fairchild Semiconductor cannot guarantee solder joint performance to this pad. Should the designer have an application which may require soldering to the heat slug, it is recommended they contact Fairchild Semiconductor for applications engineering support.

### RELIABILITY WITH HEAT SINK

As a package designed for use with a heat sink, Dual Cool was designed for reliability with a heat sink assembly attached to the package. Part of the package qualification requirements for Dual Cool was to pass with no failures board level temperature cycling to IPC-9701 conditions employing a heat sink and interface material applied to the package. The user of Dual Cool can be confident that applying a heat sink attachment system that applies forces as recommended for common thermal interface materials on the market will not cause damage to Dual Cool.

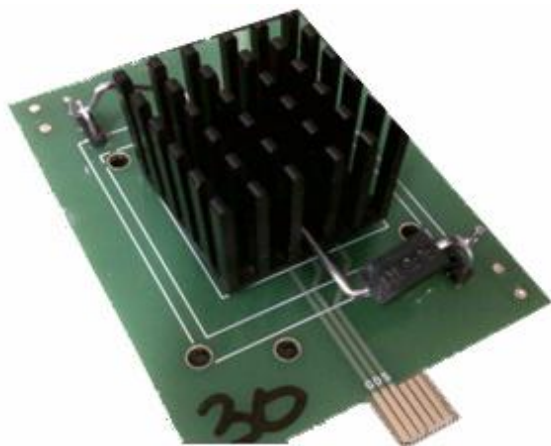


Figure 8: Dual Cool board level temperature cycling test coupon.

The Dual Cool package was introduced and the key elements of the package design demonstrated. A method for determining temperature in the application was shown. The varied performance of the three package types was reported, which should give the designer the information necessary to choose the technology that meets their performance and price tradeoff.

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### CONCLUSION



*Applicable FSIDs: FDMC2512SDC, FDMC2514SDC, FDMC3011SDC, FDMC3020DC, FDMC7658SDC, FDMC7660DC, FDMS2502SDC, FDMS2504SDC, FDMS2506SDC, FDMS2508SDC, FDMS2510SDC, FDMS3016DC, and FDMS7650DC.*

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