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AN-9045
WLCSP Assembly Guidelines

Introduction

Wafer-Level Chip-Scale Packaging (WLCSP) is actually an older packaging technology, likely the oldest finding significant growth today. The technology is valued for the same reasons it was originally designed: a comparatively small Printed Wiring Board (PWB) footprint with great package parasitic performance and relative ease of assembly. WLCSP assembly performance may require different non-destructive test tools for inspection in production; an optimized board-mount process gives the largest process window in volume production, ultimately yielding the best performance.

Purpose

This application note provides a recommended starting point for manufacturing process optimization using Fairchild Semiconductor WLCSP components. The suggestions published here have been shown to work under the given conditions, but variances in manufacturing equipment, processes, and circuit board design may lead to a combination where other parameters yield superior performance.

Manufacturing Considerations

Board Mounting

The solder joint and pad design are the most important factors in creating a reliable assembly. The pad must be designed to the proper dimensions to allow for tolerances in PWB fabrication, pick and place, and to allow for proper solder fillet formation where applicable.

Pad Finish

The most frequently encountered pad finish for consumer electronics with tin lead solders was Hot Air Solder Leveled, (HASL). With lead free, other finishes are preferred. Immersion silver, immersion nickel gold, and Organic Surface Protectant (OSP) are the board finishes of choice. Each finish has useful properties and each has its challenges. It is beyond the scope of this paper to debate each system's merits. Not any one finish is right for all applications, but the most commonly seen in large scale consumer electronics is OSP currently. A high-quality OSP, like Enthone® Ente® Plus HT, is recommended.

PWB Material

It is recommended that lead-free FR-4 be used in PWB construction. Lower-quality FR-4 can cause numerous problems with the reflow temperatures seen when using lead-free solder. IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" contains further information on choosing the correct PWB material for the intended application.

Experimental Procedure

The study that led to the recommendations in this paper for four of the most critical processing parameters are not be described in detail, but a brief description of the methodology is presented. Four factors were studied to determine a baseline of recommendations for mounting Fairchild Semiconductor WLCSP with 500 µm pitch and 300 µm diameter lead-free solder bumps. There is not a suggestion for one type of process.

Various customer and industry specifications result in WLCSP being used with many different processes. Using six-sigma based techniques and JMP® software, the interrelated effects of the factors are captured and used to define the best process for certain customer requirements.

The four factors are whether the pad is Solder Mask Defined (SMD) or non-solder mask defined (NSMD, also sometimes known as "copper defined"), pad diameter, solder stencil opening and via in pad, or no via in pad. Each factor is discussed below and a summary of recommendations is provided in the appendix.

SMD / NSMD Pads

SMD pads are exactly as the name implies; pad defined by the solder mask on the board. The opening of the solder mask is smaller than the underlying copper area for soldering to the associated bump. A NSMD pad has a solder mask opening larger than the copper pad. There are many factors influencing whether the PWB designer uses SMD or NSMD pads. Due to external influences, the designer may be forced to use one type or the other. Either type can be successfully used with WLCSP packages, but each has characteristics worth noting.

NSMD pads are perhaps more commonly recommended in literature. NSMD pads have two key advantages; solder may wet down the side of the copper pad, theoretically enhancing the solder joint-PWB bond, and copper etching is

a more precise process than solder mask at the board construction level. There are no free lunches, however. NSMD pads have less copper on the board and are therefore more prone to damage during rework. This study found that NSMD pads also had higher incidences of voiding and shorting in manufacturing than SMD pads. If NSMD pads are chosen, the opening between the pad and solder mask should have at least 50 µm clearance. The trace width of interconnections between pads should be no more than 60% the diameter of the pad. The trace should have a fillet radius at the point where it meets the pad, known as "tear dropping," to prevent the stress riser that would otherwise occur at the pad-trace intersection.

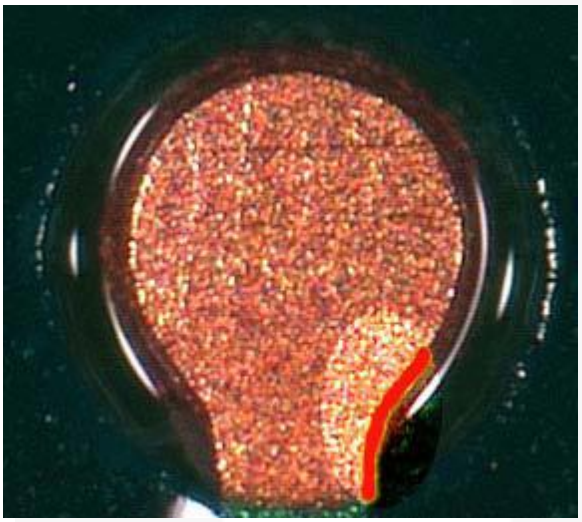

Figure 1. NSMD Pad with "Tear Drop" Radius Highlighted

SMD pads have copper areas larger than the pad and are defined by the opening in the solder mask. SMD pads have been found to have better void and short performance in reflow than NSMD pads. SMD pads also typically withstand the stresses of rework better than NSMD pads. The main downsides of SMD pads are being defined by the solder mask, which is a typically a less accurate process than the copper layer. Also, SMD pads also have less area for solder to wet to at the bump-PWB interface. However, with lead-free solders, the long-term failure mechanism (as seen in temperature cycling tests) is typically cracking at the die-bump intermetallic interface, so this may not have an effect on long-term reliability.

Pad Diameter

Pad diameter is a factor that may be determined for the board designer by corporate standards. If the board designer has the freedom to choose pad diameter, s/he may find different diameters recommended, ranging from 200-300 µm. This is due to the long history of WLCSP packages and a multitude of standards regarding their use. This note addresses pads with diameters of 250, 275, and 300 µm. With lead-free solders, engineers have found the need to reduce stress at the die-bump interface. A method of more evenly distributing the stress is to reduce the size of the PWB pad to match (or be close to) the diameter of the die under bump metal, to which the lead-free bump is attached. It has become more common to see a recommendation of 250 µm diameter pads for 300 µm bumps, which is what Fairchild Semiconductor recommends on datasheets.

Stencil Aperture

Stencil apertures are defined by the size and shape of the holes cut into the stencil used in screen printing. Fine pitch components work best with 4 mil-thick stencils and that was used here for all trials in this study. All openings are square in shape, laser cut into stainless steel, and polished. This gives better paste release than round apertures. It was found that a slight overprint of solder would yield superior voiding performance in reflow with most pad types. However, overprinting solder also increases the likelihood of shorting. It is recommended to print at 1:1 or slightly overprint as recommended in the summary chart, depending on what the process engineer is trying to optimize.

VIA In Pad

The need for via in pad is determined by the design. There are many reasons to avoid via in pad if possible, chiefly voiding / inconsistency of solder joints after reflow and the introduction of more failure points in the PWB. If the designer must use via in pad, it is recommended to drill small vias, allowing them to be plated solid if possible. With any via-in-pad PWB, the quality of the vendor making the board is more important. Via in pad create significant voiding in the solder joints. The typical void is the via diameter to a depth of approximately 1/3 the bump height.

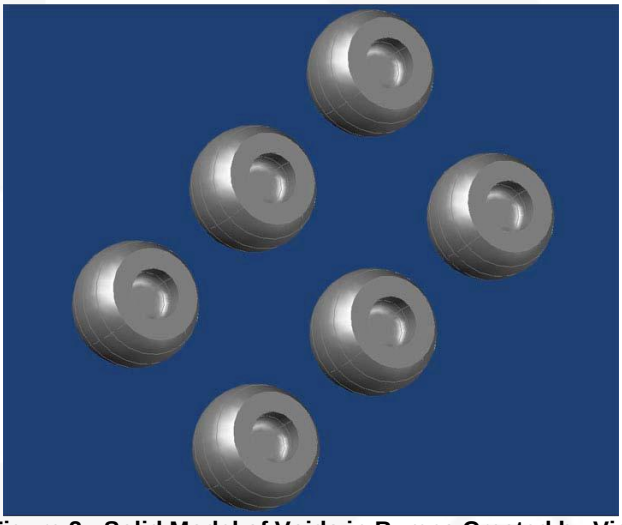

Figure 2. Solid Model of Voids in Bumps Created by Via in Pad Board Design

Finite element analysis was used to simulate the effects of this void and no increase in stress at the critical die-bump interface was found.

Solder Paste

The WLCSP is a RoHS compliant and lead free package. Any standard lead-free no-clean solder paste, made with type-3 or type-4 powder commonly used in the industry, should work with this package. The IPC Solder Products Value Council has recommended that the lead-free alloy, 96.5 Sn/3.0 Ag/0.5 Cu, known as SAC 305, is the lead-free

solder paste alloy of choice for the electronics industry. Type-3, no-clean paste, SAC 305 alloy, was used for construction of the boards studied to optimize the process.

Reflow Profile

The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor. Obtaining this information from the paste vendor is strongly recommended. If using a KIC® profiler, downloading the latest paste library from KIC® yields ramp rate and soak times at temperatures for most commonly used solder pastes. Fairchild WLCSP packages are rated for 260ºC peak temperature reflow. The appendix includes a reflow profile example. This profile is provided for reference only; different PWBs, ovens, and pastes change this profile, perhaps dramatically.

Inspection

WLCSP requires different equipment for inspection after reflow than many other surface-mount technology components. WLCSP alignment can be inspected in production by checking alignment with a boarder printed on the stencil layer of the PWB. Inspection of the solder joints for shorts and voiding is more challenging. There are two methods: side-looking cameras using technology to look under the die to allow an operator to inspect the bumps; and, more commonly, x-ray. The industry standard for voiding is currently 25% distributed throughout the solder joint.

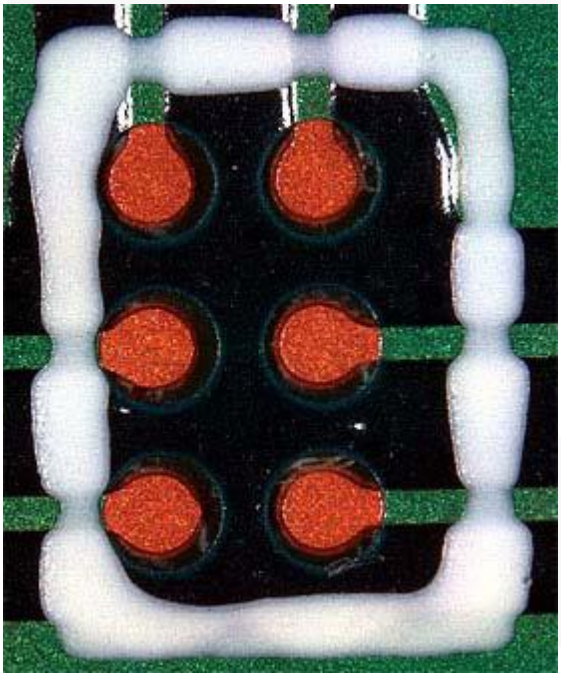

Figure 3. Printed Boarder on PWB for Visual Confirmation of WLCSP Alignment

Rework

Due to the high temperatures associated with lead-free reflow, it is recommended that this component not be reused if rework becomes necessary. The WLCSP should be removed from the PWB with hot air. After removal, the WLCSP should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick, the pads cleaned. and new paste printed with a mini stencil. A WLCSP rework station should be used to align and place the replacement WLCSP. This machine typically has a programmable reflow profile using hot air to reflow the solder and make the joint.

Board-Level Reliability

As part of the standard reliability testing, this package was temperature cycled from -10 to 100°C for the study. There could be no failures in the sample set at 1000 cycles to pass the test. Extended testing was successfully completed with various industry-standard drop and bend tests commonly required for portable electronic devices. For information on these studies, contact Fairchild Semiconductor.

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