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FSA642 — Evaluation Board User Guide

1. Introduction

This user guide is for the FSA642 evaluation board and is intended to complement the FSA642 datasheet. Technical or application-specific questions not addressed in this guide should be directed to Fairchild’s technical support team. Please contact your Fairchild representative, visit our website at www.fairchildsemi.com, or contact us at analogswitch@fairchildsemi.com.

This evaluation board is used to evaluate the high-speed performance of Fairchild’s differential 3PDT MIPI switch. SMA connectors are used for maintaining signal integrity of input and output signals. The board is designed to pass differential clock or data signals without the use of on-board loads or terminations. Clock and data trace pairs are designed for 100Ω differential impedance. For lab evaluation, a standard 50Ω pulse/data generator can supply signals into the inputs and 50Ω terminated, high-bandwidth oscilloscope sampling heads can be used to terminate the outputs.

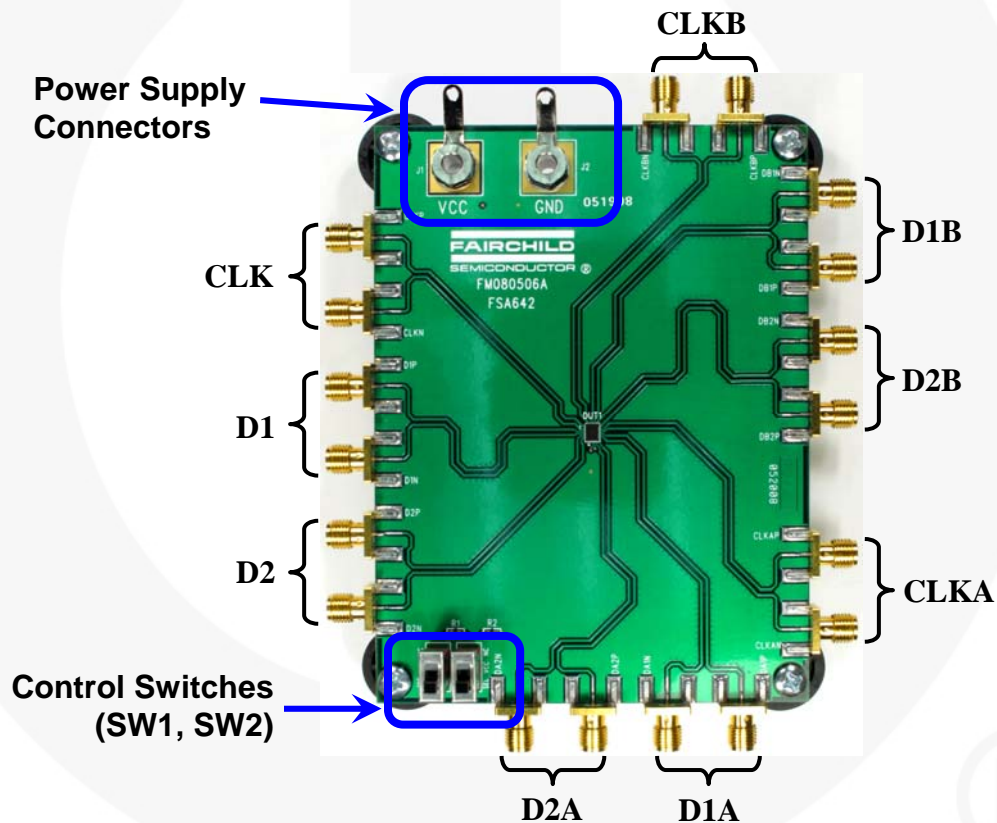


Figure 1. Evaluation Board with Component Locations Labeled

Configuration of the device is simplified by on-board switches to enable/disable the device and to control the output select manually. Signal trace layout follows the UMLP package pad layout, with clock/data inputs at the left and multiplexed outputs at top, right and bottom.

2. Getting Started

To begin using this evaluation board, perform the following steps:

1. Configure the on-board control pin switches in the desired state (*see Table 1*).
2. Connect signal cables or 50-Ω terminated scope cables to SMA connectors.
3. Apply power to the board at the power supply connectors.






Note: Per the datasheet, the recommended V_{CC} operation range is 2.65V to 4.3V.

4. Enable input signals.

3. Control Pin Configuration

This FSA642 evaluation board has two mechanical SPDT switches located at the bottom left corner. These configure the output enable (/OE) and output switch selection (SEL) functions of the FSA642. Table 1 lists the position of the mechanical switches and the corresponding functional states for the control inputs.

Table 1. Control Pin Configurations

SW1 (/OE)	SW2 (SEL)	FSA642 Switch Function
	n/a	Inputs disconnected from outputs
		CLK, D1, D2 differential pairs connected to CLKA, D1A, D2A
		CLK, D1, D2 differential pairs connected to CLKB, D1B, D2B

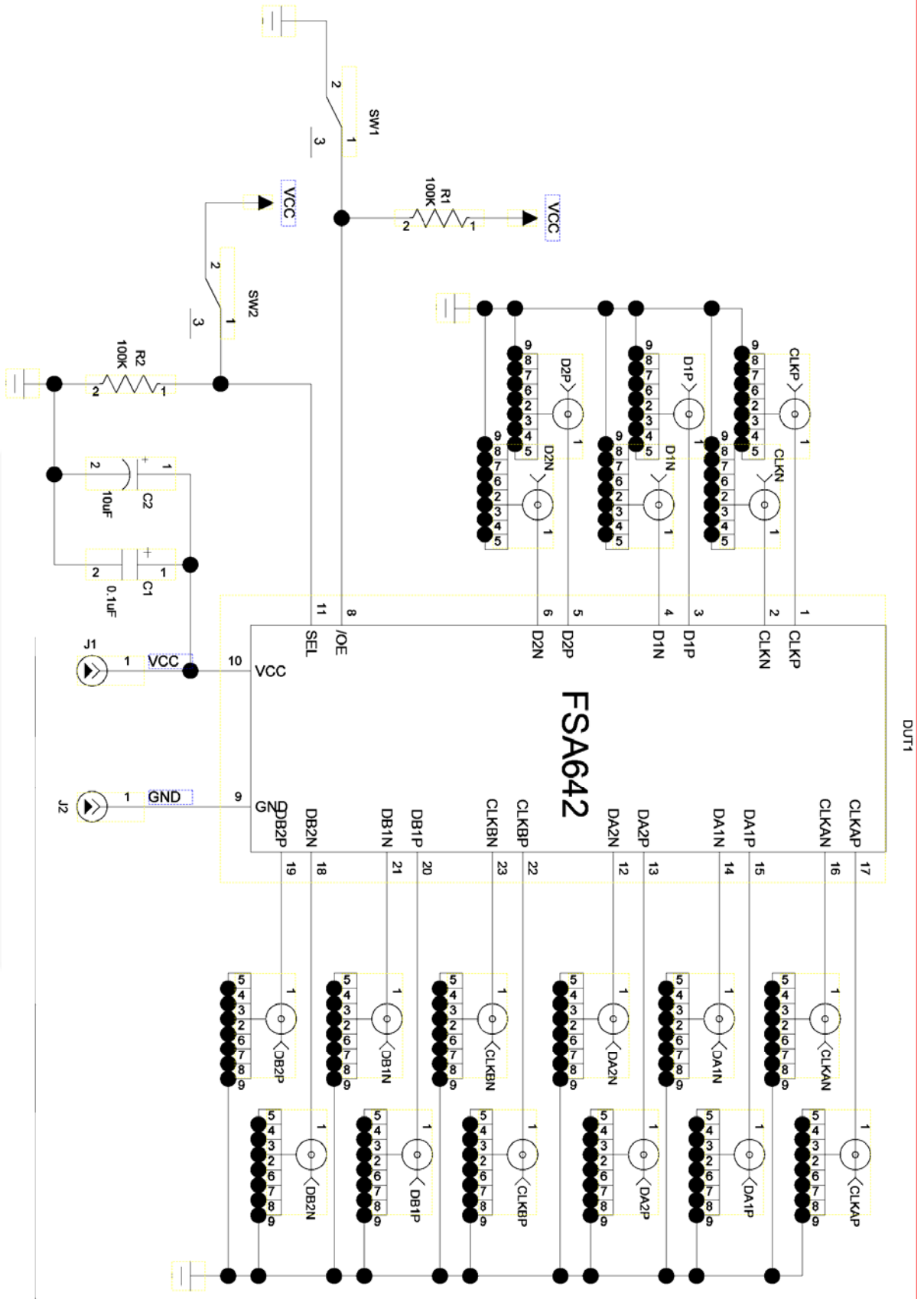


Figure 1. Application Board Schematic

WARNING AND DISCLAIMER

Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Users' Guide. Contact an authorized Fairchild representative with any questions.

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Revision History

Date	Reason for Change	Revision #
04/02/10	Initial Draft (S.Barden)	A0.0

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