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AN-8010

FMS6363 Evaluation Board Application Note

Description

The FMS6363 evaluation board provides a flexible base for evaluating the performance of the FMS6363. The board operates from a standard supply voltage of +5V ± 5%.

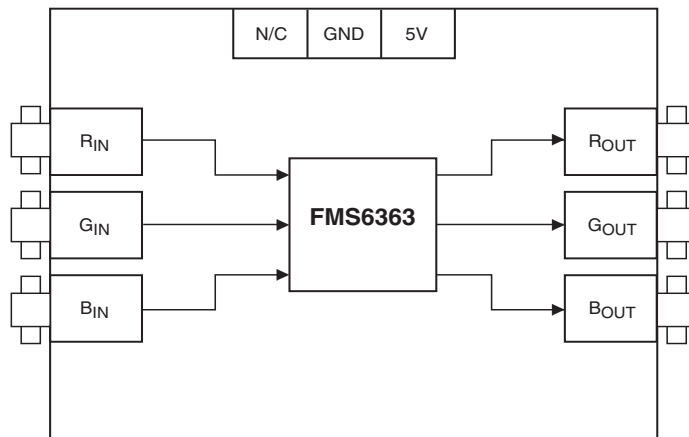
The FMS6363 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Three 6th order filters provide improved image quality compared to typical lower order passive solutions.

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

For a complete description of the FMS6363 please refer to the FMS6363 data sheet.

Evaluation Board Block Diagram



Evaluation Kit Contents

The FMS6363 Evaluation Kit contains the following items:

- AN-8010 – FMS6363 Evaluation Board Application Note
- The latest revision of the FMS6363 data sheet, which also can be obtained from <http://www.fairchildsemi.com>.
- Fully functional FMS6363 eval board
- Female power connector

Board Setup and Test

Use the following procedure to verify that the FMS6363 eval board is functional. This only verifies functionality. These instructions do not test any parameters outlined in the datasheet. The following test equipment is necessary to test the FMS6363 eval board.

- One power supply +5V \pm 5%, 250mA
- One HDTV
- One HD video signal source capable of generating necessary outputs (RGB or YPbPr)
- One video measurement set (VM5000)
- Assorted video cables

DO NOT turn on power supply until all connections are completed.

1. Set the power supply to 5.0V. Connect the power supply to the input voltage terminals of the evaluation board.
2. Connect the red output of the signal source to the R_{IN} connector on the FMS6363 board.
3. Connect the green output of the signal source to the G_{IN} connector on the FMS6363 board.
4. Connect the blue output of the signal source to the B_{IN} connector on the FMS6363 board.
5. Connect the red output of the FMS6363 board to the red input on the monitor.
6. Connect the green output of the FMS6363 board to the green input on the monitor.
7. Connect the blue output of the FMS6363 board to the blue input on the monitor.
8. Turn on the power supply.
9. Verify the HDTV is setup correctly.
10. Verify the test pattern that is produced from the generator is the same as the pattern on the monitor screen.
11. Functional test is now complete.

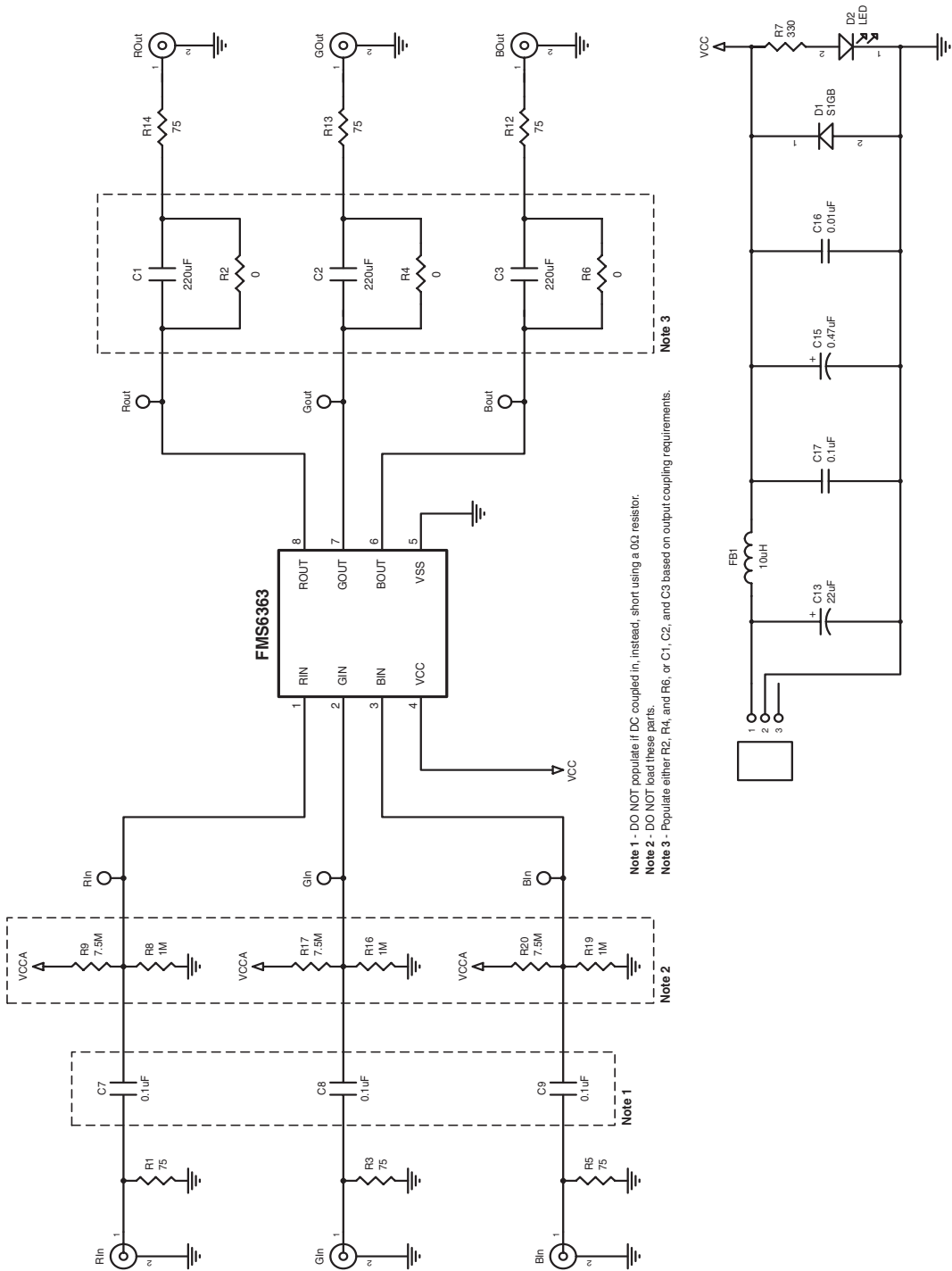


Figure 1. FMS6363 Schematic Diagram

Bill of Materials

Item	Quantity	Reference	Part
1	6	RIN, GIN, BIN, ROUT, GOUT, BOUT	BNC Connectors
2	3	C1, C2, C3	220 μ F
3	4	C7, C8, C9, C17	0.1 μ F
4	1	C13	22 μ F
5	1	C15	0.47 μ F
6	1	C16	0.01 μ F
7	1	D1	S1GB
8	1	D2	LED
9	1	FB1	10 μ H
10	1	JP1	PWRCON3
11	6	R1, R3, R5, R12, R13, R14	75 Ω
12	3	R2, R4, R6	0 Ω
13	1	R7	330 Ω
14	3	R8, R16, R19	1M Ω
15	3	R9, R17, R20	7.5M Ω
16	1	U1	FMS6363

Applications

The FMS6363 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required. The outputs can drive AC or DC-coupled single (150 Ω) loads. DC-coupling the output removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output. The FMS6363 Low Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input will be slightly offset to optimize the output driver performance. The FMS6363 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp will not operate. This allows DAC outputs to directly drive the FMS6363 without an AC coupling capacitor (usually 220 μ F). The offset is held to the minimum required value to decrease the standing DC current into the load.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. The FMS6363DEMO is a 4-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10 μ F and 0.1 μ F ceramic bypass capacitors
- Place the 10 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package
- Layout channel connections to reduce mutual trace inductance
- Minimize all trace lengths to reduce series inductances

If routing across a board, place device such that longer traces are at the inputs rather than the outputs.

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EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	Wire™
FACT™	IntelliMAX™	OPTOLOGIC®	SMART START™	
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		PowerEdge™	SuperSOT™-6	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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