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A Revised MOSFET Model With Dynamic Temperature Compensation

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Abstract

An empirical self-heating SPICE MOSFET model which accurately portrays the vertical DMOS power MOSFET electrical and thermal responses is presented. This macromodel implementation is the culmination of years of evolution in MOSFET modeling. This new version brings together the thermal and the electrical models of a VDMOS MOSFET. The existing electrical model [2,3] is highly accurate and is recognized in the industry. Simulation response of the new self-heating MOSFET model track the dynamic thermal response and is independent of SPICE's global temperature definition. Existing models may be upgraded to self-heating models with relative ease.

1. Introduction

Many power MOSFET models available today are based on an ideal lateral MOSFET device. They offer poor correlation between simulated and actual circuit performance in several areas. They have low and high current inaccuracies that could mislead power circuit designers. This situation is further complicated by the dynamic performance of the models. The ideal low power SPICE level-1 NMOS MOSFET model does not account for the nonlinear capacitive characteristics C_{iss}, C_{oss}, C_{rss} of a power MOSFET. Higher level SPICE MOSFET models may be used to implement the non-linear capacitance with mixed results. The inherent inaccuracies of modeling a power VDMOS with the SPICE MOSFET model dictated the need for an alternative approach; a macro-model.

A macro-model such as the one defined by Wheatley and Hepp [1] can address the short comings of the ideal low power SPICE MOSFET model. Highly accurate results are possible by surrounding the ideal level-1 MOSFET model with resistive, capacitive, inductive and other SPICE circuit elements. Two examples will illustrate the approach:

1) It was demonstrated in [3] that a third parallel MOSFET is required to accurately model the exponential relationship of drain current and gate-tosource voltage in the

sub-threshold region.

2) The implementation of the network (figure 1) using switches S1 and S2 provided a method to precisely model the non-linear capacitance. The result is an accurate representation of the dynamic transition between blocking and conduction.

The need for this higher level modeling accuracy becomes apparent in high frequency applications where gate charge losses as a proportion of overall losses become significant. The same situation exists for the space charge limiting effect at high drain current.

The MOSFET model reference on which this work is based has been explained in [1, 2, 3]. The reader is encouraged to refer to these references for a full understanding of the MOSFET model parameters herein referenced as the standard SPICE MOSFET model.

Recent works [8, 9] have demonstrated methods of circumventing the SPICE global temperature definition, providing a means of using the device's own junction temperature as a self-heating feedback mechanism.

The model developed in [8] has limitations involving proprietary algorithms, rendering the method of limited interest. Model implementation is convoluted, involving a MOSFET analog behavioral model (ABM) implementation whose operating characteristics are dependent on a SPICE level-3 NMOS MOSFET. As a result, both the switching circuit and the load must be duplicated for the model to function. The implementation in [9] does not model the drain-source avalanche property of a MOSFET. Neither [8] nor [9] attempt to model the temperature characteristics of the intrinsic body diode.

Introduced self-heating modeling concepts are non-proprietary and may be adapted to other MOSFET models.

2. Standard SPICE MOSFET Model

The macro-model in Figure 1 is that used in numerous Fairchild MOSFET device models. It is the evolution of many years of work and improvements from numerous contributors [1-7]. A significant advantage of this model is that extensive knowledge of device physics or process details are not required for implementing parametric data within the model. The following data curves are the basis used to generate the macro-model model over temperature:

- transfer characteristic
- saturation characteristic

- $r_{DS(ON)}$
- gate threshold voltage
- drain-to-source breakdown voltage
- intrinsic body diode voltage
- capacitance versus drain-to-source voltage
- gate charge waveform

Parametric data for up to five temperature points are used for model calibration resulting in a macro-model that provides representative simulation data for any rated operating junction temperature.

A limitation of the standard MOSFET model is found when simulating high power pulsed dissipations, and paralleled device operation. Reliance of the SPICE MOSFET primitive on the global analysis temperature variable (*.TEMP* SPICE instruction) results in simulations having all MOSFETs operating at a single predefined temperature. Device behaviour under high power dissipation transitory excursions and paralleled operation cannot be accurately modeled with a globally assigned temperature. Threshold voltage and $r_{DS(ON)}$ are but two important temperature dependant device characteristics that can vary sufficiently due to power dissipation as to render a simulation inaccurate. Accurate modeling of the previously mentioned operating modes requires incorporating temperature device behaviour at the model level rather than the global level.

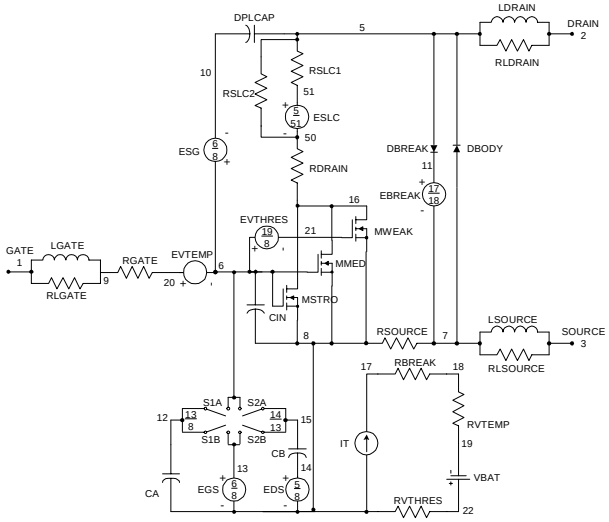

Figure 1. Standard MOSFET macro-model dependent on global temperature definition

3. Self-Heating SPICE MOSFET Model

Improved implementation of static and dynamic behavior is achieved with the self-

heating SPICE MOSFET model (Figure 2), an evolution of the standard MOSFET model (Figure 1). Temperature dependent model parameters respond in closed loop form to the junction temperature information provided by node *Tj*. Performance is independent of SPICE's global temperature definition *.TEMP* and temperature option *TNOM*, circumventing the level-1 NMOS model primitive temperature limitation. All MOSFET operating losses are inclusive in the current source *G_Pdiss* (scaling of 1A = 1W dissipation) representing instantaneous power dissipation into the thermal model.

Multiple MOSFETs may be simulated at different and variable junction temperatures. Each MOSFET may be connected to a heat sink model via node *Tcase*. The heat sink model may be device specific, so heat sink optimization becomes possible. Current source *G_Pdiss* is referenced to the simulation ground reference, permitting use of the model in bridge topologies.

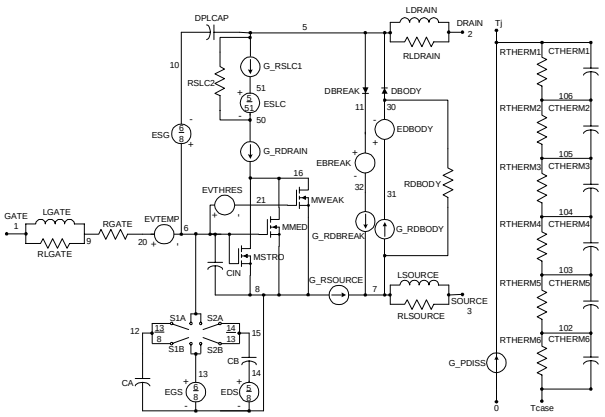

Figure 2. Self-heating MOSFET macro-model independent of global temperature definition

An example of a symbol representation of the self-heating MOSFET model is shown in Figure 3. Symbol files for OrCAD's two circuit entry tools "PSpice Schematic" and "OrCAD Capture"may be downloaded from www.fairchildsemi.com. Recommended symbol implementation is to designate the pinout attribute for *Tj* as optional (*ERC = DON'T CARE*). *Tj* is the representation of the device junction temperature. It may be used as a monitoring point, or it may be connected to a defined voltage source to override the self-heating feature. *Tcase* must be connected to a heat sink model. Treatment of connections to the model's gate, drain, and source terminals are no different than those of the standard MOSFET model.

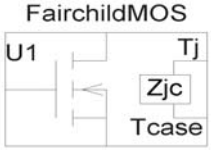

Figure 3. Self-heating MOSFET SPICE symbol

4. Self-Heating Model Implementation

Ability to describe the value of a resistor and its temperature coefficients as a behavioral model referenced to a voltage node is necessary to express dependence on junction temperature. PSPICE resistor ABMs do not permit voltage node references. Dynamic temperature dependence of the MOSFET's resistive element (expressed as separate lumped elements) and of the diode's resistive component cannot be implemented without a resistor ABM.

This limitation is overcome with a voltage controlled current source ABM expression (Figure 4). By using the nodes of the current source for voltage control, resistor behaviour may be expressed as $I = V/R(T_j)$. The resistance $R(T_j)$ becomes a behavioral model expression dependent on the voltage node *Tj* representation of junction temperature.

This voltage-controlled current source ABM model was used to modify the standard MOSFET model from Figure 1 by implementing voltage dependent expressions of *RDRAIN*, *RSOURCE*, and *RSLC1*.

Behavioral expressions were implemented in the self-heating model to eliminate *IT*, *RBREAK*, *RVTEMP*, and *VBAT* through modification of ABM expressions *EVTEMP*, *EVTHRES*, and *EBREAK*.

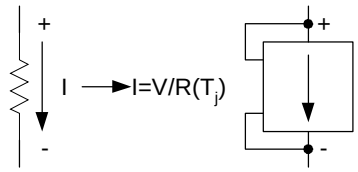

Figure 4. Implementing a voltage dependent ABM resistor model

Temperature dependent resistive elements of diodes *DBODY* and *DBREAK* were separated from the diode model, and expressed as voltagecontrolled current source ABM models *G_RDBODY* and *G_RDBREAK*. A large value resistor *RDBODY* was added to improve convergence.

EDBODY is added in series with *DBODY* to incorporate the temperature dependency of the intrinsic body diode forward conduction drop.

Junction temperature information is implemented by the inclusion of the MOSFET's thermal network $Z_{\theta JC}$ and current source *G_PDISS*. The thermal network parameters are supplied in Fairchild data sheets. *G_PDISS* calculates the MOSFET instantaneous operating loss, and expresses the result in the form of a current using the scaling ratio of 1A = 1W. This is a circuit form implementation of the junction temperature from expression (1)

$$T_j = P_{dissipation} \cdot Z_{\theta JC} + T_{case} \quad (1)$$

where T_j = junction temperature, $P_{dissipation}$ = instantaneous power loss, $Z_{\theta JC}$ = thermal impedance junction-to-case and T_{case} = case temperature. *Tj* and *Tcase* use the scaling factor 1V = 1°C.

5. Simulation Results

The unclamped inductive switching (UIS) test circuit in Figure 5 was used to compare the performance of the FDP038AN06A0 (3.8 mΩ, 60V, TO-220) self-heating MOSFET model with that of the standard model and measurement results. Incircuit measurements were performed with the device case temperature interfaced to a large heatsink at a temperature of 25°C.

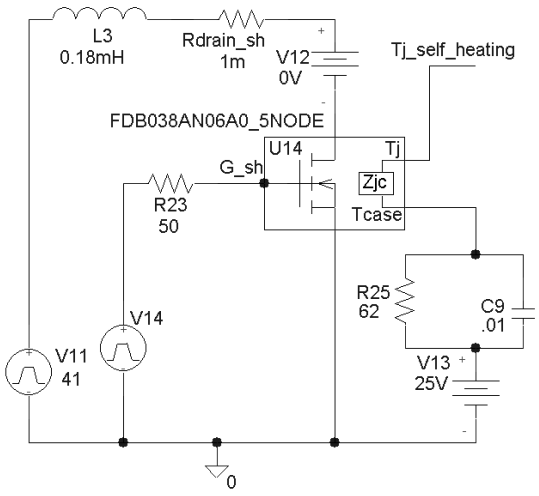

Figure 5. UIS simulation circuit

The UIS simulation for the standard MOSFET model was performed with PSPICE *TNOM* and *.TEMP* variables set to 25°C (Figure 6). The lack of temperature feedback to the model results in a drain-source breakdown voltage that is only drain current dependent. It does not demonstrate the device's breakdown voltage positive temperature coefficient. Source resistance (*G_Rsource*) is added to lower the gain at high currents. It is also a contributing element to the device $r_{DS(ON)}$. Plotting the square root of I_{DS} versus V_{GS} results in a linear curve instead of a quadratic curve, thus improving the visual resolution of the data at the higher current range.

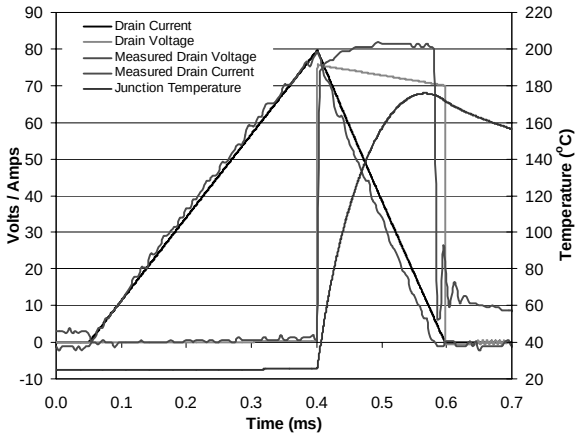

Figure 6. FDP038AN06A0 standard model UIS simulation results

UIS simulation and measured results for a selfheating MOSFET model are shown in Figure 7. Simulated drain-source breakdown voltage demonstrates the model dependence on drain current as well as on junction temperature. Excellent agreement exits.

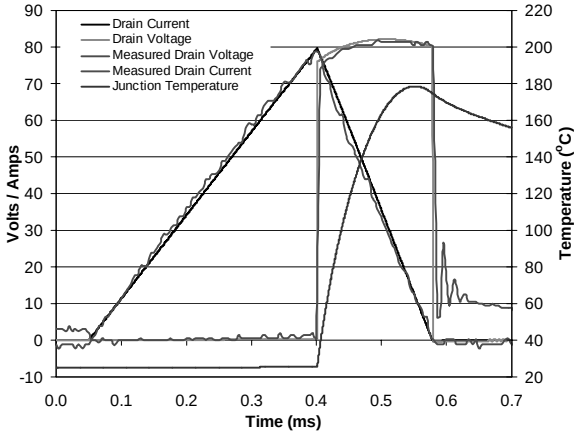

Figure 7. FDP038AN06A0 self-heating model UIS simulation results

Accuracy of the self-heating model is further verified by comparing its performance with that of the standard model, and with the characterization data from which the standard model was developed.

Results are shown in Figures 8, 9, 10 for gate threshold, $r_{DS(ON)}$, and conduction saturation voltage. Excellent agreement exists.

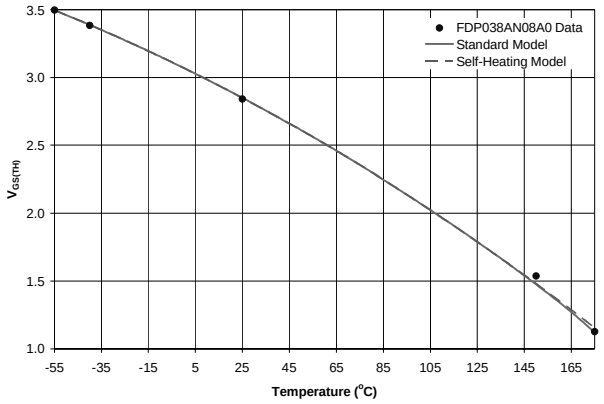

Figure 8. FDP038AN06A0 threshold voltage Conditions: I_D = 250µA

A small threshold voltage difference of 30 mV between the models exists as device junction temperature approaches 175°C, but is well within device yield parametric variation. This is a result of the different approaches used in modeling the intrinsic body diode.

The standard model intrinsic body diode is sensitive to the PSPICE *TNOM* temperature option definition. The temperature dependency on *TNOM* was eliminated in the self-heating model. As a result, the self-heating model intrinsic body diode does not exhibit the leakage current's temperature dependence.

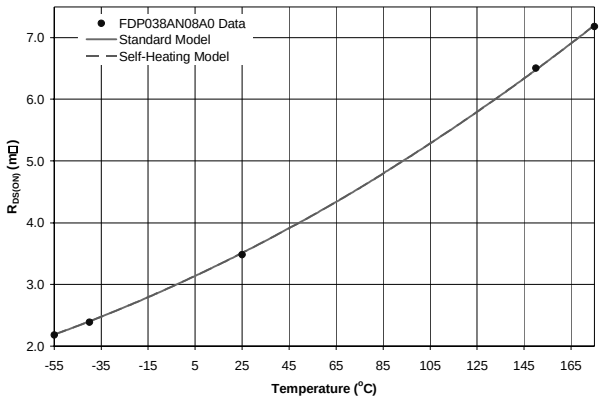

Figure 9. FDP038AN08A0 $r_{DS(ON)}$ Conditions: I_D = 80A, V_{GS} = 10V

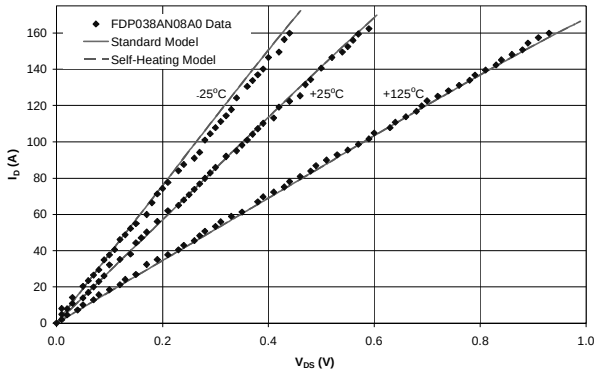

Figure 10. FDB038AN08A0 saturation voltage Conditions: V_{GS} = 10V

6. Simulation Convergence

The self-heating model was tested under numerous circuit configurations. It was found to be numerically stable. Failure to converge can occur under some large signal simulations if PSPICE's setup option *ABSTOL* setting is less than 1µA.

UIS simulations were performed on a Dell Latitude CSx having a 500MHz Pentium III processor with 256MB of memory. Windows 2000 was the operating system used with virus scan software enabled. PSPICE Schematics version 9.1 was used.

Simulation time results were:

- standard model = 7.9s
- self-heating model = 13.7s

Simulation time is expected to be longer with the self-heating model due to the dynamic interaction of the junction temperature feedback.

7. Future Model Developments

Minor inaccuracy is introduced if previously published Fairchild Semiconductor MOSFET models are modified to become self-heating models, but are within device parametric tolerance (this is not demonstrated in this paper). The inaccuracy can be eliminated by including the variable *T_ABS=25* in the level-1 NMOS MOSFET during device specific model calibration, permitting full compatibility of the model with the new self-heating model. This term was included for the standard MOSFET model calibration of the FDP038AN06A0. Temperature dependency of the self-heating model intrinsic body diode leakage current could be introduced by adding a junction temperature dependent current source across the body diode.

8. Conclusion

The self heating PSPICE power MOSFET macromodel provides the next evolutionary step in circuit simulation accuracy. The inclusion of a thermal model coupled to the temperature sensitive MOSFET electrical parameters results in a selfheating PSPICE MOSFET macro-model which allows increased accuracy during time domain simulations. The effect of temperature change due to power dissipation during time domain simulations can now be modeled. The modeling modification concepts introduced are non-proprietary and may be adapted to MOSFET SPICE models from any manufacturer.

References

[1] W.J. Hepp, C. F. Wheatley, “A New PSPICE Subcircuit For The Power MOSFET Featuring Global Temperature Options”, IEEE Transactions on Power Electronics Specialist Conference Records, 1991 pp. 533-544.

[2] “A New PSPICE Subcircuit for the Power MOSFET Featuring Global Temperature Options”, Fairchild Semiconductor, Application Note AN-7510, October 1999.

[3] S. Benczkowski, R. Mancini, “Improved MOSFET Model”, PCIM, September 1998, pp. 64-69.

[4] G.M. Dolny, H.R. Ronan, Jr., and C.F. Wheatley, Jr., “A SPICE II Subcircuit Representation for Power MOSFETs Using Empirical Methods,” RCA Review”, Vol 46, Sept 1985.

[5] C.F. Wheatley, Jr., H.R. Ronan, Jr., and G.M. Dolny, “Spicing- up SPICE II Software For Power MOSFET Modeling,” Fairchild Semiconductor, Application Note AN7506, February 1994.

[6] C.F. Wheatley, Jr. and H.R. Ronan, Jr., “Switching Waveforms of the L 2 FET: A 5Volt Gate Drive Power MOSFET,” Power Electronics Specialist Conference Record, June 1984, p. 238.

[7] G.M. Dolny, C.F. Wheatley, Jr., and H.R. Ronan, Jr., “Computer Aided Analysis Of Gate-Voltage Propagation Effects In Power MOSFETs”, Proc. HFPC, May 1986, p. 146.

[8] F. Di Giovanni, G. Bazzano, A. Grimaldi, ”A New PSPICE Power MOSFET Subcircuit with Associated Thermal Model“, PCIM 2002 Europe, pp. 271-276.

[9] M. März, P. Nance, “Thermal Modeling of Power-electronic Systems”, Infineon Technologies, Application Note, mmpn_eng.pdf.

Appendix I
Standard MOSFET SPICE Model

```
.SUBCKT FDP038AN06A0 2 1 3
*Nom Temp=25 deg C
*7 February 2003
Ca 12 8 1.5e-9
Cb 15 14 1.5e-9
Cin 6 8 6.1e-9
Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
Ebreak 11 7 17 18 69.3
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1
It 8 17 1
Lgate 1 9 4.81e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 4.63e-9
RLgate 1 9 48.1
RLdrain 2 5 10
RLsource 3 7 46.3
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 1.0e-4
Rgate 9 20 1.36
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 2.8e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
Vbat 22 19 DC 1
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/
+(1e-6*300),10))}
.MODEL DbodyMOD D (IS=2.4E-11 N=1.04 RS=1.65e-3 TRS1=2.7e-3
+ TRS2=2e-7 CJO=4.35e-9 M=5.4e-1 TT=1e-9 XTI=3.9)
.MODEL DbreakMOD D (RS=7.0e-2 TRS1=5e-4 TRS2=1.0e-7)
.MODEL DplcapMOD D (CJO=1.7e-9 IS=1e-30 N=10 M=0.47)
.MODEL MmedMOD NMOS (VTO=3.3 KP=9 IS=1e-30 N=10 TOX=1
```

```
+ L=1u W=1u RG=1.36 T_abs=25)
.MODEL MstroMOD NMOS (VTO=4.00 KP=275 IS=1e-30 N=10
+ TOX=1 L=1u W=1u T_abs=25)
.MODEL MweakMOD NMOS (VTO=2.72 KP=0.03 IS=1e-30 N=10
+ TOX=1 L=1u W=1u RG=13.6 RS=.1 T_abs=25)
.MODEL RbreakMOD RES (TC1=9e-4 TC2=1e-7)
.MODEL RdrainMOD RES (TC1=5.5e-2 TC2=3.2e-4)
.MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-5)
.MODEL RsourceMOD RES (TC1=5e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-6.7e-3 TC2=-1.5e-5)
.MODEL RvtempMOD RES (TC1=-2.5e-3 TC2=1e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4
+ VOFF=-1.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5
+ VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1
+ VOFF=.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=.5
+ VOFF=-1)
.ENDS
*Thermal Model Subcircuit
.SUBCKT FDP038AN06A0_Thermal TH TL
CTHERM1 TH 6 6.45e-3
CTHERM2 6 5 3e-2
CTHERM3 5 4 1.4e-2
CTHERM4 4 3 1.65e-2
CTHERM5 3 2 4.85e-2
CTHERM6 2 TL 1e-1
RTHERM1 TH 6 3.24e-3
RTHERM2 6 5 8.08e-3
RTHERM3 5 4 2.28e-2
RTHERM4 4 3 1e-1
RTHERM5 3 2 1.1e-1
RTHERM6 2 TL 1.4e-1
.ends
```

Appendix II
Self-Heating MOSFET SPICE Model

```
.SUBCKT FDP038AN06A0_5NODE 2 1 3 Tj Tcase
** Spice model for FDP038AN06A0
*7 February 2003
Ca 12 8 1.5e-9
Cb 15 14 1.5e-9
Cin 6 8 6.1e-9
EDbody 31 30 VALUE={IF(V(Tj,0)<175,-1.5E-3*V(Tj,0)+.03,-.2325)}
Dbody 30 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
RDBODY 30 7 1E15
G_Rdbody 7 31 VALUE={V(7,31)/(1.65e-3*(1+2.7E-3*(V(Tj,0)-25)+
+2E-7*PWR((V(Tj,0)-25),2)))}
G_Rdbreak 32 7 VALUE={v(32,7)/(7.0e-2*(1+5e-4*(V(Tj,0)-25)+
+1e-7*PWR((V(Tj,0)-25),2)))}
Ebreak 11 32 VALUE={69.3*(1+9.5E-4*(V(Tj,0)-25)+1e-7*
+PWR((V(Tj,0)-25),2))}
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 VALUE={-6.7E-3*(V(Tj,0)-25)-1.5E-5*PWR((V(Tj,0)-
+25),2)}
Evtemp 20 6 VALUE={-2.5e-3*(V(Tj,0)-25)+1e-6*PWR((V(Tj,0)-25),2)}
Lgate 1 9 4.81e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 4.63e-9
RLgate 1 9 48.1
RLdrain 2 5 10
RLsource 3 7 46.3
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
G_Rdrain 50 16 VALUE={V(50,16)/(1E-4*(1+5.5E-2*(v(Tj,0)-25)+
+3.2E-4*pwr((v(Tj,0)-25),2)))}
Rgate 9 20 1.36
G_RSLC1 5 51 VALUE={v(5,51)/(1e-6*(1+1E-3*(v(Tj,0)-25)+
+1E-5*pwr((v(Tj,0)-25),2)))}
RSLC2 5 50 1e3
G_Rsource 8 7 VALUE={V(8,7)/(2.8E-3*(1+5e-3*(V(Tj,0)-25)+
+1e-6*pwr((V(Tj,0)-25),2)))}
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/
+(1e-6*300),10))}
G_PDISS 0 TH+ VALUE={I(ESLC)*V(5,7) + I(EVTEMP)*V(9,7) +
```

```
+ I(EBREAK)*V(5,7) + I(EDBODY)*V(7,5)}CTHERM1 Tj 106 6.45E-3
CTHERM2 106 105 3e-2
CTHERM3 105 104 1.4e-2
CTHERM4 104 103 1.65e-2
CTHERM5 103 102 4.85e-2
CTHERM6 102 Tcase 1e-1
RTHERM1 Tj 106 3.24e-3
RTHERM2 106 105 8.08e-3
RTHERM3 105 104 2.28e-2
RTHERM4 104 103 1e-1
RTHERM5 103 102 1.1e-1
RTHERM6 102 Tcase 1.4e-1
.MODEL DbodyMOD D (T_ABS=25 IS=2.4E-11 N=1.04 CJO=4.35e-9
+ M=0.54 TT=1.0e-9 XTI=3.9)
.MODEL DbreakMOD D ()
.MODEL DplcapMOD D (CJO=1.7e-9 IS=1e-30 N=10 M=0.47)
.MODEL MmedMOD NMOS (T_ABS=25 VTO=3.3 KP=9 IS=1e-30
+ N=10 TOX=1 L=1u W=1u RG=1.36)
.MODEL MstroMOD NMOS (T_ABS=25 VTO=4.0 KP=275 IS=1e-30
+ N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (T_ABS=25 VTO=2.72 KP=0.03
+ IS=1e-30 N=10 TOX=1 L=1u W=1u RG=13.6 RS=.1)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4
+ VOFF=-1.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5
+ VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1
+ VOFF=.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=.5
+ VOFF=-1)
.ENDS
```

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CoolFET™	FRFET™	MicroPak™	QS™	TinyLogic®
CROSSVOLT™	GlobalOptoisolator™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
DOME™	GTO™	MSX™	Quiet Series™	TruTranslation™
EcoSPARK™	HiSeC™	MSXPro™	RapidConfigure™	UHC™
E^{2}CMOS™	I^{2}C™	OCX™	RapidConnect™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	VCX™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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