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AN-6204

FAN6204 — Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

Introduction

This application note presents the design considerations for Fairchild secondary-side synchronous rectification (SR) controller, FAN6204, which is suitable for Continuous Conduction Mode (CCM) / Discontinuous Conduction Mode (DCM) / Quasi-Resonant (QR) flyback converters and dual-switch forward free-wheeling rectification (Figure 1 and Figure 2).

FAN6204 utilizes a proprietary innovative linear-predict timing control to determine the turn-on and turn-off timing of SR MOSFET. This control technique detects the voltage of the transformer winding and output voltage instead of MOSFET current, so noise immunity can be accomplished. Furthermore, this technique doesn't need a communication signal from the primary side, so this feature reduces external components and simplifies PCB layout.

In abnormal test conditions, since Linear-Predict Timing control (LPT) and causal function may not guarantee safe operation, some protection functions should be applied. Fault Causal Timing protection, Gate Expand Limit protection, and RES voltage drop protection are used for load-change test condition. LPC and RES pins' open/short protection is to prevent fault operation of SR controller if LPC/RES resistors are damaged. In addition, internal Over-Temperature Protection (OTP) and V_{DD} Over-Voltage Protection (VDD OVP) are also included to avoid a timing sequence where FAN6204 is uncontrollable under high-temperature or output over-voltage condition.

To improve no-load or light-load efficiency, a Green Mode function is utilized. In Green Mode, the SR controller stops all SR switching to reduce the operating current, keeping power consumption at low levels in light-load condition.

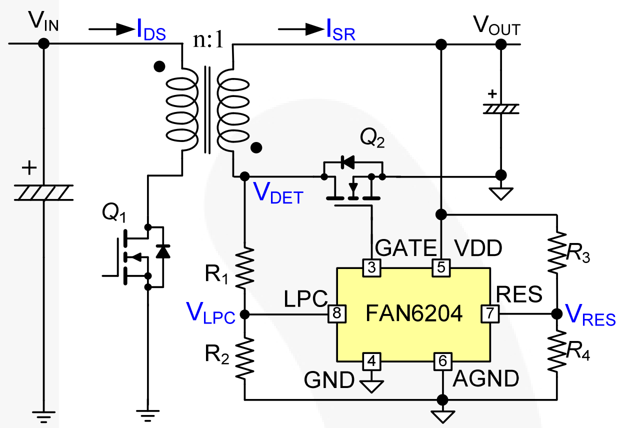

Figure 1. Typical Application Circuit for Flyback Converter

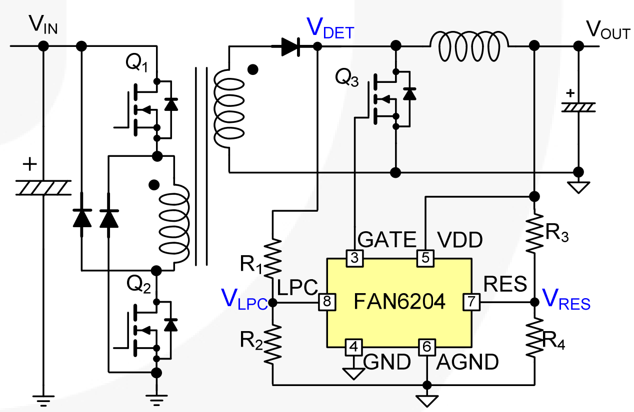

Figure 2. Typical Application Circuit for Dual-Switch Forward Free-Wheeling Rectification

External Components Design

(a) Flyback Rectification Application

As shown in Figure 1, the resistors on the LPC and RES pins need to be designed appropriately for linear predict timing control. Referring to Figure 3, when LPC voltage is higher than V_{LPC-EN} over a blanking time (t_{LPC-EN}), SR gate is ready to output. After LPC voltage drops below $V_{LPC-TH-HIGH}$ (0.05 V_{OUT}), SR MOSFET starts to output. Therefore, V_{LPC-EN} must be higher than $V_{LPC-TH-HIGH}$ or the SR MOSFET cannot be turned on. Consequently, the voltage divider of LPC, R_1 and R_2, should be considered as:

$$0.83 \cdot \frac{R_2}{R_1+R_2} \cdot \left(\frac{V_{IN.MIN}}{n} + V_{OUT}\right) > 0.05V_{OUT} + 0.3 \quad (1)$$

On the other hand, the linear operating range of LPC and RES (1~4 V) should also be considered as:

$$\frac{R_2}{R_1+R_2} \cdot \left(\frac{V_{IN.MAX}}{n} + V_{OUT}\right) < 4 \quad (2)$$

$$1 < \frac{R_4}{R_3+R_4} \cdot V_{OUT} < 4 \quad (3)$$

Since the voltage scale-down ratio between RES and LPC (K) is 5, the discharge time of C_T ($t_{CT.DIS}$) is same as the inductor current discharge time ($t_{L.DIS}$). However, considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) should be larger than 5 to guarantee that $t_{CT.DIS}$ is shorter than $t_{L.DIS}$. It is typical to set K to 5~5.5.

$$K \cdot \frac{R_2}{R_1+R_2} = \frac{R_4}{R_3+R_4} \quad (4)$$

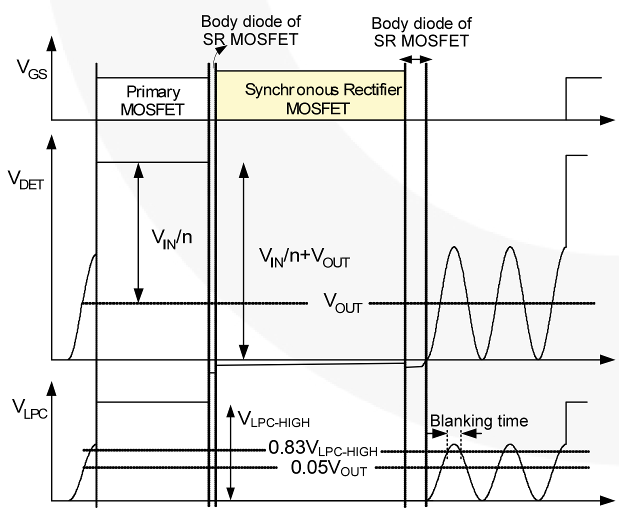

Figure 3. Typical Waveforms of QR Flyback Converter with FAN6204

(b) Dual-Switch Forward Free-Wheeling Rectification Application:

Figure 2 shows a typical application circuit for applying FAN6204 on forward free-wheeling diode rectification. V_{LPC-EN} must be higher than $V_{LPC-TH-HIGH}$ so the voltage divider of LPC, R_1 and R_2, should be considered as:

$$0.83 \cdot \frac{R_2}{R_1+R_2} \cdot \frac{V_{IN.MIN}}{n} > 0.05V_{OUT} + 0.3 \quad (5)$$

The linear operating range of LPC and RES (1~4 V) should also be considered as:

$$\frac{R_2}{R_1+R_2} \cdot \frac{V_{IN.MAX}}{n} < 4 \quad (6)$$

$$\frac{R_4}{R_3+R_4} \cdot V_{OUT} < 4 \quad (7)$$

Considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) is set to 5~5.5.

$$K \cdot \frac{R_2}{R_1+R_2} = \frac{R_4}{R_3+R_4} \quad (8)$$

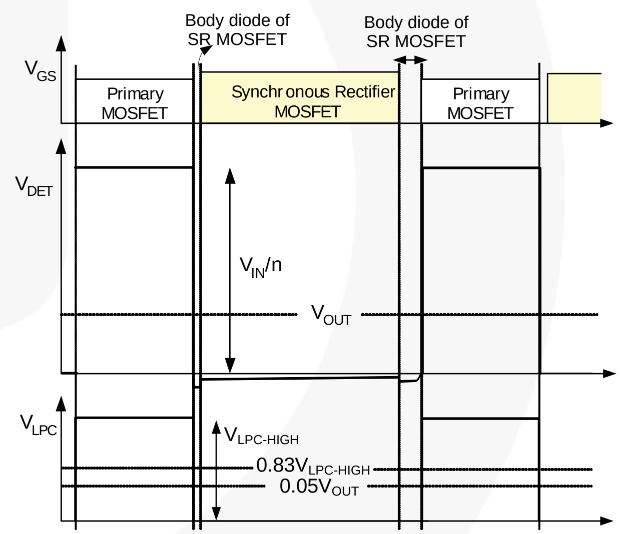

Figure 4. Typical Waveforms of Forward Free-Wheeling Rectification with FAN6204

(c) Consideration of External Component Value

LPC Part: To prevent LPC pin damage by negative voltage while V_{LPC} drops below $V_{LPC\text{-}SOURCE}$ (0.2 V), FAN6204 sources a current, $I_{LPC\text{-}SOURCE}$, from the LPC pin to clamp V_{LPC} at a positive voltage level. To operate regularly, the clamped voltage level must be lower than $V_{LPC\text{-}TH\text{-}HIGH}$, so R_2 should not be too large. If the low clamped voltage is higher than $V_{LPC\text{-}TH\text{-}HIGH}$, R_2 should be decreased to guarantee proper operation of SR controller. Once R_2 is decided, R_1 can also be determined due to calculated LPC ratio. The recommended value of R_2 is under 15 kΩ. In addition, if the noise interference is serious, a ceramic capacitor (around 10 pF to 22 pF) parallel on LPC pin is recommended.

RES Part: For power saving, the values of R_3 and R_4 are designed as large as possible (theoretically). Actually, since high-impedance components can cause noise interference, the values of RES resistors should not be designed too large. For the reason, the recommended value is 10 kΩ to several hundred kΩ.

(Design Example) Assume the input voltage (V_{IN}) is 373 V for high line ($V_{IN.MAX}$) and 127 V for low line ($V_{IN.MIN}$) in a flyback system; the output voltage is 19 V; and transformer turn-ratio (n) is 4.75. The maximum value of LPC ratio can be obtained from Equation (1):

$$\frac{R_1 + R_2}{R_2} < \frac{0.83 \cdot \left(\frac{V_{IN.MIN}}{n} + V_{OUT}\right)}{\frac{2 \cdot V_O}{40} + 0.3} = 30.4$$

The maximum value of LPC ratio can be obtained from Equation (2):

$$\frac{R_1 + R_2}{R_2} > \frac{\left(\frac{V_{IN.MAX}}{n} + V_{OUT}\right)}{4} = 24.4$$

Consequently, the LPC ratio should be between 24.4 and 30.4. After considering tolerance, LPC ratio is chosen to 26.38 and resistor value of LPC pin is R_1=330 kΩ and R_2=13 kΩ.

Assuming the scale-down ratio between LPC and RES (K) is 5.32, the RES ratio should be:

$$RES\ ratio = \frac{LPC\ ratio}{K} = \frac{26.38}{5.32} = 4.96$$

In addition, RES ratio=4.96 should also be checked by Equation (3):

$$1 < \frac{R_4}{R_3 + R_4} \cdot V_{OUT} = \frac{19}{4.96} = 3.8 < 4$$

Thus, R_3 and R_4 are chosen to 36 kΩ and 9.1 kΩ, respectively.

V_{DD} Section

Output voltage (V_O) can be applied as V_{DD} of FAN6204, while V_O is regulated between 5 V and 24 V. If V_O is not regulated in that range, an additional winding of transformer can be utilized to provide energy to V_{DD}. The simplified circuit is shown as Figure 5. To prevent the variation of the V_{DD} supply voltage, use a voltage regulator or voltage clamping components, such as a Zener diode, to clamp V_{DD} voltage in a proper range.

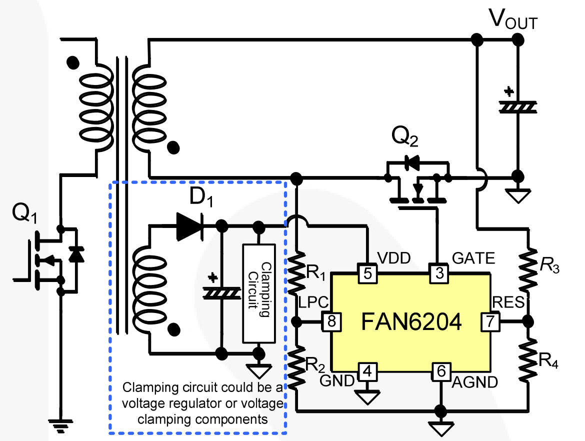

Figure 5. Simplified Circuit of Additional Winding for V_{DD} Supply

Printed Circuit Board Layout

Figure 6 shows the schematic for FAN6204 in a converter. Good PCB layout improves power system efficiency, minimizes excessive EMI, and prevents the power supply from being disrupted during surge/ESD tests.

IC Side:

- Reference ground of LPC and RES pins are connected to IC's AGND directly. (trace 1)
- IC's GND and AGND pins should be connected together with a **short, wide trace** or a **wide area**. (trace 1 and trace 2)
- Reference ground of VDD should connect to this **ground area of IC**, then the reference ground of VDD connects to C_{OUT}'s ground. (trace 3)
- The trace line of LPC and RES should be **far away from magnetic components.**

SYSTEM Side:

- Since trace 4 is the power loop on secondary side, it is as **short** as possible.
- Y-CAP should be connected to C_{OUT}'s ground with a **wide** trace on secondary side. (trace 5)

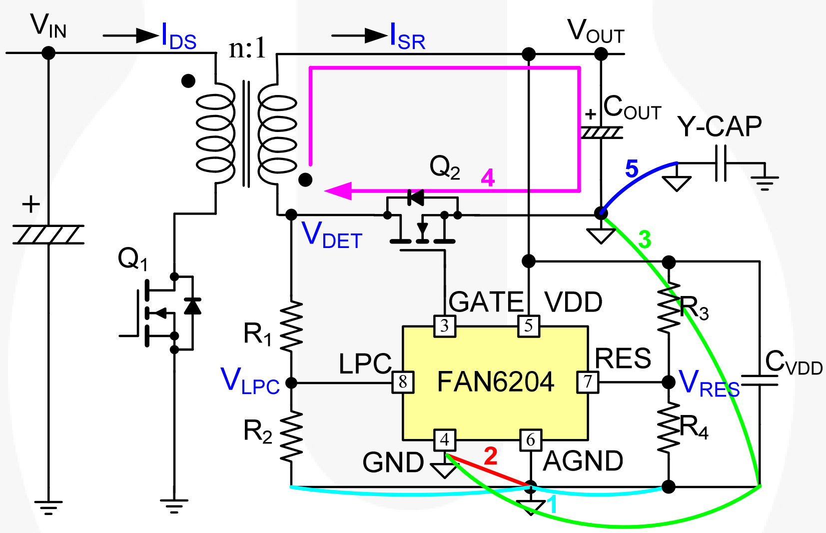

Figure 6. Layout Considerations

Design Example

This section shows a design example of 90 W (19 V/4.74 A) adaptor using FAN6921. The PFC output voltage is 250 V at low AC input voltage, 400 V at high AC input voltage. From the specification, all critical components are treated and final measurement results are given.

Table 1. System Specification

Input	
Input Voltage Range	90~264 V_{AC}
Line Frequency Range	47~63 Hz
Output	
Output Voltage (V_o)	19 V
Output Power (P_o)	90 W

The critical parameters are summarized, shown in Table 2.

Table 2. Critical System Parameters

PFC Stage	
PFC Output Voltage Level 1 (*PFCVo1*)	250 V
PFC Output Voltage Level 2 (*PFCVo2*)	400 V
PFC Inductor (L_b)	**385 µH**
Turns of PFC Inductor (N_b)	**60 T**
Turns of Auxiliary Winding (N_{AUX})	8 T
Minimum Switching Frequency ($f_{s,min,PFC}$)	55 kHz
PWM Stage	
Turns of Primary Inductor of PWM Transformer (N_P)	41 T
Turns of Auxiliary Winding of PWM Transformer (N_{AUX})	6 T
Turns Ratio of PWM Transformer (*n*)	6.8
Primary Inductor (L_P)	700 µH
Minimum Switching Frequency ($f_{s,min,PWM}$)	52 kHz

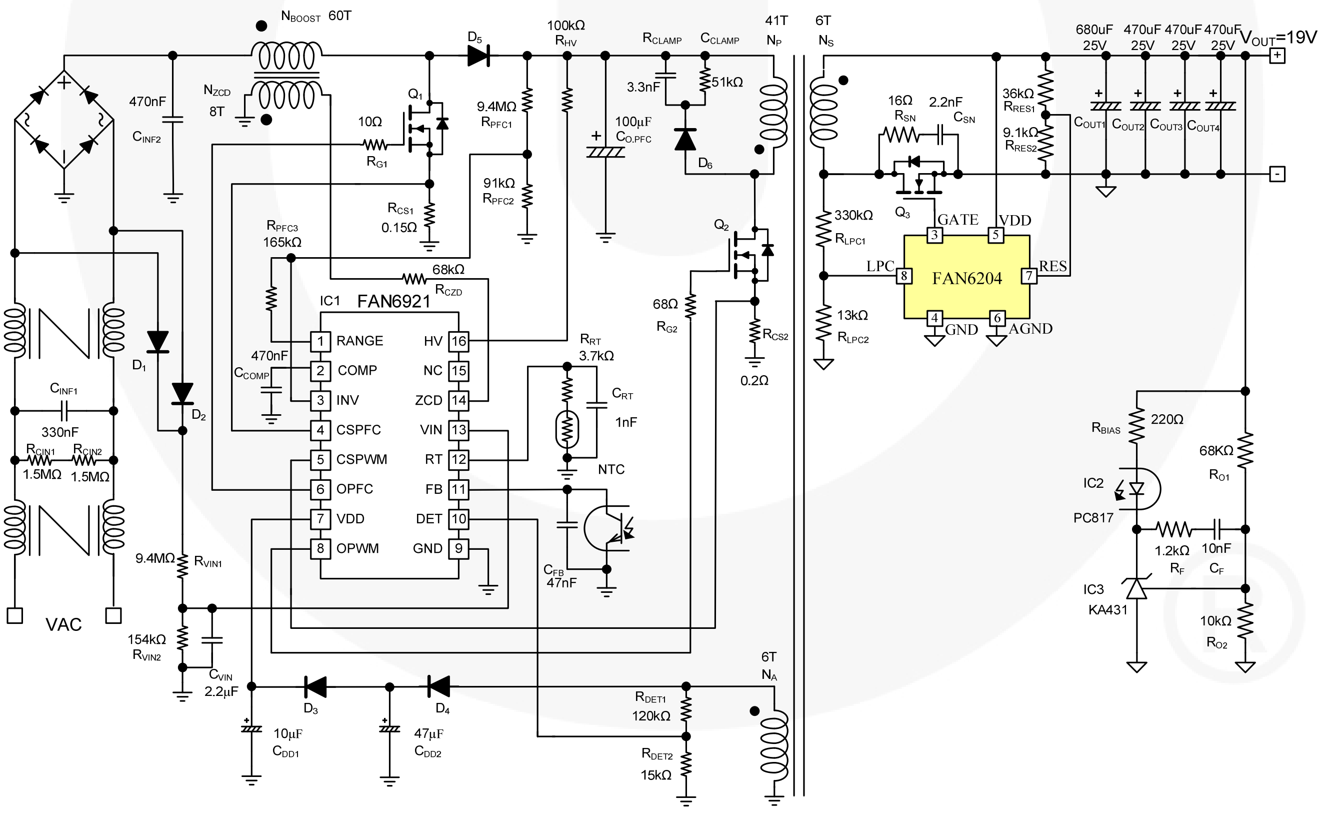

Figure 7. Complete Circuit Diagram

Table 3. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			C_{RT}	1 nF	
R_{PFC1}	9.4 MΩ	1/4 W	C_{FB}	47 F	
R_{PFC2}	91 kΩ	1/8 W	C_{CLAMP}	3.3 nF	
R_{PFC3}	165 kΩ	1/8 W	$C_{O.PFC}$	100 µF	450 V
R_{VIN1}	9.4 MΩ	1/4 W	C_{SN}	2.2 nF	
R_{VIN2}	154 kΩ	1/8 W	C_{F}	10 nF	
R_{ZCD}	68 kΩ	1/4 W	C_{OUT1}	680 µF	25 V
R_{HV}	100 kΩ	1/2 W	C_{OUT2}	470 µF	25 V
R_{CLAMP}	51 kΩ	1/4 W	C_{OUT3}	470 µF	25 V
R_{RT}	3.7 kΩ	1/8 W	C_{OUT4}	470 µF	25 V
R_{CS1}	0.15 Ω	1 W	**Diode**		
R_{CS2}	0.2 Ω	2 W	D_{1}	S1J	
R_{G1}	10 Ω	1/4 W	D_{2}	S1J	
R_{G2}	68 Ω	1/4 W	D_{3}	1N4148	
R_{DET1}	120 kΩ	1/4 W	D_{4}	1N4935	
R_{DET2}	15 kΩ	1/8 W	D_{5}	EGP30J	
R_{CIN1}	1.5 MΩ	1/4 W	D_{6}	RGP10M	
R_{CIN2}	1.5 MΩ	1/4 W	**MOSFET**		
R_{LPC1}	330 kΩ	1/8 W	Q_{1}	FCPF11N60	
R_{LPC2}	13 kΩ	1/8 W	Q_{2}	FDPF15N65	
R_{RES1}	36 kΩ	1/8 W	Q_{3}	FDP090N10	
R_{RES2}	9.1 kΩ	1/8 W	**IC**		
R_{SN}	16 Ω	1/2 W	IC_{1}	FAN6921MR	
R_{O1}	68 kΩ	1/8 W	IC_{2}	FOD817A	
R_{O2}	10 kΩ	1/8 W	IC_{3}	KA431	
R_{BIAS}	200 Ω	1/4 W	IC_{4}	FAN6204	
R_{F}	1.2 kΩ	1/8 W			
Capacitor					
C_{INF1}	330 nF	XCAP			
C_{INF2}	470 nF				
C_{VIN}	2.2 µF				
C_{COMP}	470 nF				
C_{DD1}	10 µF	50 V			
C_{DD2}	47 µF	50 V			

Figure 8 shows the test waveforms of 100% loading (4.74 A) on 19 V/90 W demonstration board. The SR gate can be turned off by linear-predict timing control and can keep a dead time between the primary-side and secondary-side MOSFET.

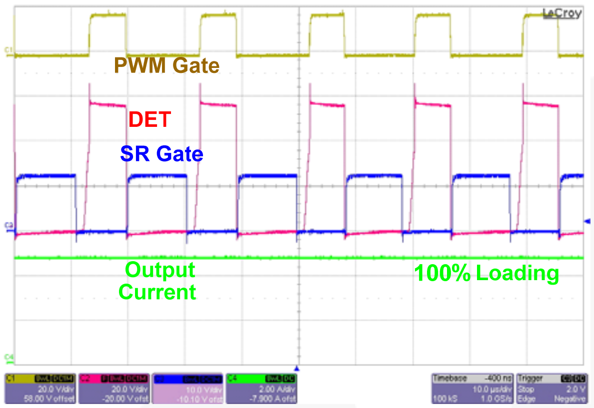

Figure 8. Test Waveforms of 100% Loading

Figure 9 shows the test waveforms of 25% loading on 19 V/90 W demonstration board. Linear-predict timing control can also be activated to turn off SR MOSFET to prevent overlap with PWM MOSFET.

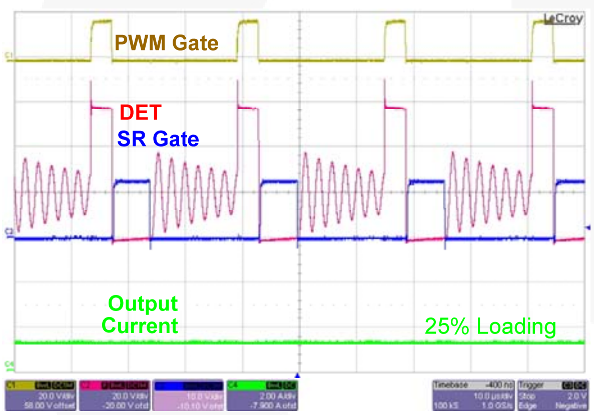

Figure 9. Test Waveforms of 25% Loading

Figure 10 and Figure 11 show the test waveforms for load changing from light load to heavy load and from heavy load to light load. There is no overlap between the primary- and secondary-side MOSFET.

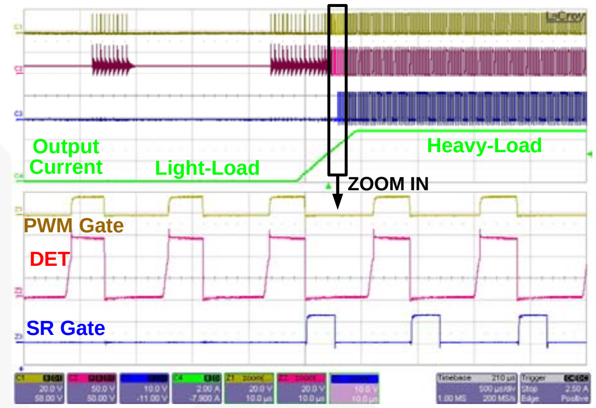

Figure 10. Test Waveforms for Load Change (Light Load to Heavy Load)

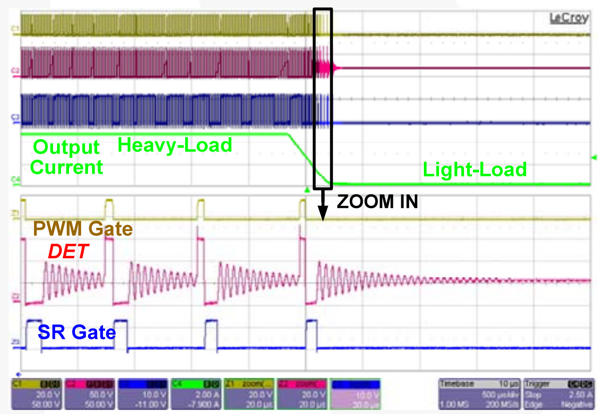

Figure 11. Test Waveforms for Load Change (Heavy Load to Light Load)

Related Datasheets

FAN6921MR — Highly Integrated Quasi-Resonant Current PWM Controller

FAN6921ML — Highly Integrated Quasi-Resonant Current PWM Controller

SG6742MR/ML —Highly Integrated Green-Mode PWM Controller

FAN6754A —Highly Integrated Green-Mode PWM Controller

FAN6204 —Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

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