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AN-6019 Fairchild Analog Switch Products ESD Test Methodology Overview

Summary

Analog Switches are often placed near the interconnections of the PCB board where they are used to route or isolate incoming or outgoing signals. For this reason, Fairchild Analog Switches have some of the highest Electrostatic Discharge (ESD) performance ratings in the industry. By testing the products to the most stringent of standards, JEDEC, Fairchild offers designers piece of mind through superior ESD protection. This Application Note provides an explanation of Fairchild's ESD test methodology for Analog Switches.

Human Body Model

Human Body Model (HBM) testing is conducted with strict adherence to JEDEC JESD22-A114. This test simulates the real-world event of human contact to the integrated circuit (IC). The HBM stress event is generated through a simple capacitor resistor combination, as depicted in Figure 1. The JEDEC standard requires a single positive and a single negative polarity stress applied to each pin combination in the IC. Pass/Fail determinations are based on the IC's compliance with datasheet parameters. Once the performance level for the entire IC is determined, additional testing is conducted on selected I/O pins, vs. ground, since the I/Os are the most likely to experience an HBM event. A reporting of the performance of the I/O pins is offered on the product datasheet.

Charged Device Model

Charged Device Model (CDM) testing simulates the potential ESD event ICs experience in the automated assembly process. Voltage potentials in the hundreds or even thousands of volts can be measured in assembly environments. To simulate these events and protect against them, Fairchild Analog Switches are tested to the JEDEC JESD22-C101 standard. All bonded pins of an IC are discharged (positive and negative potential) to a grounding pin. The performance of the product is provided in the Fairchild datasheet.

Machine Model

Machine Model (MM) testing has been used for years as a model to represent machine-to-machine ESD discharges. The international ESD community has determined that MM waveforms do not truly represent real-world ESD events. However, since this model has been used as a benchmark for product performance, Fairchild offers results of these tests upon request. Fairchild adheres to the JEDEC JESD22-A115 standard for this stress event.

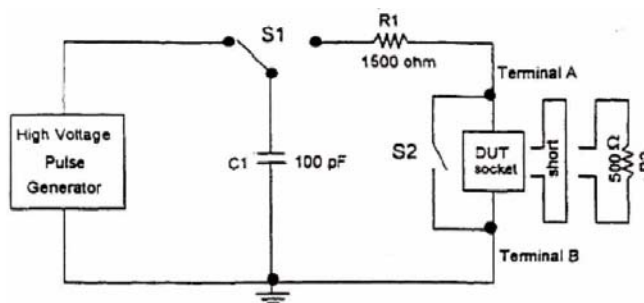


Figure 1. Human Body Model Test Circuit as outlined in JEDEC JESD22-A114

Fairchild Semiconductor's analog switches lead the market in ESD performance. An example using the FSUSB30 is provided in Figure 2. For further questions or to request specific ESD testing to meet application needs, contact Fairchild Semiconductor.

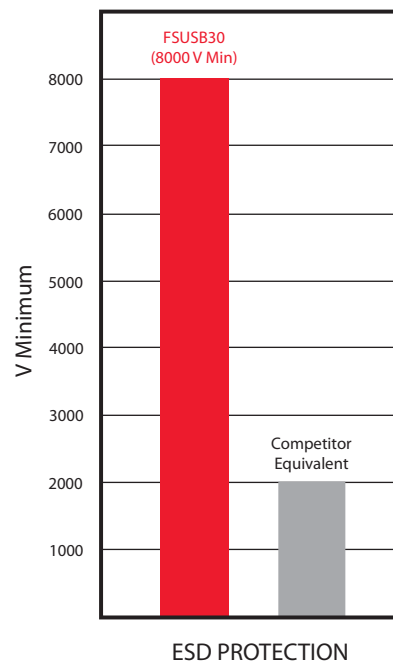


Figure 2. Fairchild's FSUSB30 ESD protection vs. competitor performance

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