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Application Note AN-5053

µSerDes™ Devices with a Synchronous Pixel Interface

Introduction

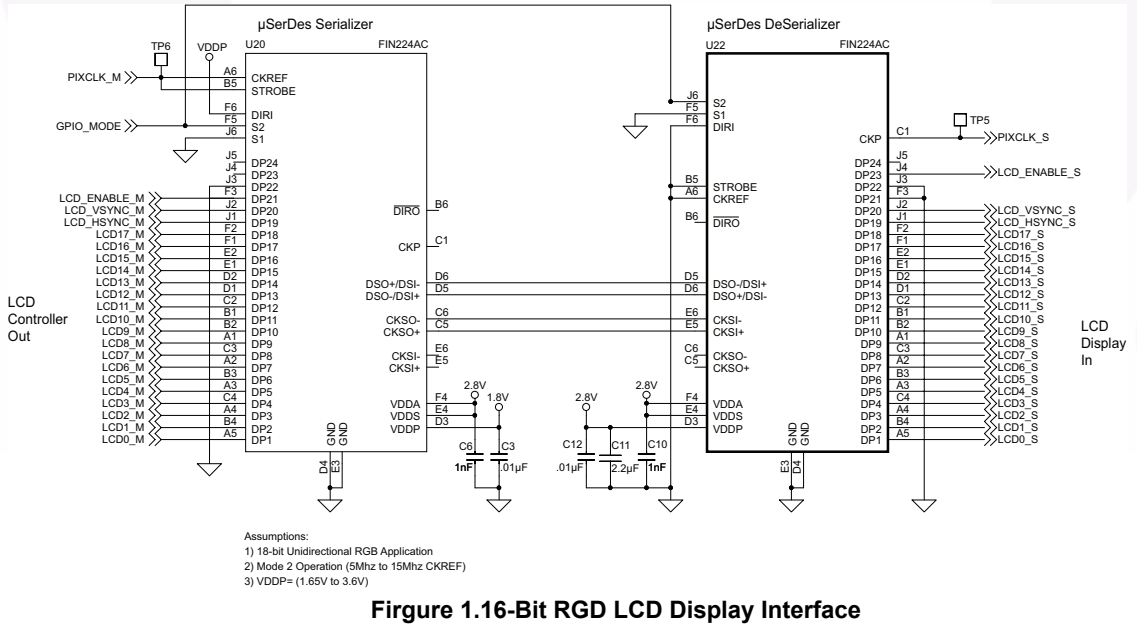
A synchronous pixel interface format is typically made up of n-bits of color data, VSYNC and HSYNC frame and line synchronization signals, and a free-running pixel clock that runs continuously while the display is being updated. Pixel interfaces can be RGB, YUV, or other formats. For the purpose of simplicity, this application note typically refers to an RGB interface, but the information is equally applicable to other formats.

Standard 16- and 18-bit RGB display interfaces can be readily serialized and deserialized through use of the FIN224AC. For 8- and 10-bit RGB and YUV interfaces, the FIN212AC would be a more optimal solution. The FIN224AC has been designed to work synchronously over an input pixel clock frequency range of 2MHz to 26MHz. The FIN212AC can operate between 5MHz and 40MHz. Lower frequencies of operation can be done by over sampling the data or
running in a PLL-bypass mode. Bursting data through the device is also supported. Each of these methods of transferring data is explained below. For simplification purposes, only the FIN224AC is referenced, though the discussion is applicable to the FIN212AC, with minor differences.

Synchronous RGB Display Interface with No Frame Buffer

A standard RGB interface sends data synchronously from the display interface to the actual display. Data runs continuously with one word of data being sent with each pixel clock. A standard RGB interface consists of a bank of data signals used to represent the desired color DATA[0:n], a vertical synchronization signal (VSYNC), a horizontal synchroni-zation signal (HSYNC), and a pixel clock. From the FIN224AC serializer perspective, the DATA, VSYNC, and HSYNC signals are all considered data inputs and all are treated identically. For a 16-bit data interface, an additional four-control signals could also be sent across the interface. When operating in this mode, the LCD interface pixel clock input is used as both the reference clock (CKREF) input and the data strobe (STROBE) input. The CKREF signal is used as the reference signal for the FIN224AC internal PLL. The STROBE signal is used to latch data into the serializer and initiate the serialization sequence.

Figure 1 shows a simple schematic representation of a RGB data interface. Assuming that there are two bits reserved for vertical synchronization and two bits for horizontal synchronization and that the display is being refreshed 60 times per second, the required input clock rate is 4.675MHz (242x322x60). Each frame of data requires 16.67ms to be sent.



Assumptions:
1) 18-bit Unidirectional RGB Application
2) Mode 2 Operation (5Mhz to 15Mhz CKREF)
3) VDDP= (1.65V to 3.6V)

Firgure 1.16-Bit RGD LCD Display Interface

The S2 and S1 pins specify the mode of the PLL for a given input clock frequency, as shown in Table 1. The DIRI pin is used to specify whether the FIN224AC operates as a serializer or a deserializer, as shown in Table 2.

These three control pins are all that need to be specified to control the basic features of the FIN224AC device. For the deserializer to operate, mode 1, 2, or 3 must be selected. No difference in deserializer functionality is observed based on the mode of operation.

Table 1. Frequency Mode Selection of FIN224AC

Mode Number	S2	S1	DIRI	Description
0	0	0	x	Power-Down Mode
1	0	1	1	22-Bit Serializer 2MHz to 5MHz CKREF
	0	1	0	22-Bit Deserializer
2	1	0	1	22-Bit Serializer 5MHz to 15MHz CKREF
	1	0	0	22-Bit Deserializer
3	1	1	1	22-Bit Serializer 10MHz to 26MHz CKREF (Divide by 2 Serial Data) (Note: FIN224C required for RGB applications)
	1	1	0	22-Bit Deserializer

Table 2. Serializer/Deserializer Mode

DIRI	Comments
0	Deserializer
1	Serializer

Powering Up the FIN224AC as a Serializer

The following are the recommended steps in powering up the FIN224AC:

Initial state: DIRI hardwired to a logic HIGH.
S2 = S1 = 0

Step 1: Powering up the device.

The FIN224AC has three power supplies. V_{DDP} is the parallel interface voltage and should match the parallel voltage of the device to which it is connected. V_{DDP} can be any voltage between 1.65V and 3.6V. V_{DDS} is the voltage for the serial I/O and the majority of the digital core logic. V_{DDA} is the supply voltage for the PLL and the bandgap circuitry. V_{DDS} and V_{DDA} should be the same voltage level.

Step 2: Configure the appropriate S1 and S2 pins HIGH.

When S1 and S2 are in the low state, the device is reset and powered down. It is strongly recommended that the device be reset prior to operation. The appropriate PLL dividers and enable circuitry is enabled upon transition to the appropriate mode. For simplicity of system design, it is recommended that the appropriate S1 and S2 pins be connected to the signal used for powering down the system. One such configuration is shown in Figure 1.

Step 3: Start CKREF and wait for the PLL to lock, then apply STROBE signal.

The PLL does not start up until at least two rising edge transitions on CKREF have occurred. Data is not transferred to the serial port until the STROBE signal transitions HIGH. If the STROBE signal begins transitioning prior to the PLL being locked, data transfers should be considered invalid.

Step 4: Begin valid data transfers.

Once the PLL is locked, a valid word is transferred on each rising edge transition of STROBE.

At this point, the serializer is putting out valid data words as long as the STROBE signal is transitioning. One data word is sent for each STROBE signal. The CKREF signal must be a steady repetitive signal for the PLL to continue operating and to remain locked. Figure 2 shows what the DSO and CKSO output waveforms look like when the serializer is sending out correct data.

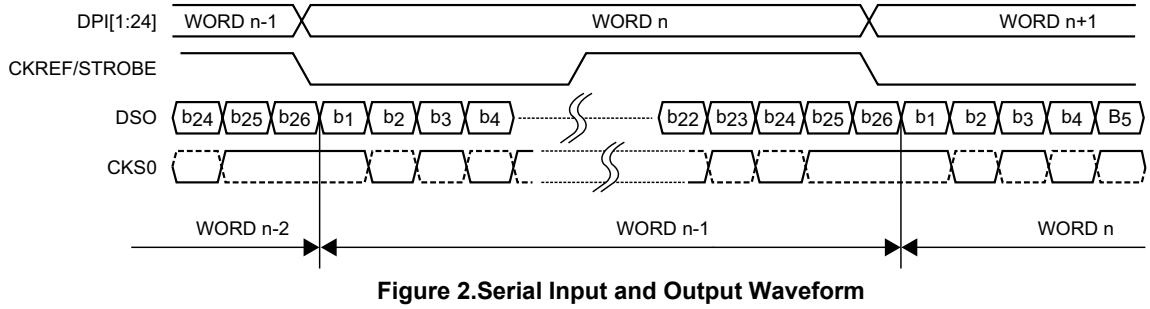


Figure 2.Serial Input and Output Waveform

Powering Up the FIN224AC as a Deserializer

Initial State: DIRI hardwired as a logic LOW.
S2 = S1 = 0.

Step 1: Powering up the device.
The FIN224AC has three power supplies. V_{DDP} is the parallel interface voltage and should match the parallel voltage of the display interface. If the device that is being driven is over-voltage tolerant, V_{DDP} can be greater than the voltage of the display if desired. V_{DDP} can be any voltage between 1.65V and 3.6V. V_{DDS} is the voltage for the serial I/O and the majority of the digital core logic. V_{DDA} supplies power to the bandgap and internal current sources needed for the serial I/Os. Since the PLL is inactive, the PLL is not drawing current. V_{DDS} and V_{DDA} should be the same voltage level.

Step 2: Configure the appropriate S1 and S2 pins HIGH.

When S1 and S2 are in the low state, the device is reset and powered down. It is strongly recommended that the device be reset prior to operation. The specific values of the S1 and S2 signals are not critical for deserializer operation. Any mode other than MODE 0 is valid for deserializer mode. It is recommended that the values of S1 and S2 be set the same as that of the serializer.

These two steps are all that is required to ensure correct operation of the deserializer. As long as the serializer is putting out correct data and clock, the deserializer is operating. The deserializer only outputs a valid word if the serializer has received a STROBE signal.

RGB Display Interface with Buffering

Some LCD display interfaces have a memory buffer that allows data to be burst at a much greater rate than required by the display refresh rate. The FIN224AC can handle this method of transfer by allowing separate control of the CKREF signal and the STROBE signal. The CKREF signal must continually run for the PLL to remain locked. The STROBE signal, however, only needs to be sent when DATA needs to be sent. If no STROBE signal is received, no word is serialized or sent across the serial interface. The serial interface has been designed to ensure that the deserializer never loses a word by sending a word boundary indicator embedded in the data and clock stream. An advantage of this approach is that the serializer and deserializer can be disabled during the non-data period. This conserves dynamic power in a portion of the serializer and serial I/Os.

Two modes of operation need to be considered when working with a buffered interface. The first strobes the data at the same frequency as the CKREF. This mode is nearly identical to the standard RGB interface, except that the STROBE signal is not hardwired to the CKREF signal. No specific phase alignment between CKREF and STROBE is required. The internal working of the serializer handles synchronizing the STROBE signal with the internal bit clock generated by the PLL. Other than the separation of the CKREF and STROBE signal, no difference is required in connecting the FIN224AC as a serializer. The deserializer hook-up can be 100% identical to that of the RGB mode.

The second mode of operation is when CKREF is operating at a faster frequency than the STROBE. This mode does not result in the loss of any data provided that:

$f_{CKREF} \geq 26/23 \times f_{STROBE}$.

For the FIN212AC, $f_{CKREF} \geq 14/11 \times f_{STROBE}$.

When operating in this mode, the average deserializer output period is equal to $1/f_{STROBE}$. The given period of any cycle can vary by $1/13 \times t_{CKREF}$ relative to the previous or subsequent period. The frequency of this bit slip is dependent upon the relative magnitude of the differences in the f_{CKREF} and f_{STROBE}. Because the interface is buffered, this should not cause any issues with the data displayed on the LCD.

PLL-Bypass Mode

If desired, the PLL can be bypassed and a bit-clock can be provided directly to the FIN224AC by connecting a clock source directly to the CKSI signal. Figure 4 illustrates connecting the FIN224AC in PLL-bypass mode. Upon power-up or when coming out of reset mode, the FIN224AC assumes that the CKSI signal is the source of the bit-clock for the serializer. If the CKREF signal transitions two times, the bit-clock source changes to the output of the PLL and the CKSI source is locked out from operating as the bit-clock source until the next reset or power-up condition occurs. For proper operation of the PLL-bypass mode, the CKREF signal should be grounded.

This mode of operation can be useful when operating below the minimum frequency of the PLL. If multiple devices are being used in parallel, a single clock source can be used to drive both of the devices.

When operating in this mode, all of the modes previously described in the previous sections can still operate. The bit-clock frequency provided must be 13x (7x for the FIN212AC) the STROBE frequency for a standard RGB interface. The maximum frequency of bit-clock operation remains 390MHz for the FIN224AC but there is no longer a minimum input frequency restriction.

Source Synchronous Data Transfers

The serial interface transfers data using an edge-aligned, double-data rate clock. The clock signal is aligned to the trailing edge of the data. This allows for a maximum set-up time of approximately one data bit and 0ns hold time. By utilizing a double-data rate clock, the maximum frequency is half that of a standard source synchronous data transfer. Data bits are transferred in on both edges of the serial clock. Odd data bits are transferred on the falling edge of the clock and even data bits are transferred on the rising edge. The deserializer internally slightly skews the data so it is appropriately captured.

For maximum frequency of operation, the alignment of the clock and data signals must be maintained. The skew between the clock and the data signals output by the serializer are typically less than 100ps. Serial interface signal routes need to be the same length so that no significant additional skew is introduced. For operation below the maximum frequency, trace and cable lengths can be mismatched. The longer signal path should always be data. Delaying the data provides more hold time to the signal. For extremely noisy environments or environments where there is a high amount of ISI, this can be used to improve BER if any problems are observed.

Powering Up and Powering Down the FIN224AC

Initially at power-up, the S1 and S2 signals should both be at logic level "0." The three supplies (V_{DDP}, V_{DDS}, V_{DDA}) may be powered up in any order. After the supplies are stable, the proper mode can be applied to the circuit. When in MODE 0 (S1 = S2 = "0"), all internal circuitry is shut off. The parallel inputs are gated off so as to not burn any power even if the signal connected to it is floating. The parallel outputs are 3-STATED and the serial input and outputs are disabled. Additionally all analog circuitry is disabled. MODE 0 should be used for completely powering down the device.

A partial power-down of the serializer is possible by stopping the CKREF signal. For this to work, the PLL must have already been running. Once the CKREF is removed, an internal-state machine detects the lack of CKREF transitions and shuts down the PLL and serial I/O. CKREF can be stopped either HIGH or LOW. The only circuit that remains operational is the bandgap. Leaving the bandgap enable facilitates the PLL starting up gain.

Once CKREF is restarted, the PLL must go through a lock sequence prior to application of STROBE. The lock sequence takes approximately 1000 clock cycles. This time is significantly less than a single frame of display data. The CKREF signal should only be stopped if the re-lock time is not an issue

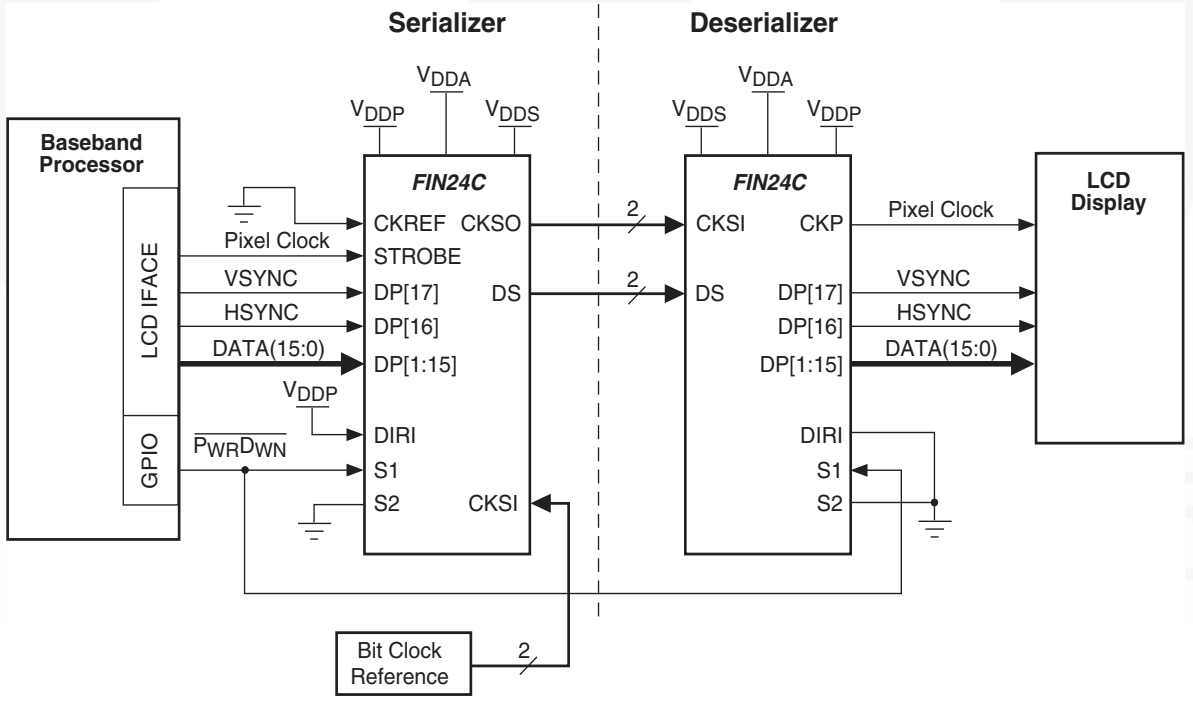


Figure 3.16-Bit RGB PLL-Bypass Mode

Related Datasheets

FIN212AC
FIN24AC
FIN224AC
FIN224C
FIN324C

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