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Bus Switch Undershoot Protection: Which Systems Need this Protection and Why

Bus switches have become commonplace in many system applications. Bus switches are used for bus isolation, bus data exchange and multiplexing. These devices offer low On resistance and use very little system power.

However, bus switches do have a potential drawback. Due to their inherent structure, they are sensitive to negative input and output voltage spikes. These negative voltage transients are referred to as undershoot, and can cause a disabled, or Open, switch to turn On and pass this negative voltage level to the isolated side of the device. This can cause data corruption, and even a system fault. Although bus switches, like most logic families, are equipped with clamping diodes, these diodes are designed primarily for ESD and EOS protection and will not react early enough to protect against a data corrupting undershoot event.

Fortunately the Fairchild Semiconductor FSTU Bus Switch family of switches are offered with the patented undershoot protection circuit (UHC®). The UHC prevents the device from turning On and passing this potentially corrupting negative spike to the isolated circuit. But who needs this type of protection, and in which systems will it be unnecessary? System design plays the largest part in whether a bus switch will see many, or any undershoot events. Designing a system with reduced noise levels offers many advantages, and is a major focus of good design principles. But what if the system designer must design within constraints that force compromises in signal integrity or less than optimum noise margins? Examples of these compromises are systems that use reflected wave design, such as the PCI® bus, or a system that will routinely be subjected to hot insertion and extraction.

Reflected Wave Designs

Reflected wave bus designs rely on the reflected wave generated by an unterminated, or severely under-terminated, line or bus to double the voltage to the level required to switch the bus or line. Figures 1, 2 and Figure 3.

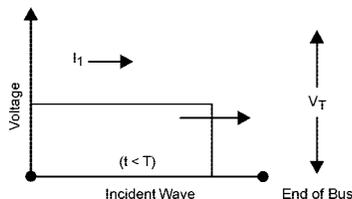


FIGURE 1. The Incident wave travels toward the unterminated bus end. T = delay of the transmission line (bus). t = time of sample. I1 = Incident wave current.

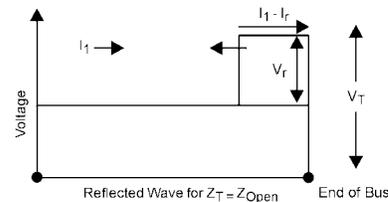


FIGURE 2. When the wave reaches the unterminated end, voltage is doubled and reflected back down the bus, until the entire line reaches the full logic level. This level is held until the line switches LOW, and the cycle is repeated in reverse. It is this HIGH-to-LOW going waveform that may cause an undershoot event to occur.

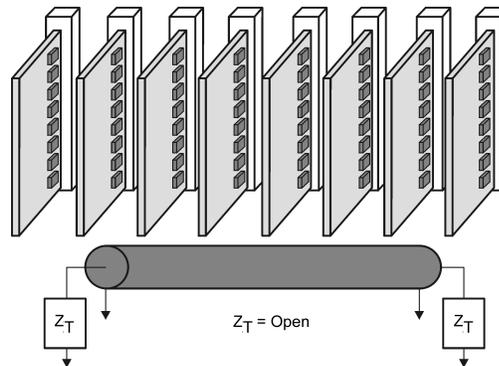


FIGURE 3. Reflected wave bus.

The advantages of this design are its relative simplicity, the low drive current required to switch the bus, and the low impact that the placement and number of plug in cards has on bus signal integrity.

The disadvantages of this design are limited maximum bus switching speed and the potential for large overshoot and undershoot voltage spikes. For example, the PCI® Local Bus Specification [Revision 2.2] states a 5 volt signaling AC waveform worst case specification of +11V and -5.5V (into a 55Ω load).

In a reflected waveform bus environment, not only will a bus switch with UHC prevent data corruption, but can also protect other sensitive components from damage. Memory modules in particular are extremely sensitive to voltage undershoot. Coupling large negative voltage spikes from a noisy bus to a memory module can not only cause data corruption, but also can damage or destroy DRAMs and controllers not designed to dissipate these harsh voltage transients.

Bus Switches for Isolation and Expansion

On a Reflected wave bus, the maximum number of loads needs to be carefully adhered to for proper system operation. For example, a PCI bus has a maximum load allowance of three simultaneous I/O devices. For systems where more flexibility and more I/O is needed, (such as a network server) additional sockets can be added with the use of bus switches. A bus switch multiplexer/demultiplexer allows bus expansion without increasing the simultaneous bus loading. Figure 4. This allows the bus to operate as designed, while isolating unused cards from the bus until the bus controller/arbitrator switches them onto the bus. When one card is connected to the bus, another card is disconnected by use of the multiplexer/demultiplexer. This keeps the bus loading at the specified level, while allowing for greatly increased system flexibility and capacity.

The UHC circuitry ensures that any undershoot generated on the isolated cards, or on the bus, are not coupled through a disabled bus switch.

In a standard PCI environment, all 3 loads are active on the bus and isolation is not necessary. On an expanded bus, it is critical that unused cards are completely isolated from the system. Bus switches with UHC are ideal in accomplishing both the multiplexing and undershoot hardened isolation. This eliminates data corruption or system faults caused by undershoot.

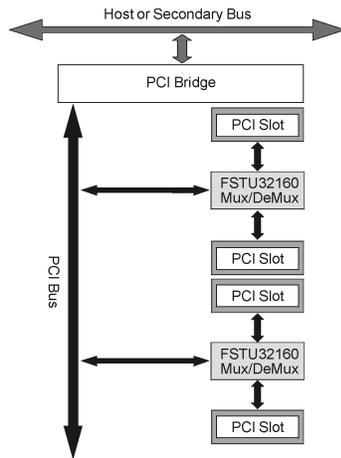


FIGURE 4. A PCI Network Saver bus using FSTU32160 for bus expansion and hot swapping.

Hot Insertion and Extraction

Bus switches can also add benefits to an open system where isolated cards are removed or inserted under system power.

Systems that require hot insertion and extraction have special problems that must be taken into consideration and designed for. When a card is inserted or removed from a system slot, spurious voltage droops and spikes are generated as the card is powered UP or DOWN.

There are design practices that have become commonplace to help eliminate potential data corruption and system faults associated with hot swapping. A common design technique is the use of staggered edge pins on the card,

with the ground plane mated first, followed by the V_{CC} and control pins, with data bus pins mated last. Figure 5. An additional precaution is to ensure that the card is powered up with the off-board drivers in a high impedance (also known as high-Z) state.

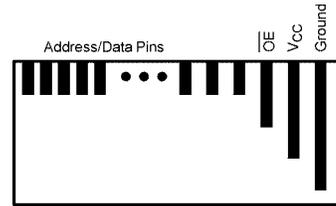


FIGURE 5. Card edge connector with staggered pin heights.

However, during the mating process, the card may quickly cycle back and forth through its minimum operational voltage level several times. This can still generate spurious voltage droops and spikes on the system power lines and card signal lines. These voltage transients can be coupled to the data bus. Additionally, during the insertion or extraction process, and upon its completion, the card introduces an additional capacitive load, with the potential to influence or corrupt system data.

It has become commonplace to use bus switches in this type of application to insure noise and capacitive load isolation during these transition periods. A bus switch with the UHC protection circuit gives additional insurance against negative transient effects during the hot insertion process. This circuitry does not change the DC or AC active performance of the bus switch yet adds a much higher margin of system reliability. Figure 6

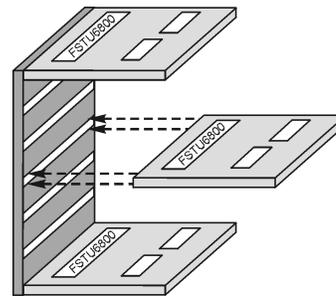


FIGURE 6. Hot insertion cards with FSTU bus switches.

Pre-Charged Outputs and their Additional Benefit

Pre-charged outputs are a feature that compliments undershoot protection, but does not take its place. Even with bus switch isolation, card edge or pin connectors introduce a capacitive load to a bus upon insertion. This added capacitive load disrupts signals running on the bus by diverting current intended to drive the signals instead to charge the capacitive load of these additional pins. This causes voltage spikes and droops, which in turn cause data corruption.

Pre-Charged Outputs and their Additional Benefit (Continued)

Pre-Charged outputs employ a user defined bias voltage ranging from 1.5V to V_{CC} to set the output pin voltage level during high-Z state. The pre-charge voltage is disconnected from the outputs when the device switches out of high-Z. Figure 7

As the device switches from high-Z to active, this biasing action minimizes the current that would be needed to fully charge the pin capacitance to the bus voltage level.

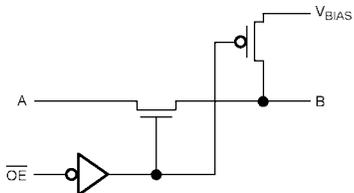


FIGURE 7. Bus Switch Pre-charge circuit

By minimizing these capacitive loading effects on the active bus, signal spikes or droops and noise associated with this capacitive loading change are reduced or eliminated. This reduces the chances of data corruption on an active bus when switching a bus card from high-Z to the active state.

Although pre-charged outputs minimize induced bus noise when a card switches from high-Z to active, they do nothing to guard against voltage spikes or undershoots in an already noisy environment, and will not stop an undershoot

event from being coupled from one bus to another. Bus switches with pre-charge and UHC provide the ideal solution in this type of application.

Summary

Bus switches are in many system applications for bus isolation, bus data exchange and multiplexing. Bus switches offer low On resistance and use little system power. However, they are sensitive to voltage undershoot. Undershoot can cause a disabled, or Open, switch to pass a negative voltage level to an isolated data bus. This can cause data corruption, and even a system fault.

System design plays the largest part in whether a bus switch will experience undershoot events. If a system must be designed within constraints that force compromises in signal integrity and minimum noise margin levels, undershoot events may be frequent. Examples of these compromises are systems that use reflected wave design, or a system that will routinely be subjected to hot insertion and extraction.

A bus switch with the UHC protection circuit prevents undershoots from being coupled onto an isolated bus, preventing data corruption or system faults. In systems with high levels of noise due to reflections or voltage spikes, UHC protection adds a key margin of reliability. In systems routinely subjected to hot insertion events, bus switches with UHC, and pre-charge provide the optimum level of protection.

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