ON Semiconductor

Is Now

Onsemi

To learn more about onsemi[™], please visit our website at <u>www.onsemi.com</u>

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product factures, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and asfety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or by customer's technical experts. onsemi products and actal performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiari



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at <u>www.onsemi.com</u>

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor dates sheds, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor dates sheds and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights of others. ON Semiconductor products are not designed, intended, or authorized for use on similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor and its officers, employees, subsidiaries, affliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out or i, directly or indirectly, any lange of the applicatio customer's to unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the





AN-4174 Board Assembly Guideline for Fairchild Smart Power Stage 5 mm x 5 mm

Introduction

Various components packed in a Power Quad Flat No-Lead (PQFN) package are being used in system power delivery applications today. Fairchild's SPS 5×5 package is an ultra-compact $5 \text{ mm } \times 5 \text{ mm}$ PQFN that offers high efficiency, high power density, and high switching frequency in applications such as synchronous buck DC-DC converters in high-performance computing telecom. A Dual CoolTM package is also offered that allows the component to dissipate heat through both the PCB and its top side.

This application note is designed to provide board assembly guidelines for the SPS 5×5 package. These guidelines include the printed circuit board attributes, design guide, stencil pattern, and assembly process guides.



Figure 1. SPS 5 x 5 Package, Top View

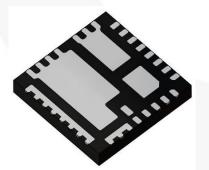


Figure 2. SPS 5 x 5 Package, Bottom View

Board Attributes and Design Guide

Solder Masking and Trace Routing

PQFN devices can be mounted either on Non-Solder Mask Defined (NSMD) or Solder Mask Defined (NSMD) board pads. Comparison of the two pad designs are shown in Figure 3.

- NSMD pad is done by etching the copper pad allowing the solder mask opening to be larger than the copper land geometry.
- SMD pad is defined by a photoimageable mask process which has the mask overlap the edge of the land pad.

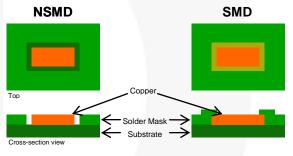


Figure 3. Comparing NSMD and SMD

One advantage for the NSMD pad is its larger solder mask opening. This allows the solder to adhere at the sides of the pad that may improve the reliability of the solder joints. On the other hand, since SMD have much larger pads, it allows more metal for dissipating heat during application. SMD pads also help prevent solder bridging since the mask overlap contains the solder within the solderable pads during reflow.

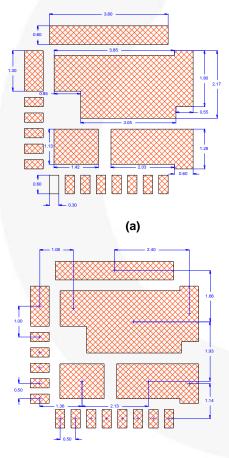
The leads for the SPS 5 x 5 are designed to be in fine pitch layout wherein the distance between leads is 0.25 mm. It is recommended to use the SMD pad design to avoid shorts caused by solder bridging between leads.

Board Surface Finish

The type of board surface finish affects wetting, bond strength, voiding and may also affect reliability. The surface finishes that are typically used in assembly are the Hot-Air Surface Leveling (HASL), Organic Solder Ability Preservative (OSP) and Electroless Nickel Immersion Gold (ENiG). HASL has a superior solder ability characteristic since the wetting of the solder involves merely the coalescence of molten solder with the surface finish which is coated with solder. OSP has excellent flatness that is good for fine pitch packages. ENiG provides very good aging tolerance and has excellent solder ability as well.

ENIG, OSP, HASL or other surfaces finishes may be used for the SPS 5 x 5. There is no specific recommendation for this package; however, the optimum compatibility of the board surface finish to be used and the chosen solder paste must be considered. The ENIG finished board was used for the SPS 5 x 5 board mount evaluations.

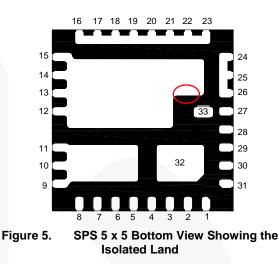
Land Pattern Design



(b)

Figure 4. Recommended Land Pattern Design (a) Pad Dimensions, (b) Distance between Pads

The recommended land pad pattern for SPS 5×5 is shown in Figure 4. Lad pad patterns takes into consideration the tolerances of the PCB fabrication and the component placement during assembly. This tolerance can typically vary up to a maximum of 0.10 mm to avoid misalignment of the mounted component after reflow. The pads for the leads are made to extend from the edge of the package to allow filleting of the solder. The isolated land 33 may not be soldered to avoid solder bridging to its neighboring pad and leads. Solder bridging is more likely to occur when there is larger volume of solder paste.



Board Assembly Considerations by Solder Paste Printing and Reflow Process

Solder Paste

The solder pastes that are commonly used in mounting PQFN packages are the Type 3 and Type 4 pastes with metal loading that ranges from 88% to 90%. The flux material composition of these pastes are classified as rosinbased, low-activity, and halide-free (ROL0) or the no-clean solder paste (usually a ROL0 or ROM0). In mounting the SPS 5 x 5, it is recommended to use a no-clean flux to avoid cleaning trapped flux residues under the package due to the low standoff heights of the solder joints.

Solder pastes are sensitive to storage conditions and exposure time. Using pastes that are beyond its exposure limit may cause issues such as voiding and reliability. It is important to follow the handling and storage recommendations from the solder paste manufacturer.

The most common solder alloys in board mounting assembly are the eutectic 63Sn/37Pb (SnPb) and the 96.5Sn/3.0Ag/0.5Cu (SAC305). The latter is a lead free solder paste alloy of choice for the electronics today. A good choice of solder paste alloy relative to the aperture design of the stencil and board surface finish should be evaluated first to avoid rejects such as solder balling, voiding and wettability issues.

Stencil Aperture and Thickness

The recommended stencil aperture design for the SPS 5 x 5 is shown in Figure 6.

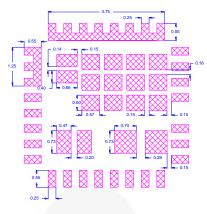


Figure 6. Recommended Stencil Design

The aperture for leads and exposed die pad are relatively smaller than the board pads. The apertures for the exposed pad are about 50 to 60% of the land pad size. The apertures for the leads are smaller than the land pads to balance the thickness of the resulting solder joint from the exposed die pad. The recommended stencil thickness is 0.125 mm.

For the recommended apertures, the aspect and area ratios meet the typical minimum acceptable value for a laser-cut stencil. The formula for the area and aspect ratios according to IPC-7525 "Stencil Design Guidelines" are:

$$Area \ Ratio = \frac{Area \ of \ Pad}{Area \ of \ Aperture \ Walls} > 0.66$$
$$Aspect \ Ratio = \frac{Width \ of \ Aperture}{Thickness \ of \ Stencil \ Foil} > 1.5$$

In board mount assembly, it is important to optimize the coverage of the printed solder paste. An insufficient solder paste print results to misshapen joints which are smaller or partially made joints. Insufficient solder may also cause relatively large voids, however this may also be caused from the surface finish, solder paste alloy and reflow profile, and substrate condition.

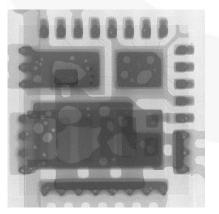


Figure 7. X-ray Showing Large Voids due to Insufficient Solder Paste Printed

On the other hand, too much solder paste printed may cause solder balling around the perimeter of the package or underneath the package especially when the paste used out gases more. This is due to the out gassing of the flux during reflow that pushes the solder out of the pads which results into solder balls. This may also cause solder bridging between exposed pads to and leads.

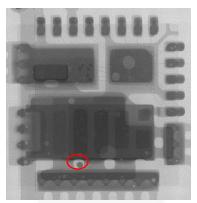


Figure 8. X-ray Showing Solder Ball Underneath the Package

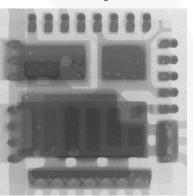


Figure 9. X-ray Showing an Acceptable Condition of Joints and Void Level

Component Placement

Inaccurate placement of the package on the board may lead to poor solder joints thus, mounting the package manually is not recommended. Depending on the placement accuracy of the pick-and-place machine, the PQFN packages can tolerate up to a certain amount of placement offset to have an acceptable solder joint due to its re-aligning behavior. This re-alignment of the package with the board depends on solder pastes. Assembly process and experiments need to be done to confirm the limits of the re-alignment.

Placement pressure must also be considered. Too much pressure exerted on the package may cause the solder to spread too much producing solder balls and bridges during reflow. It is recommended to control the placement height. Some component mounters have the ability to control the height or the amount of bonding force during component placement. This should be characterized to have a sufficient adhesion between the pad and the solder to avoid package fall-off or misalignment during transport from mounter to reflow oven.

Reflow Process and Component Moisture Sensitivity

The assembly should be reflowed according to the recommended temperature profile of the solder paste by its manufacturer. Incorrect temperature profile results to solder quality issues such as relatively large voids, solder balling, package tilt, and uncured solder.

The package should not be exposed to temperatures higher than 260° C. SPS 5 x 5 is tested and qualified to be reliable up to three reflow passes at the maximum reflow peak temperature of 260° C.

Temperature profiling should be done to check that the reflow profile used is correct. This can be done after the oven is turned on or after every profile recipe is changed. Thermocouples are usually used to measure temperatures in the oven. The thermal distribution within the board may vary with different board designs with varying number of components and component sized mounted on it. To ensure that the mounted components are exposed to the correct temperature profile during reflow, it is important to place the thermocouples on areas where the components are mounted. In this way, the temperature to which the components are exposed is monitored.

Guidelines on different reflow methodologies for surfacemount devices are presented in Fairchild's application note AN-7528. It also includes the appropriate temperature profile for each reflow technology and the conditions that may affect the components on board.

The PQFN package is tested to meet moisture sensitivity level 1 at 260°C peak reflow temperature per IPC/JEDEC J-STD-020. Therefore, baking this component prior to assembly is not necessary.

References

- [1] IPC-7093, Design and Assembly Process Implementation for Bottom Termination Components.
- [2] IPC7525, IPC Standard, Stencil Design Guidelines.
- [3] AN-7528 Fairchild Application Note, Guidelines for Soldering Surface Mount Components to PC Boards.
- [4] FSC-QAR-0024, Guideline on the Methodology of Board Level Characterization.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at <u>www.onsemi.com/site/pdf/Patent-Marking.pdf</u>. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor has against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death ass

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5817-1050 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

© Semiconductor Components Industries, LLC