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Interfacing to MM74HC High-Speed CMOS Logic

Fairchild Semiconductor
April 1998



Interfacing to MM74HC High-Speed CMOS Logic

This application note pertains to the VHC Speciality Function devices only (listed in this section of the databook). These devices are direct pin, function and spec replacements for their MM74HC counterparts.

On many occasions it might be necessary to interface MM74HC logic to other types of logic or to some other control circuitry. HC-CMOS can easily be interfaced to any other logic family including 74LS TTL, MM74C, CD4000 CMOS and 10,000 ECL logic. Logic interfacing can be sub-divided into two basic categories: interfacing circuitry operating at the same supply voltage and interfacing to circuitry operating on a different voltage. In the latter case, some logic level translation is usually required, but many easily available circuits simplify this task. Usually, both instances require little or no external circuitry.

Interfacing Between TTL and MM74HC Logic

This high-speed CMOS family can operate from 2–6V, however, in most applications which interface to TTL, both logic families will probably operate off the same 5V TTL supply. The interconnection can be broken down into two categories: TTL outputs driving CMOS inputs, and CMOS outputs driving TTL inputs. In both cases the interface is very simple.

In the first case, TTL driving HC, there are some minor differences in TTL specifications for totem-pole outputs and high-speed CMOS input specifications. The TTL output low level is completely compatible with the MM74HC input low, but TTL outputs are specified to have an output high level of

2.4V (2.7V for LSTTL). High-speed CMOS's logic "1" input level is 3.5V ($V_{CC}=5.0V$), so TTL is not guaranteed to pull a valid CMOS logic "1" level. If the TTL circuit is only driving CMOS, its output voltage is usually about 3.5V. HC-CMOS typically recognizes levels greater than 3V as a logic high, so in most instances TTL can drive MM74HC.

To see why TTL does not pull up further, *Figure 1* shows a typical standard TTL gate's output schematic. As the output pulls up, it can go no higher than two diode voltage drops below V_{CC} due to Q2 and D2. So when operating with a 5V supply, the TTL output cannot go much higher than about 3.5V. *Figure 1* shows an LSTTL gate, which has an output structure formed by Q2 and Q4. As the LSTTL output goes high, these two transistors cannot pull higher than two base-emitter voltage drops below V_{CC} , and, as above, the output cannot go much higher than 3.5V. If the output of either the LSTTL or TTL gate is loaded or the off sink transistor has some collector leakages, the output voltage will be lower.

Many LSTTL and ALSTTL circuits take R2 of *Figure 1* and instead of connecting it to ground, it is connected to the output. This enables the TTL output to go to 4.3V ($V_{CC}=5.0V$) which is more than adequate to drive CMOS. A simple measurement of open circuit V_{OH} can verify this circuit configuration.

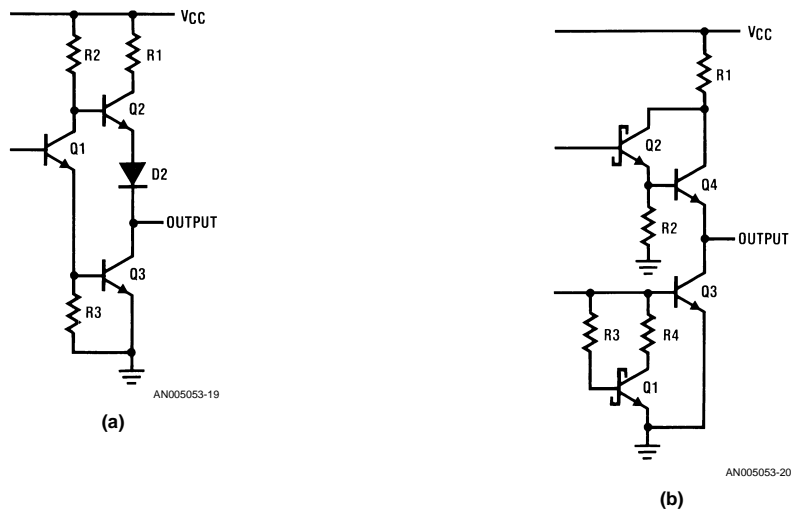


FIGURE 1. Schematic Diagrams for Typical (a) Standard and (b) Low Power Schottky TTL Outputs

Since LSTTL specifications guarantee a 2.7V output high level instead of a 3.5V output high, when designing to the worst case characteristics greater compatibility is sometimes desired. One solution to increase compatibility is to raise the output high level on the TTL output by placing a pull-up resistor from the TTL output to V_{CC} , as shown in *Figure 3*. When the output pulls up, the resistor pulls the voltage very close to V_{CC} . The value of the resistor should be chosen based on the LSTTL and CMOS fanout of the LS gate. *Figure 2* shows the range of pull-up resistors values versus LS fanout that can be used. For example, if an LSTTL device is driving only CMOS circuits, the resistor value is chosen from the left axis which corresponds to a zero LSTTL fanout.

A second solution is to use one of the many MM74HCT TTL input compatible devices. These circuits have a specially designed input circuit that is compatible with TTL logic levels. Their input high level is specified at 2.0V and their input low is 0.8V with $V_{CC}=5.0V\pm 10\%$. Thus LS can be directly connected to HC logic and the extra pull-up resistors can be eliminated. The direct interconnection of the TTL to CMOS translators is shown in *Figure 4*.

If TTL open collector outputs with a pull-up resistor are driving MM74HC logic, there is no interface circuitry needed as the external pull-up will pull the output to a high level very close to V_{CC} . The value of this pull-up for LS gates has the same constraints as the totem-pole outputs and its value can be chosen from *Figure 2* as well. The special TTL to CMOS buffers may also be used in this case, but they are not necessary.

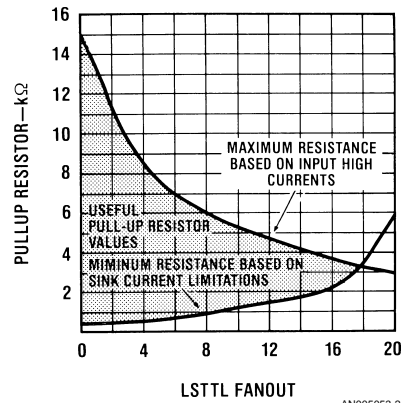


FIGURE 2. Range of Pull-Up Resistors for Low Power Schottky TTL to CMOS Interface

When MM74HC outputs are driving TTL inputs, as shown in *Figure 5*, there is no incompatibility. Both the high and low output voltages are compatible with TTL. The only restriction in high-speed CMOS driving TTL is the same fanout restrictions that apply when TTL is driving TTL.

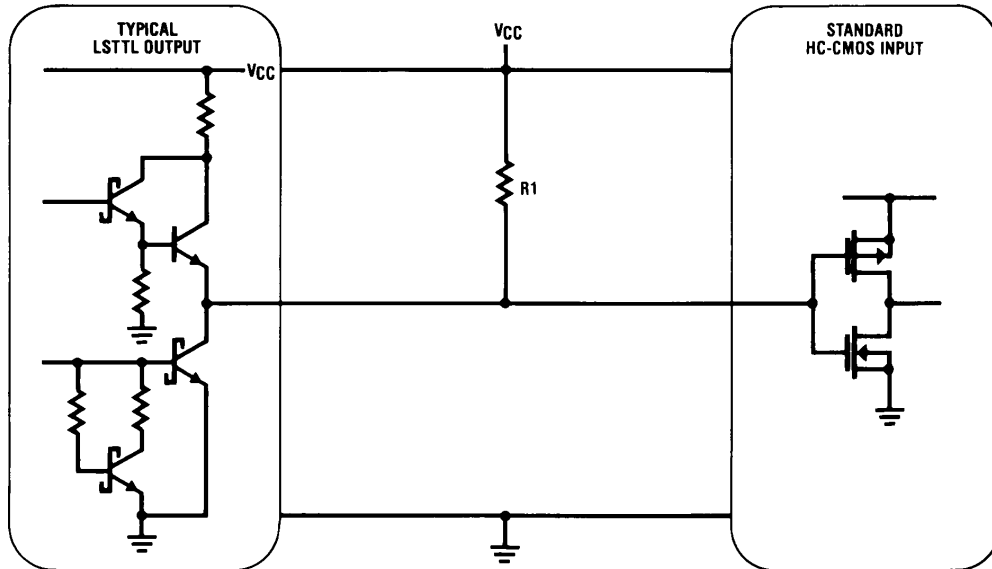


FIGURE 3. Interfacing LSTTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

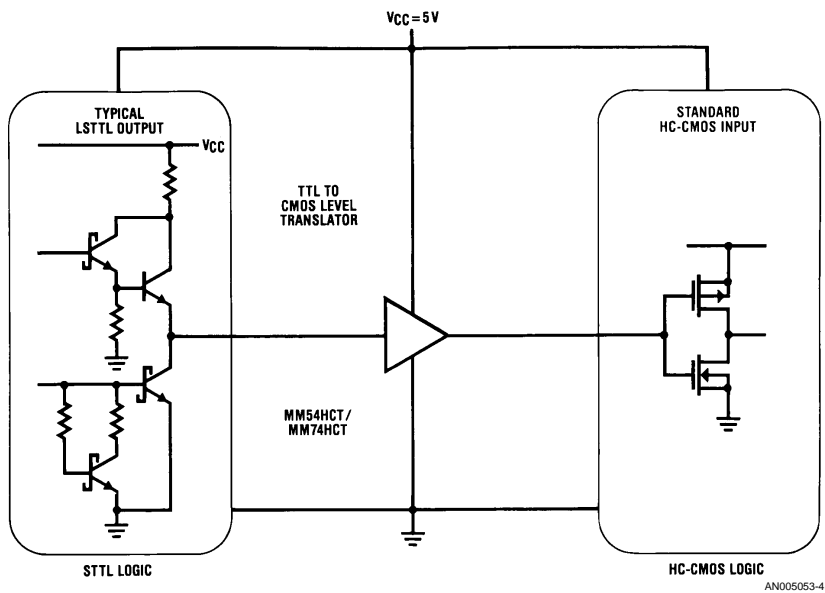


FIGURE 4. LSTTL Outputs Directly Drives MM74HCT Logic Directly Which Can Interface to MM74HC

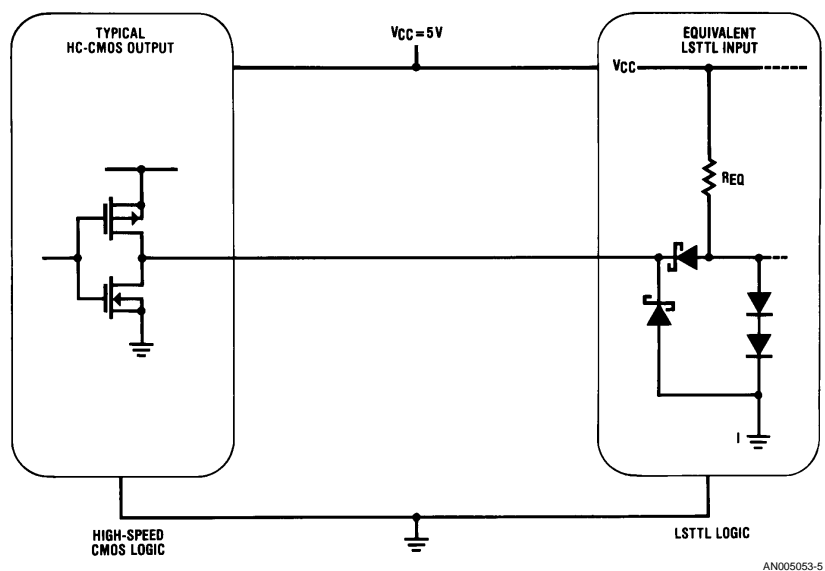


FIGURE 5. High-Speed CMOS Can Directly Connect Up to LSTTL Within its Fanout Restrictions

High-speed CMOS has much improved output drive compared to CD4000 and MM74C metal-gate CMOS logic. *Figure 6* tabulates the fanout capabilities for this family. MM74HC standard outputs have a fanout capability of driving 10 LSTTL equivalent load and MM74HC bus driver outputs can drive up to 15 LSTTL inputs. It is unlikely that greater fanouts will be necessary, but several gates can be paralleled to increase output drive.

MM74HC and NMOS/HMOS Interconnection

With the introduction of CMOS circuits that are speed-equivalent to LSTTL, these fast CMOS devices will replace much of the bipolar support logic for many NMOS and HMOS microprocessor and LSI circuits. As a group, there is no real standard set of input and output specifications, but most NMOS circuits conform to TTL logic input and output logic level specifications.

NMOS outputs will typically pull close to V_{CC} . As with LSTTL, standard MM74HC CMOS inputs will typically accept NMOS outputs directly. However, to improve compatibility the MM74HCT series of TTL compatible circuits may be used. These devices are particularly useful in microprocessor systems, since many of the octal devices are bus oriented and have pin-outs with inputs and outputs on opposite sides of the package. As with LSTTL, a second solution is to add a pull-up resistor between the NMOS output and V_{CC} . Both methods are shown in *Figure 7*.

MM74HC outputs can directly drive NMOS inputs. In fact, this situation is the same as if high-speed CMOS was driving itself. NMOS circuits have near zero input current and usually have input voltage levels that are TTL compatible. Thus MM74HC needs no additional circuitry to drive NMOS and there is also virtually no DC fanout restriction.

Interfacing High-Speed CMOS to MM74C, CD4000 and CMOS-LSI

MM74HC CMOS and metal-gate CMOS logic interconnection is trivial. When both families are operated for the same power supply, no interface circuitry is needed. MM74HC,

CD4000 and MM74C logic families are completely input and output logic level compatible. Since both families have very low input currents, there is essentially no fanout limitations for either family.

The same input and output compatibility of the HC-CMOS makes it also ideal for use interfacing to CMOS-LSI circuits. For example, MM74HC can be directly connected to CMOS microprocessors, as well as CMOS telecommunications products.

MM74HC to ECL Interconnection

There may be some instances where an ECL logic system must be connected to high-speed CMOS logic. There are several possible methods to interconnect these families. *Figure 8* shows one method which uses the 10125/10525 ECL to TTL interface circuit to go from ECL to HC-CMOS logic and the 10124/10524 to connect CMOS outputs to ECL inputs. These devices allow the CMOS to operate with $V_{CC}=5V$ while the ECL circuitry uses a $-5.2V$ supply.

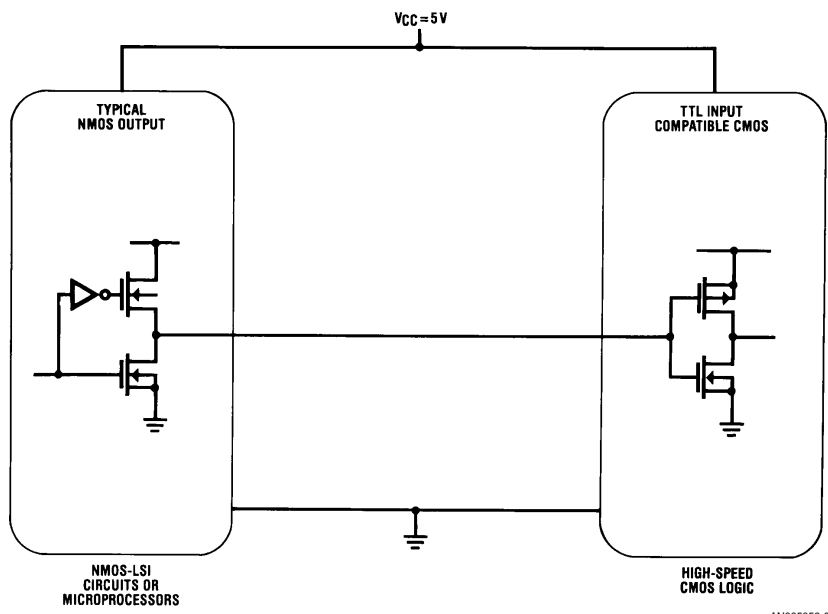
An alternate approach would be to operate the CMOS from the $-5.2V$ ECL supply as shown in *Figure 9*. Thus CMOS outputs could be directly connected to ECL inputs.

Logic Interfaces Requiring Level Translation

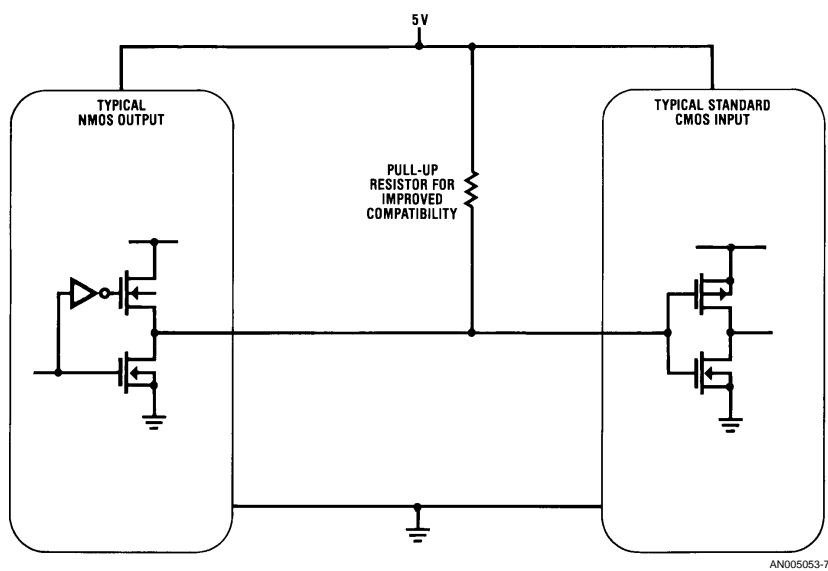
There are many instances when interfacing from one logic family to another that the other logic family will be operating from a different power supply voltage. If this is the case, a level translation must be accomplished. There are many different permutations of up and down level conversions that may be required. A few of the more likely ones are discussed here.

HC-CMOS Equivalent Fanouts	LSTTL		TTL		S-TTL		ALS-TTL	
	Min	Typ	Min	Typ	Min	Typ	Min	Typ
Standard Output MM74HC	10	20	2	4	2	4	20	40
Bus Driver Output MM74HC	15	30	4	8	3	6	30	60

FIGURE 6. Equivalent Fanout Capabilities of High-Speed CMOS Logic

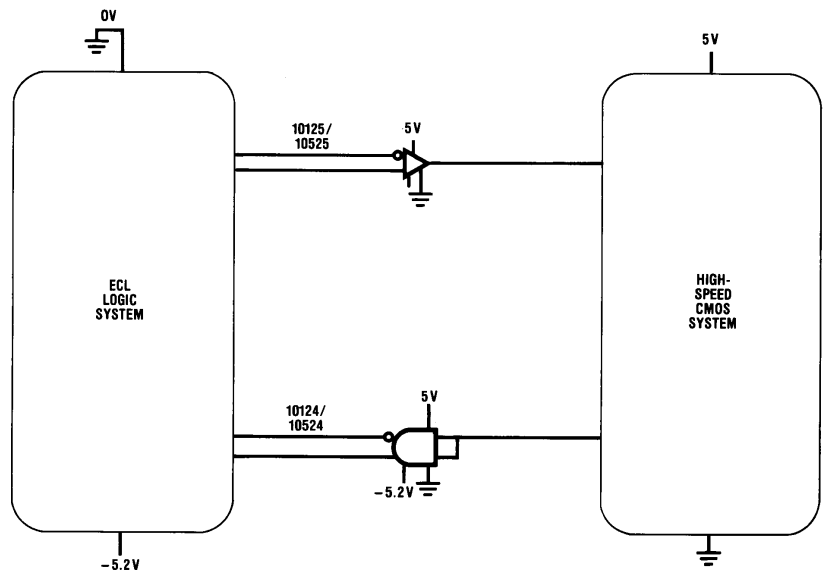


(a)



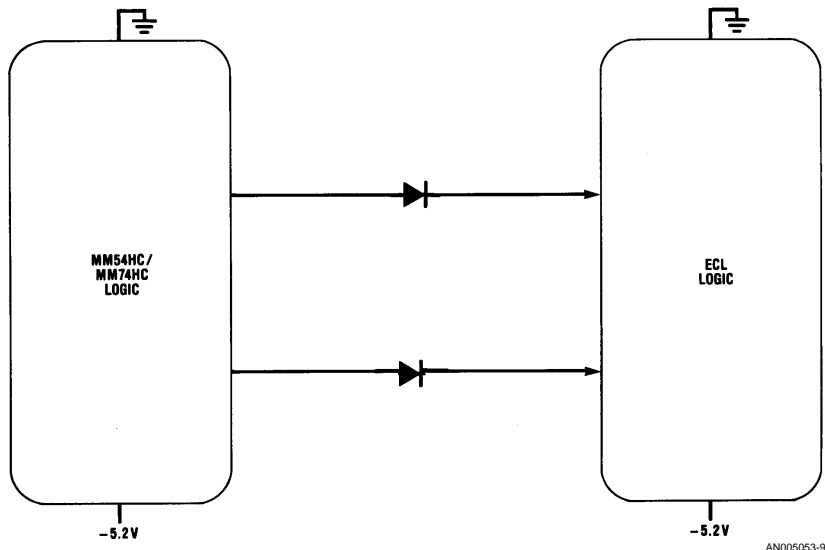
(b)

FIGURE 7. Improved Compatibility NMOS to CMOS Connection Using (a) TTL Input Compatible Devices or (b) External Pull-Up Resistors



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FIGURE 8. MM74HC to ECL and ECL to HC-CMOS Interface



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FIGURE 9. HC-CMOS Driving ECL Logic from Same Power Supply

If MM74HC is operated in a battery back up application for a TTL system, high-speed CMOS may be operated at $V_{CC}=2-3V$ and can be connected to 5V TTL. CMOS operating at 3V can be directly connected to TTL since its input and output levels are compatible with TTL, and the TTL output

levels are compatible with CMOS inputs, as shown in *Figure 10*. When high-speed CMOS is operated at 2V, the TTL outputs will exceed the CMOS power supply and the CMOS outputs will just barely pull high enough to drive TTL, so some level translation will be necessary.

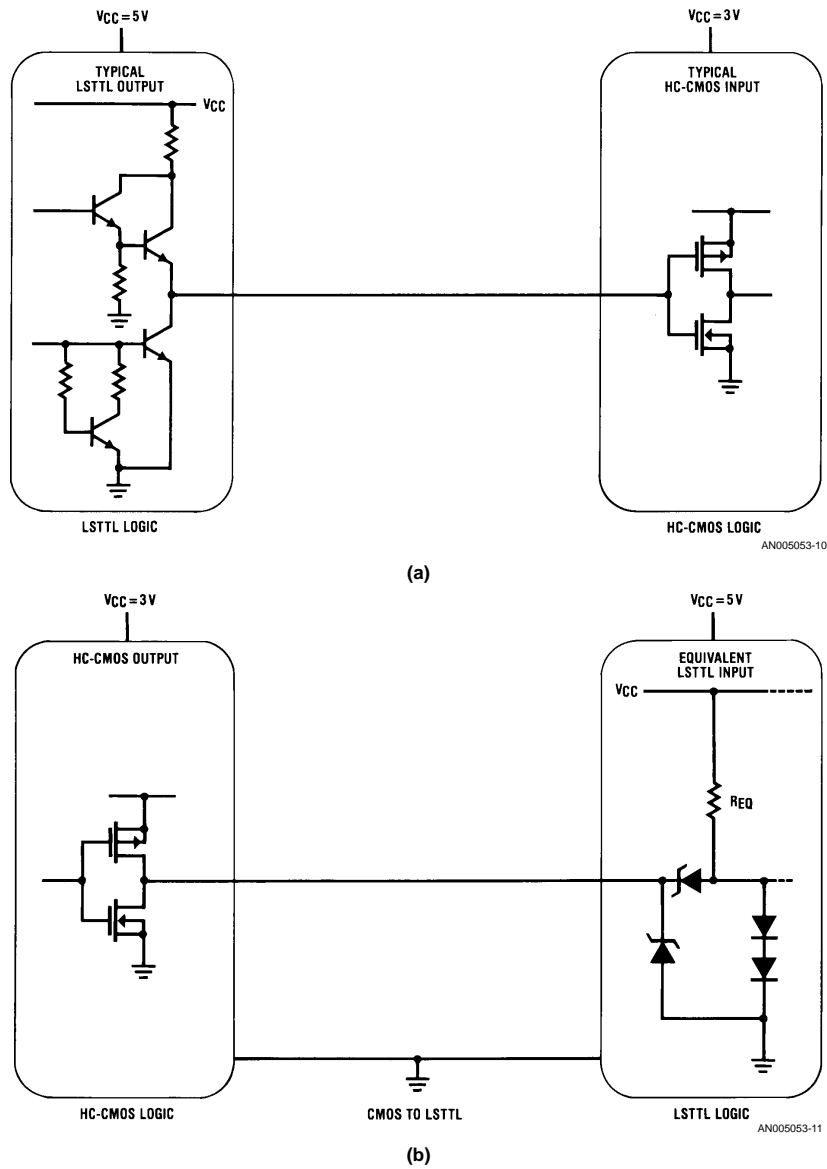
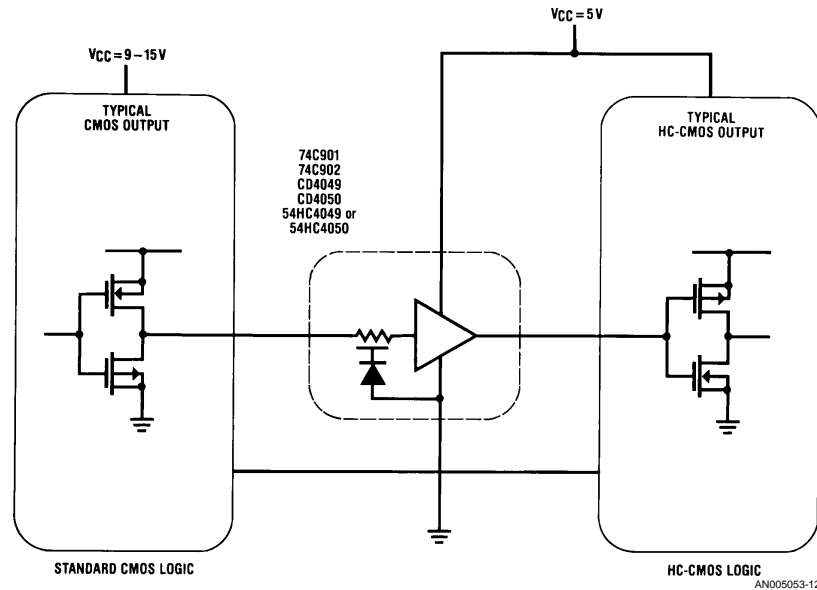


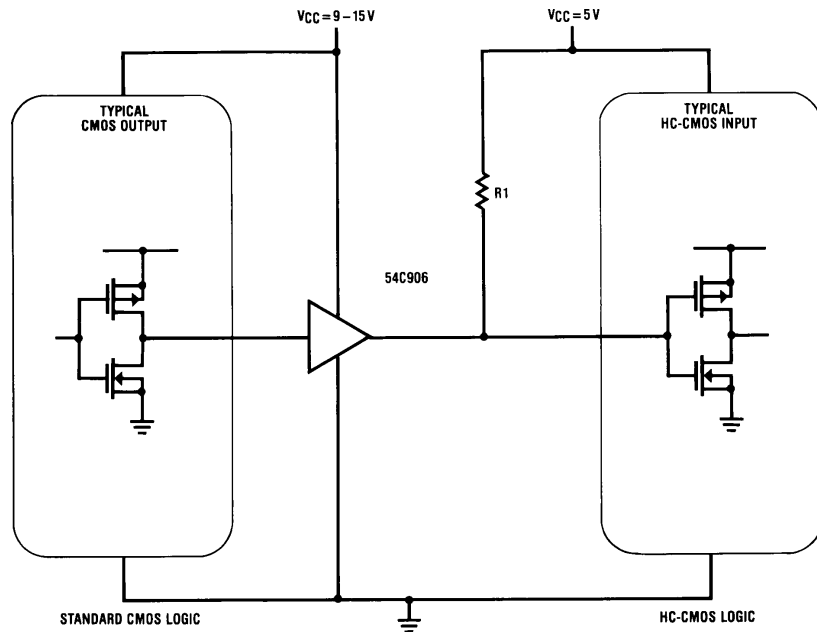
FIGURE 10. When HC-CMOS Is Operating At $V_{CC}=3V$ No Logic Level Conversion Circuitry Is Needed

CD4000 and MM74C metal-gate CMOS logic can be operated over a wider supply range than MM74HC, and because of this there will be instances when metal-gate CMOS and HC-CMOS will be operated off different supply voltages. Usually 9V to 15V CD4000 logic levels

will have to be down converted to 5V high-speed CMOS levels. Figure 11 shows several possible down conversion techniques using a CD4049, CD4050, MM74HC4049, MM74HC4050, or MM74C906.



(a)



(b)

FIGURE 11. CD4000 or 74C Series CMOS to HC-CMOS Connection with Logic Level Conversion Using (a) Special Down Converters or (b) Open Drain CMOS

Since CMOS has a high input impedance, another possibility is to use a resistor voltage divider for down level conversion as shown in *Figure 12*. Voltage dividers will, however, dissipate some power.

Up conversion from MM74HC to metal-gate CMOS can be accomplished as shown in *Figure 13*. Here an MM74C906 open drain buffer with a pull-up resistor tied to the larger power supply is used.

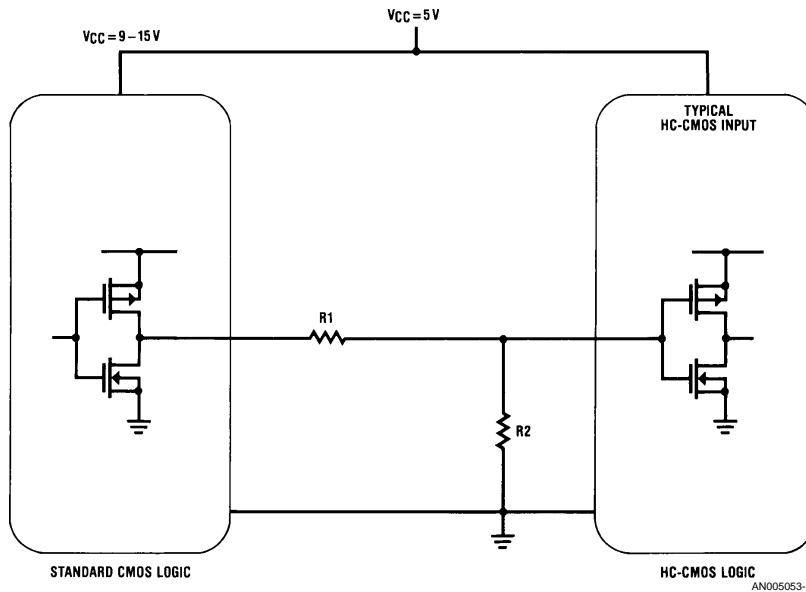


FIGURE 12. CMOS to "HC" CMOS Logic Level Translation Using Resistor Divider

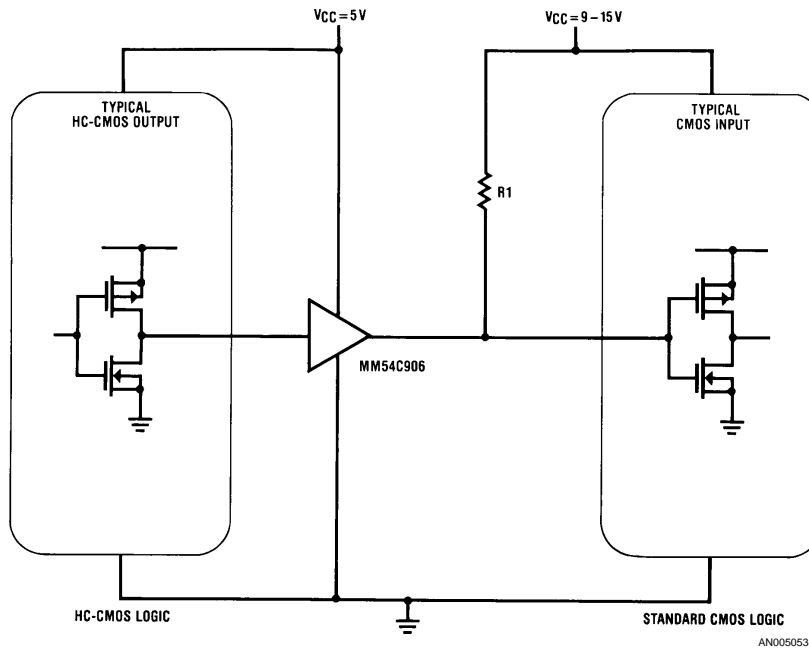


FIGURE 13. HC-CMOS to CD4000 or 74C Series CMOS Connection with Logic Level Conversion Using an Open Drain CMOS Circuit

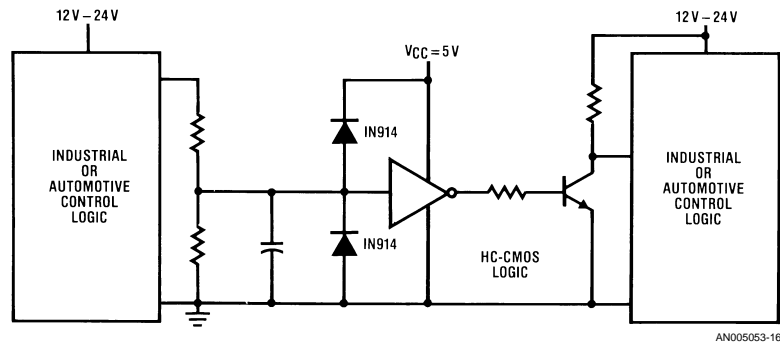


FIGURE 14. Interfacing Between HC-CMOS and High Voltage Control Logic

High Voltage and Industrial Control Interfaces

On occasion, interfacing to industrial and automotive control systems may be necessary. If these systems operate within the metal-gate CMOS supply range, interfacing MM74HC to them is similar to interfacing to CD4000 operating at a higher supply. In rugged industrial environments, care may be required to ensure that large transients do not harm the CMOS logic. Figure 14 shows a typical connection to a high voltage system using diode clamps for input and output protection.

The higher drive of HC-CMOS can enable direct connection to relay circuits, but additional isolation is recommended. Clamp diodes should again be used to prevent spikes generated by the relay from harming the CMOS device. For higher current drive an external transistor may be used to interface to high-speed CMOS. Both of these are shown in Figure 15. Also, the higher drive enables easy connection to SCR's and other power control semiconductors as shown in Figure 16.

Conclusion

Interfacing between different logic families is not at all difficult. In most instances, when no logic level translation between is done, no external circuitry is needed to interconnect logic families. Even though the wide supply range of MM74C and CD4000 creates many possible logic level conversion interface situations, most are easily handled by employing a minimum of extra circuitry. Additionally, several special interface devices also simplify logic level conversion.

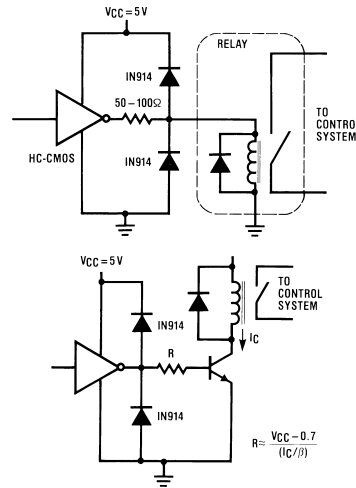


FIGURE 15. Interfacing MM74HC to Relays

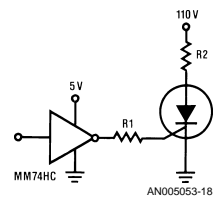


FIGURE 16. MM74HC Driving an SCR



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