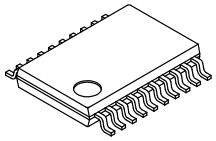
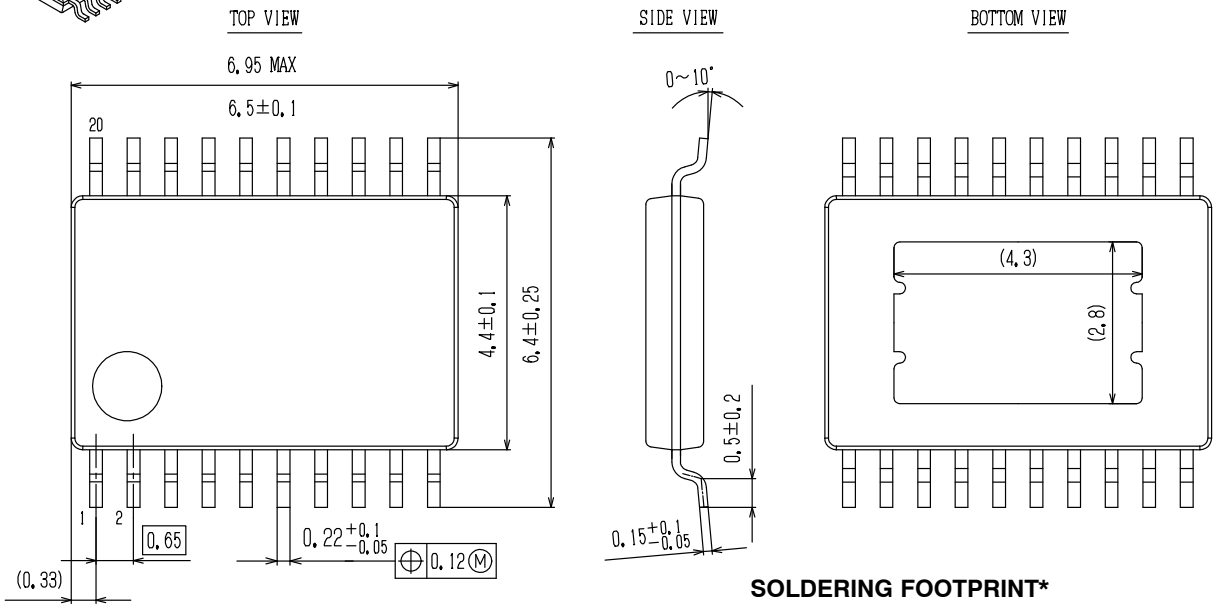
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

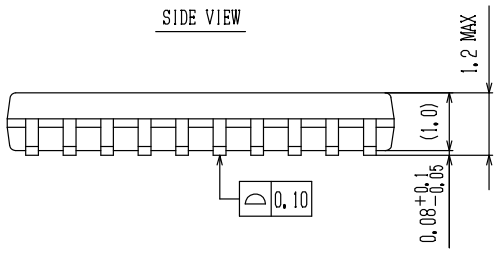
ON Semiconductor®

TSSOP20 4.4x6.5 / TSSOP20J (225 mil)
CASE 948AZ
ISSUE A

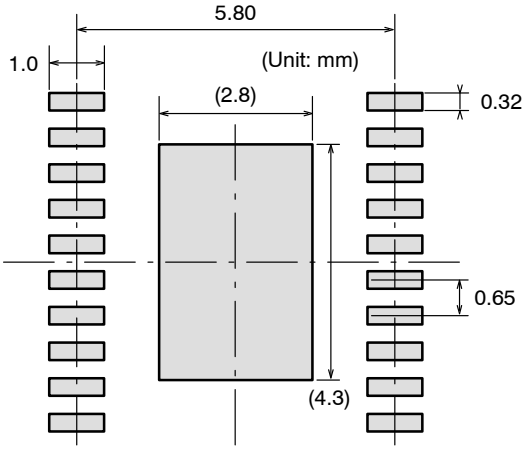
DATE 23 OCT 2013



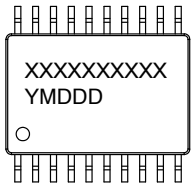




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

NOTES: 1. The measurements are not to guarantee but for reference only.
2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
3. After setting, verification on the product must be done.
(Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through−Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void • gradient • insufficient thickness of soldered joint or bond degradation could lead to IC destruction because thermal conduction to substrate becomes poor.)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**TSSOP20 4.4X6.5 / TSSOP20J (225 MIL)**	**PAGE 1 OF 1**