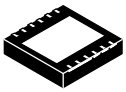
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

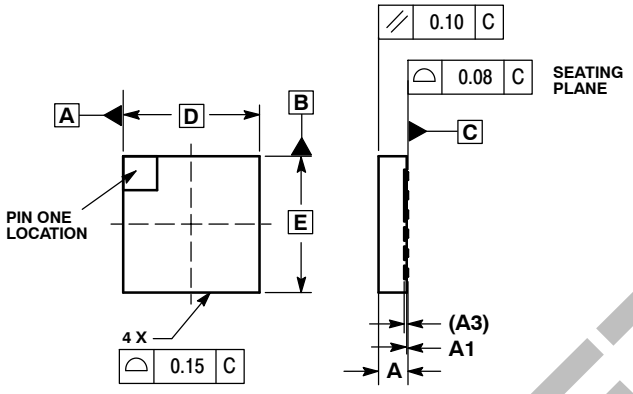
ON Semiconductor®

PLLP–12, 9x9 mm
CASE 488AB
ISSUE D

DATE 18 NOV 2019



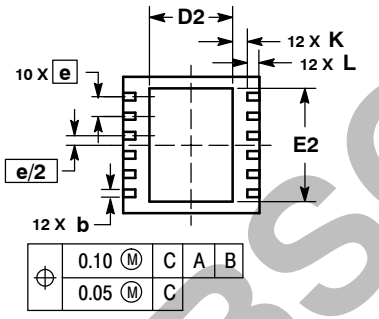
SCALE 1:1



TOP VIEW SIDE VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE LEAD, DIMENSION B, AND EXPOSED PAD.

DIM	MILLIMETERS MIN	MAX
A	1.750	1.950
A1	0.000	0.050
A3	0.254 REF	
b	0.400	0.600
D	9.000 BSC	
E	9.000 BSC	
e	1.270 BSC	
D2	5.400	5.600
E2	7.400	7.600
K	0.850 REF	
L	0.850	0.950



BOTTOM VIEW

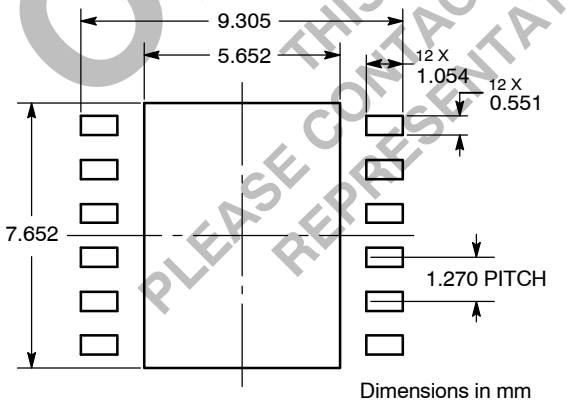
GENERIC MARKING DIAGRAM*

xxxxxxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. OVLO
2. UVLO
3. ENABLE/TIMER
4. GND
5. CCHARGE
6. CURRENT LIMIT
7. POWER GOOD
8. N/C
9. N/C
10. SOURCE
11. SOURCE
12. SOURCE

SOLDERING FOOTPRINT*



Dimensions in mm

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**PLLP–12, 9*9 MM, SMART HOTPLUG**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY P. CELAYA.	01 MAR 2004
A	CHANGED TITLE OF CASE TO 12 PIN PLLP. REQ. BY S. CHANG.	03 FEB 2005
B	CHANGED DIMS A3, K AND L. ADDED STYLE 1. REQ. BY S. CHANG.	28 APR 2005
C	ADDED SOLDERING FOOTPRINT. REQ. BY S. CHANG.	18 JUL 2005

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