交错式功率因数校正
Interleaved PFC
Agenda

- Introduction:
  - Basics of interleaving
  - Main benefits

- NCP1631: a novel controller for interleaved PFC
  - Out-of-phase management
  - The NCP1631 allows the use of smaller inductors
  - Main functions

- Experimental results and performance
  - General waveforms
  - Efficiency

- Summary
交错式功率因数校正(PFC) Interleaved PFC

- 以两个功率为$(P_{in(avg)}/2)$的较小PFC段替代单个较大PFC段
- Two small PFC stages delivering $(P_{in(avg)}/2)$ in lieu of a single big one

- 如果两个相位异相，因此产生的电流$(I_{L(tot)}$)和$(I_{D(tot)})$纹波大幅减小
- If the two phases are out-of-phase, the resulting currents $(I_{L(tot)})$ and $(I_{D(tot)})$ exhibit a dramatically reduced ripple.
交错式PFC优势 Interleaved Benefits

- More components but:
  - 150 W PFC比300 W PFC更易于设计 A 150-W PFC is easier to design than a 300-W one
  - 模块化途径 Modular approach
  - 散热更好 Better heating distribution
  - 扩展临界导电模式(CrM)范围 Extended range for Critical Conduction Mode (CrM)
  - 元件尺寸更小，支持纤薄设计 Smaller components
    (帮助符合严格的外形因数需求，如平板电视 help meet strict form factor needs – e.g., flat panels)
  - 两个不连续导电模式(DCM) PFC看上去象一个连续导电模式(CCM) PFC转换器 Two DCM PFCs look like a CCM PFC converter...
    - 简化电磁干扰(EMI)滤波，减小输出均方根(rms)电流 Eases EMI filtering and reduces the output rms current
什么是 $I_{L(tot)}$ 总输入电流纹波？
What is the ripple of the $I_{L(tot)}$ total input current?

什么是 $I_{D(tot)}$ 总输出电流纹波？
What is the ripple of the $I_{D(tot)}$ total output current?
低交流线路时的输入电流纹波
Input Current Ripple at Low Line

当输入电压保持低于输出电压的一半时，输入电流看上去像CCM滞后PFC的输入电流。When \( V_{in} \) remains lower than \( V_{out}/2 \), the input current looks like that of a CCM, hysteretic PFC.

\((I_{L(tot)})\)在两个接近的正弦迹线间摆动。\((I_{L(tot)})\) swings between two nearly sinusoidal envelops.
高交流线路时的输入电流纹波
Input Current Ripple at High Line

输入电压超过输出电压的一半时，谷底电流保持恒定！
When $V_{in}$ exceeds ($V_{out}$/2), the valley current is constant!

此电流等于

$$I_{in(t)} = \frac{V_{out}}{2 \cdot R_{in}}$$

其中，$R_{in}$ 是 PFC 输入阻抗

where $R_{in}$ is the PFC input impedance

$V_{in} = V_{out}/2$ 时
无纹波
No ripple when $V_{in} = V_{out}/2$

$$P_{in(avg).V_{out}} = \frac{V_{out}}{2 \cdot R_{in}}$$

$$\frac{P_{in(avg).V_{out}}}{2 \cdot V_{in(rms)}^2}$$
交流线路输入电流  Line Input Current

对于每个支路而言，正弦波的某处波形有如：  
For each branch, somewhere within the sinusoid:

\[ I_{L1} \]

\[ 2 \cdot \langle I_{L1} \rangle_{T_{sw}} \]

两个平均正弦相位电流之和得到总线电流：  
The sum of the two averaged, sinusoidal phases currents gives the total line current:

\[ I_{in} = \left\langle I_{L(tot)} \right\rangle_{T_{sw}} = \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}} \]

假定有极佳的电流平衡：  
Assuming a perfect current balancing:

\[ 2 \cdot \langle I_{L1} \rangle_{T_{sw}} = 2 \cdot \langle I_{L2} \rangle_{T_{sw}} = I_{in} \]

每个支路的峰值电流就是 \( I_{in}(t) \)：  
The peak current in each branch is \( I_{in}(t) \)
The refueling current (output diode(s) current) depends on the mode:

- **Phase 1**
- **Phase 2**

### Single phase CCM

- **Single phase CCM**
- **Single phase CrM**
- **Interleaved CrM**

**Rms value over** $T_{sw}$

\[ I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}} \]

\[ \frac{2}{\sqrt{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}} \]

\[ \sqrt{\frac{2}{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}} \]
大电容均方根电流降低

* A Reduced Rms Current in the Bulk Capacitor *

正弦电流积分可得到 (电阻型负载)：Integration over the sinusoid leads to (resistive load):

<table>
<thead>
<tr>
<th>二极管均方根电流 (ID(rms))</th>
<th>Capacitor rms current (IC(rms))</th>
<th>300-W, Vout = 390 V, Vin(rms) = 90 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \sqrt{\frac{8}{3} \cdot \left( \frac{P_{out}}{\eta} \right)^2} ]</td>
<td>[ \sqrt{\frac{8}{3} \cdot \left( \frac{P_{out}}{\eta} \right)^2} ]</td>
<td>[ \sqrt{\frac{2}{3} \cdot \left( \frac{P_{out}}{\eta} \right)^2} ]</td>
</tr>
<tr>
<td>1.9 A</td>
<td>1.7 A</td>
<td>2.2 A</td>
</tr>
</tbody>
</table>

交错式CrM或FCCrM*大幅降低均方根电流

Interleaving dramatically reduces the rms currents

降低损耗，减少发热量，提升可靠性 reduced losses, lower heating, increased reliability

* 频率钳位CrM Frequency Clamped CrM
交错式PFC小结 Finally…

交错式PFC结合了 Interleaved PFC combines:

- 临界导电模式(CrM)工作的优势 The advantages of CrM operations
  - 不需要低反向恢复时间(trr)二极管 No need for low trr diode
  - 高能效 High efficiency
- 降低输入电流纹波，将大电容中均方根电流减至最小 A reduced input current ripple and a minimized rms current in the bulk capacitor
- 散热更好 A better distribution of heating

元器件数量更多，但尺寸“较小” More components but “small” ones

热心调配，适合纤薄外形因数应用，如笔记本适配器和液晶电视 Well adapted to slim form factor applications such as notebook adapters and LCD TVs

更多信息参见安森美半导体应用笔记AND8355 Refer to application note AND8355 for more details
议程 Agenda

- 简介 Introduction:
  - 交错式PFC基础知识 Basics of interleaving
  - 主要优势 Main benefits

- NCP1631：新颖的交错式PFC控制器 NCP1631: a novel controller for interleaved PFC
  - 异相管理 Out-of-phase management
  - NCP1631支持使用较小电感 The NCP1631 allows the use of smaller inductors
  - 主要功能 Main functions

- 实验结果及性能 Experimental results and performance
  - 一般波形 General waveforms
  - 能效 Efficiency

- 总结 Summary
NCP1631概览  NCP1631 Overview

- 交错式2相PFC控制器  Interleaved, 2-phase PFC controller

- 频率钳位临界导电模式(\textbf{FCCrM})优化完整负载范围内的能效
  Frequency Clamped Critical conduction Mode (\textbf{FCCrM}) to optimize the efficiency over the load range.

- 包括启动、过流保护(OCP)或瞬态序列在内的所有条件下提供稳固的异相工作
  Substantial out-of-phase operation in all conditions including start-up, OCP or transient sequences.

- 具备前馈，改善环路补偿
  Feedforward for improved loop compensation

- 简化下行转换器设计
  Eased design of the downstream converter:
  - 提供“pfcOK”信号，含动态响应增强器及待机管理功能
    pfcOK, dynamic response enhancer, standby management

- 高保护等级
  High protection level:
  - 输入欠压保护，精确的1引脚限流，浪涌电流检测，单独引脚用于(可编程)过压保护(OVP)等
    Brown-out protection, accurate 1-pin current limitation, in-rush currents detection, separate pin for (programmable) OVP...
NCP1631 Overview

- Interleaved, 2-phase PFC controller

- Zero voltage detection (branch1)
- Zero voltage detection (branch2)

- Latch input: if $V_{Latch} > 2.5$ V, the controller shuts down

- One CS pin to sense the total input current for Over-Current Protection and Inrush detection

- Over and Under voltage protection (OVP, UVP)

- Brown-out detection with a 50-ms blanking delay to meet hold-up time requirements

- Adjusts the frequency foldback characteristic

- Adjusts the regulation loop bandwidth

- DCC2
- DCC1
- RE5V / pfcOK
- DRV1
- DRV2
- GND
- CS
- BO
- FOLD
- Vcc
- Vcontrol
- OSC
- Ref
- Rt
- FB
- OVP / UVP

- Interleaved, 2-phase PFC controller

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- Over and Under voltage protection (OVP, UVP)
NCP1631 Typical Application

Synchronization of phases is completely internal

提示下行转换器PFC已经就绪 Indicates the downstream converter that the PFC is ready

单个电流感测电阻 1 current sense resistor

完全内部实现相位同步 Synchronization of phases is completely internal
交错式PFC：主/从方案
Interleaving: Master / Slave Approach…

- 主支路自由工作  The master branch operates freely
- 从支路以180°相移跟随主支路工作  The slave follows with a 180° phase shift
- 主要挑战：维持CrM工作（无CCM，无死区时间） Main challenge: maintaining the CrM operation (no CCM, no dead-time)

\[ L_2 < L_1 \]

电流模式：电感不平衡
Current mode: inductor unbalance

电压模式：导通时间转换
Voltage mode: on-time shift
交错式PFC：交互作用相位方案

Interleaving: Interactive-Phase Approach...

- 每个相位都恰当地工作在CrM Each phase properly operates in CrM
- 两个相位交互作用，设定180°的相移 The two branches interact to set the 180° phase shift
- 主要挑战：保持恰当的相移 Main challenge: to keep the proper phase shift

其中一个相位的导通时间扰动 On-time perturbation for one phase

维持了CrM工作，但导通时间扰动可能会让180°相移减弱
CrM operation is maintained but a perturbation of the on-time may degrade the 180° phase shift

我们选择的是这种方案 We selected this approach
交错式管理 Interleaving Management

- 振荡器管理异相工作 The oscillator manages the out-of-phase operation
- 振荡器充当交错式时钟产生器 It acts as the interleaved clocks generator

Diagram: 5 V and 4 V signals in CRM and DCM operations.
电流平衡

NCP1631采用电压模式工作

两个支路的导通时间相同，故开关周期也相同

电感不平衡

电感不平衡

不影响开关周期

仅导致每个支路转换的功率数量有差别

两个支路仍保持同步

保持临界导电模式(CrM)工作(或FCCrM)

180°相移没有改变
人为制造不平衡 Artificial Unbalancing

- 在测试中，采用300 µH的线圈来替代支路1中的150 µH电感
  In this test, the 150-µH inductor of branch 1 is replaced by a 300-µH coil !!!!

- 因此，支路2消耗更多电流，且支路2中的MOSFET(通常)更热
  Hence, more current is drawn by branch2 and MOSFET of branch2 is (normally) hotter

- 后面的图中显示PFC段在这些极端条件及满载下的工作特性
  The following plots show how the PFC stage behaves in these extreme conditions and full load
Still Operates in a Robust Manner…

120 Vrms, 0.8 A  
(PF = 0.997, THD = 6%)

230 Vrms, 0.8 A  
(PF = 0.980, THD = 11%)

I_in (5 A/div)  
I_line (5 A/div)

OSC pin voltage (5 V/div)  
I_in (5 A/div)
Switching Frequency Variations in CrM

- Normalized $f_{sw}$ variations within the ac line sinusoid ($V_{in,rms} = 90$ V, $V_{out} = 400$ V)
- Normalized $f_{sw}$ (at the sinusoid top) vs $V_{in,rms}$
- $f_{sw}$ becomes high at light load, leading to large switching losses
- $f_{sw}$ should be limited
Limiting $f_{sw}$ to Optimize the Efficiency

At the top of the sinusoid:

$$
\frac{f_{sw}}{V_{out}} = \frac{V_{in, pk}^2}{4 \cdot L \cdot P_{in, avg} \cdot \left(1 - \frac{V_{in, pk}}{V_{out}}\right)}
$$

CrM operation requires large inductors to limit the switching losses at light load.

Can’t we clamp $f_{sw}$ not to over-dimension L?

Frequency Clamped Critical conduction Mode (FCCrM)
Frequency Clamped Critical Conduction Mode

- At light load, the current cycle is short.
- When shorter than the oscillator period, no new cycle until the oscillator period is elapsed.
- On-times are increased to compensate the dead-times.
- No PF degradation.
NCP1631 Operation - FCCrM

- In FCCrM, the switching frequency is clamped:
  - Fixed frequency in light load mode and near the line zero crossing
  - Critical conduction mode (CrM) achieved at full load.

- FCCrM optimizes the efficiency over the load range.

- FCCrM reduces the range of frequencies to be filtered (EMI).

- FCCrM allows the use of smaller inductors

  - No need for large inductances to limit the frequency range!
  - E.g., 150 µH (PQ2620) for a wide mains 300-W application

- Frequency foldback reduces the clamp frequency at light load to further improve the efficiency.
NCP1631频率反走 NCP1631 Frequency Foldback

- 输入功率减小到低于预设功率电平(P_{LL})时，钳位频率线性降低 The clamp frequency linearly decays when P_{in} goes below a preset level (P_{LL})

- P_{LL}由引脚6电阻设定 P_{LL} is programmed by the pin6 resistor

示例：40%负载及130 kHz额定频率时的频率反走
Example: FF at 40% load and a 130-kHz nominal frequency

- 钳位频率逐渐减小 Gradual decay of the clamp frequency
- 工作不间断 No discontinuity in the operation
- 振荡器电容两端的电阻设定最低钳位频率(如20 kHz，参见应用笔记AND8407) A resistor across the oscillator capacitor sets a minimum clamp frequency (e.g., 20 kHz - see application note AND8407)

- 引脚6的输出电压正比于功率。I_{FF}电流钳位至105 µA，用于给振荡器电容充电及放电 Pin 6 pins out a voltage proportional to the power. The I_{FF} current is clamped to 105µA and used to charge and discharge the oscillator capacitor

\[ \frac{(P_{in})_{FF}}{(P_{in})_{HL}} = \frac{R_{pin6} \cdot 105 \, \mu A}{1.66} \approx \frac{R_{pin6}}{15810} \]
轻载工作  Light Load Operation

轻载时频率减小  Frequency is reduced at light load
采用深度DCM工作，减小开关损耗
Heavy DCM operation to reduce the switching losses

死区时间  Dead-time

重负载条件下的CrM工作
CrM at heavy load conditions
## 空载能耗 No Load Consumption

<table>
<thead>
<tr>
<th>条件 Conditions</th>
<th>交流线路电压 Line Voltage (V)</th>
<th>输入能耗 Input Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Frequency Foldback (pin6 grounded)</td>
<td>115</td>
<td>107</td>
</tr>
<tr>
<td>2 separate $V_{out}$ sensing networks for FB and OVP for a total 185-µA leakage on the $V_{out}$ rail</td>
<td>230</td>
<td>138</td>
</tr>
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<td>Frequency Foldback ($R_{FF} = 4.7$ kΩ)</td>
<td>115</td>
<td>96</td>
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<td>230</td>
<td>134</td>
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<td>Frequency Foldback ($R_{FF} = 4.7$ kΩ)</td>
<td>115</td>
<td>38</td>
</tr>
<tr>
<td>one $V_{out}$ sensing network for FB and OVP for a total 48-µA leakage on the $V_{out}$ rail</td>
<td>230</td>
<td>82</td>
</tr>
</tbody>
</table>

- 数据系在300 W NCP1631演示板在测得 Measured on the 300-W NCP1631 demoboard
- 外部$V_{CC}$、3颗680 kΩ电阻给X2电容放电 External $V_{cc}$, 3 * 680-kΩ resistors to discharge the X2 capacitors
- 频率反走技术不仅提升轻载能效，还提升空载条件下的能效 Frequency Foldback improves the efficiency in light load but also in no-load conditions

(*)默认演示板配置 Default demoboard configuration
**NCP1631 故障管理**  NCP1631 Fault Management

输入欠压  Brown-out
欠压保护  Undervoltage protection
闩锁条件  Latch-off condition
晶圆过热  Die overtemperature
提升Vcc工作电平  Improper Vcc level for operation
Rt引脚提供的电流太小  Too low current sourced by the Rt pin

在关闭模式，电路主要元件休眠，能耗极低：< 500 µA
In OFF mode, the major part of the circuit sleeps and consumption is minimized to < 500 µA
**NCP1631 Over Current Protection (OCP)**

1) **NCP1631** monitors a negative voltage, $V_{CS}$, proportional to the current drawn by both interleaved branches, $I_{in}$.

2) $I_{CS}$ current maintains 0 V on CS pin.

$$-(R_{CS} \cdot I_{in}) + (R_{OCP} \cdot I_{CS}) = 0 \implies I_{CS} = \frac{R_{CS}}{R_{OCP}} \cdot I_{in}$$

3) If $I_{CS}$ exceeds 210 µA, OCP is triggered.

- **自由选择** $R_{CS}$ (最优) Select $R_{CS}$ freely (optimally)
- **$R_{OCP}$** 设定限流 $R_{OCP}$ sets the current limit
- **$R_{CS}$** 损耗极低 Minimized losses in $R_{CS}$
NCP1631 Overcurrent Protection

When \( I_{CS} > 210 \, \mu A \), the OCP switch closes and a current equal to \( 0.5 \times (I_{CS} - 210 \, \mu A) \) is injected into the negative input of the \( V_{TON} \) processing opamp.

- The on-time sharply reduces proportionally to the magnitude of the over-current event.

- No discontinuity in the operation, out-of-phase operation is maintained.

- No need for preventing OCP from tripping during a normal transient.

- The current can be accurately limited.

Images showing waveforms for \( I_{in}, I_{line}, V_{control} \) and \( V_{control}, I_{in}, I_{line} \).
NCP1631 In-rush Current Detection

In the circuit, when plugged into the mains, the bulk capacitor is abruptly charged to the line voltage and the charge current (in-rush current) is huge. Drive turn-on during this time can damage the MOSFETs.

When plugged into the mains, the bulk capacitor is abruptly charged to the line voltage and the charge current (in-rush current) is huge. Drive turn-on during this time can damage the MOSFETs.
NCP1631过压保护
NCP1631 Over Voltage Protection

- 反馈(FB)及过压保护(OVP)各有单独引脚(提供冗余) Separate pins for FB and OVP (redundancy)
- 这两种功能使用相同的2.5 V内部参考，用于简易、精确地设定OVP电平 The two functions share the same 2.5-V internal reference for an eased and accurate setting of the OVP level

方法1：OVP和FB共用一个反馈网络
Method 1: One feedback network for OVP and FB

\[
\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}}
\]

方法2：OVP和FB用两个独立的反馈网络
Method 2: Two separate feedback networks

\[
\frac{V_{out(ovp)}}{V_{out(nom)}} = \frac{R_{ovp1} + R_{ovp2}}{R_{out1} + R_{out2}} \cdot \frac{R_{out2}}{R_{ovp2}}
\]
50 ms消隐时间的输入欠压(BO)保护

Brown-out Protection with a 50-ms Blanking Time

- 忽略时间短于50 ms的主电源中断  Mains interruptions shorter than 50 ms are ignored
- 消隐时间帮助满足维持时间要求  The blanking time helps meet hold-up time requirements
- BO引脚电压用于前馈  The BO pin voltage serves for feedforward

对于消隐时间而言，BO引脚电压维持在BO阈值附近，当交流线路恢复时不延迟电路重启  For the blanking time, the BO pin voltage is maintained around the BO threshold not to delay the circuit restart when the line has recovered

20 ms时间的线路中断  20-ms line interruption
NCP1631 pfcOK/REF5V Signal

- The pfcOK signal can be used to enable/disable the downstream converter.

- It is high (5 V) when the PFC stage is in normal operation and low otherwise.

- The pfcOK signal is low:
  - Any time the PFC is off because a major fault is detected (UVLO condition, thermal shutdown, UVP, Brown-out, Latch-off / shutdown, $R_t$ pin open)
  - For the start-up phase of the PFC stage until the nominal bulk voltage is obtained

- The pfcOK pin can be used as a 5-V power source (5-mA capability)
使用简单易用的Excel电子表格来计算外部元件 (www.onsemi.cn) A (simple but easy to use) Excel Spreadsheet (www.onsemi.com) computes the external components.
议程 Agenda

- 简介 Introduction:
  - 交错式PFC基础知识 Basics of interleaving
  - 主要优势 Main benefits

- NCP1631：新颖的交错式PFC控制器 NCP1631: a novel controller for interleaved PFC
  - 异相管理 Out-of-phase management
  - NCP1631支持使用较小电感 The NCP1631 allows the use of smaller inductors
  - 主要功能 Main functions

- 实验结果及性能 Experimental results and performance
  - 一般波形 General waveforms
  - 能效 Efficiency

- 总结 Summary
NCP1631 Demoboard

Wide mains, 300 W, PFC pre-converter

NCP1631

MUR550
The circuit is latched off if $V_{cc}$ exceeds 17.5 V. Could be used for thermal protection.
正如预料，输入电流看上去象是CCM波形 As expected, the input current looks like a CCM one

高交流线路时，频率反走影响纹波 At high line, frequency foldback influences the ripple
这些图在正弦波形顶部获得 These plots were obtained at the sinusoid top

电流以每个相位频率的2倍摆动 The current swings at twice the frequency of each phase

低及高交流线路时相移充分达到180° At low and high line, the phase shift is substantially 180°
充电序列 Refueling Sequences

- CrM的低交流线路电压时谷底开关 CrM at low line with valley switching
- 高交流线路电压时固定频率工作(频率钳位) Fixed frequency operation at high line (frequency clamp)
- 两种情况下都异相工作 Out-of-phase operation in both cases
能效测量 Efficiency Measurements

- 输出电压通常为390 V The output voltage is generally 390 V

- 对于300 W应用而言, 输出电流是: For a 300-W application, the output current is:
  - 满载时770 mA 770 mA at full load
  - 20%负载时154 mA 154 mA at 20% of the load

- 两类电流一般以相同工具测量 Both currents are generally measured with the same tool

- 处于20%负载时，输入功率为63 W If @ 20% of the load, the input power is 63 W

- 输出电流1 mA误差会造成: 1-mA error in I\text{out} leads to
  - I\text{out} = 153 mA → 能效 Eff = 100 \times 390 \times 0.153 / 63 = 94.7 %
  - I\text{out} = 155 mA → 能效 Eff = 100 \times 390 \times 0.155 / 63 = 95.9 %

- 1 mA误差导通1.2%的能效差别! A 1-mA error causes a 1.2% difference in the efficiency!

- 在10%及20%负载条件下测量时需要细心! Measurements @ 10% and 20% of the load need care!!!
能效测量 Efficiency Measurements

- 能效并不只取决于控制模式 The efficiency does not only depend on the control mode
- 电感、MOSFET、二极管、EMI滤波器等都会影响能效 The inductor, the MOSFETs, diodes, EMI filter… play a role
- 例如，我们可以比较采用200 µH PQ2625电感与采用150 µH PQ2620电感时的能效差别 For instance, if we compare the efficiency with a 200-µH PQ2625 inductor to that with a 150-µH PQ2620 one:

<table>
<thead>
<tr>
<th>Load (%)</th>
<th>Efficiency @ 230 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 µH</td>
<td>97.0</td>
</tr>
<tr>
<td>150 µH</td>
<td>97.4</td>
</tr>
</tbody>
</table>

频率反走限制轻载时的能效差别 Frequency Foldback limits the difference at light load
在20%至100%负载范围，能效保持为：

- 低线路电压时高于95.8% (> 95.8% at low line)
- 高线路电压时高于97.0% (> 97.0 % at high line)

更多信息请访问 [www.onsemi.cn](http://www.onsemi.cn)，参见NCP1631EVB/D资料

Refer to NCP1631EVB/D at [www.onsemi.com](http://www.onsemi.com) for details
调节频率反走 Tweaking Frequency Foldback …

能在 pfcOK(5 V) 及频率反走引脚间增加电阻

A resistor can be added between the pfcOK (5 V) and frequency foldback pins

这样做，频率钳位会大幅减弱

Doing so, the frequency clamp decays more sharply:

\[ V_{\text{REGUL}} = \frac{R_2 \cdot 5V}{R_1 + R_2} \]

(\(V_{\text{REGUL}} \) is proportional to the PFC power)
能效提升 Efficiency Improvement

- 振荡器引脚上的电阻能设定最低频率 A resistor on the oscillator pin sets the minimum frequency
- 增加电阻$R_1$时，PFC段在10%和20%负载条件下工作在最低频率 (20 kHz) With $R_1$, the PFC stage operates at the minimum frequency (20 kHz) at 10% and 20% of the load
- 调节频率反走进一步提升轻载能效 The tweak further improves the light load efficiency
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总结 Summary

- 交错式PFC支持使用较小的元器件、改善热性能、增强CrM功率范围并减小电流纹波
  Interleaved PFC allows use of smaller components, improves thermal performance, increases the CrM power range and reduces current ripple.

- NCP1631以单颗IC方案集成构建强固及紧凑的2相交错式PFC段所需的全部特性，且外部元件极少
  The NCP1631 provides a single IC solution which incorporates all the features necessary for building a robust and compact 2-phase interleaved PFC stage with minimal external components.

- FCCrM及频率反走支持使用小电感在完整负载范围内的高能效工作
  Its FCCrM and frequency foldback allows an efficient operation over the load range with small inductors.
For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies