Simulate with Physical and Scalable Discrete Models... What could we get ? Heinrich Kamamen, Didier Balocco



## Content

- Simulate Devices to Extract Parameters
  - On-Region simulation
  - ► R<sub>DS(ON)</sub> simulation
  - Transfer characteristic
  - Output Capacitor

Small Signal, Effective, Energy related or Charge related

Breakdown Voltage (and Drain Leakage Current)

# Application Simulations

Evaluate Losses and Junction Temperature on a DC-DC Boost

### Simulate devices : Let us practice !

? Is it easy and useful ?
? What can kind of results could be obtained ?



### **On-Region simulation**

**Drain Current vs Drain-to-Source Voltage** 



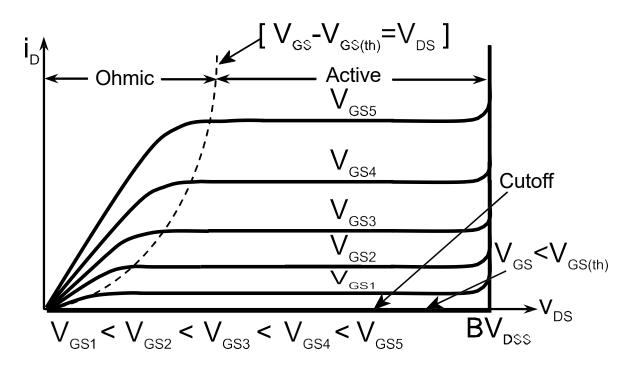
## **MOSFET On-Region – Books' Curve**

In books, we found the following onregion curves.

We have two regions:

Ohmic and Active

This is well known but in practice, this curve can be slightly different.



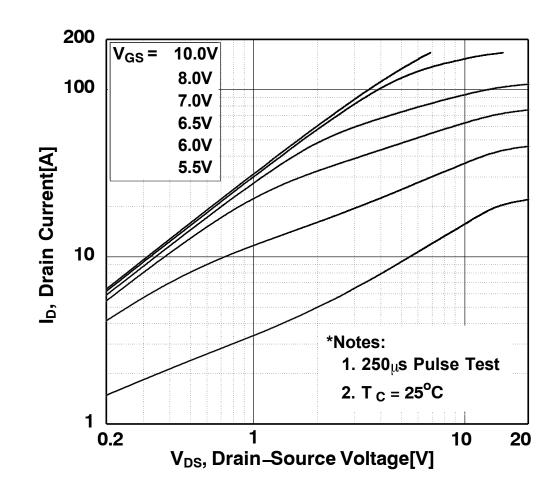


## **MOSFET On-Region – Data Sheet Curve**

For the NTHL040N65S3F, SuperFET3 Fast recovery 40 m  $\nu$ 

The data sheet give the following curve with Log-Log scales.

This curve is done with a 250-µs pulse test to avoid the MOSFET to heat...





## **MOSFET On-Region - Schematic**

The schematic is very simple :

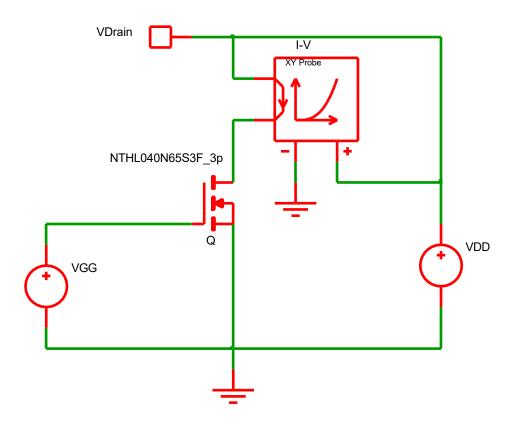
The MOSFET

A Drain-to-Source voltage source

A Gate-to-Source voltage source

That's all you need...

We add a "X-Y Probe" pseudocomponent to pre-set the output graph.



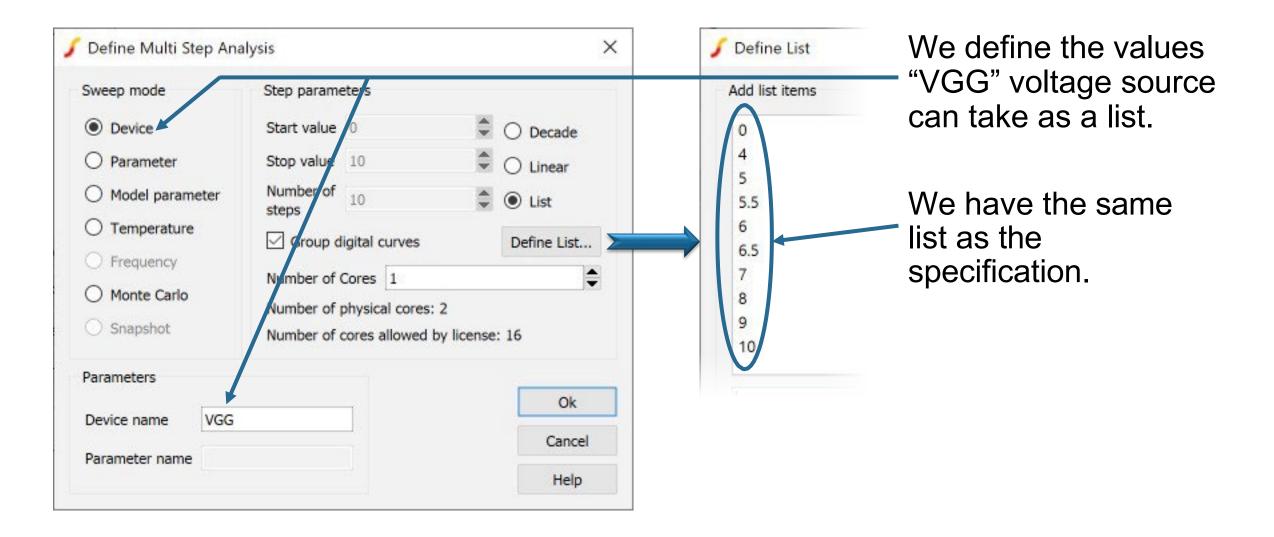


## **MOSFET On-Region – Setup 1**

🖌 Choose Analysis		×	
Transient AC	DC Noise TF SOA Data Options	Analysis Mode	We define the
Sweep parameters	5	Transient	simulation as
Start value	•	AC	"DC Sweep" on
Stop value	20 Deca	ade 🗹 DC Sweep	"VDD" source
Number of points		Noise	
Device name	VDD		
	Mode: Device VDD Define	DCOP	We define the
Monte Carlo and n	nulti-step analysis		variation amplitude.
Enable multi-s	tep  Define		
Selected mode: D	evice VGG		We enable the "Multi-Step"
		Ok	analysis to vary the
		Run	"VGG" source by
		Cancel	discrete steps
		Help	

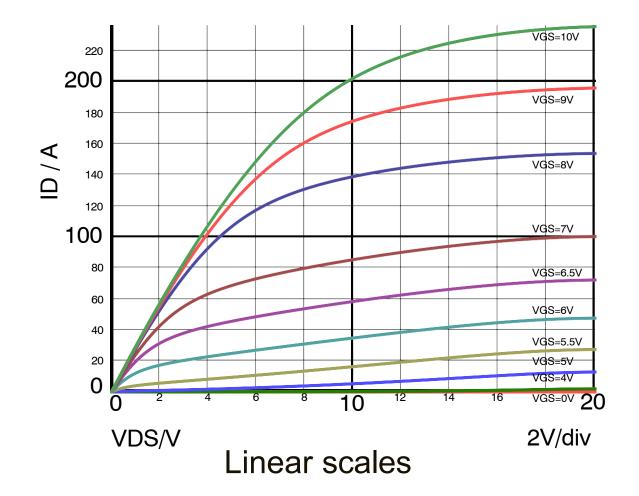
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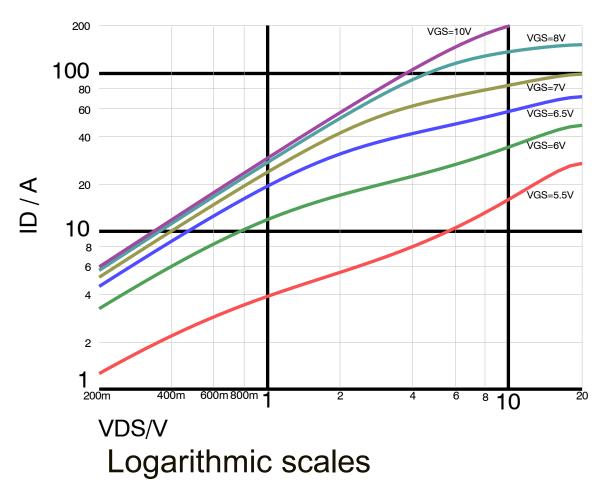
## **MOSFET On-Region – Setup 2**





## **MOSFET On-Region - Results**

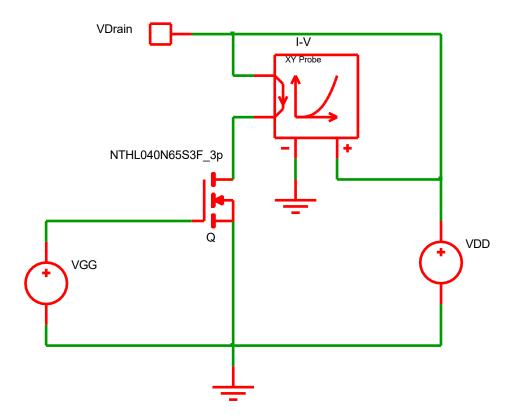






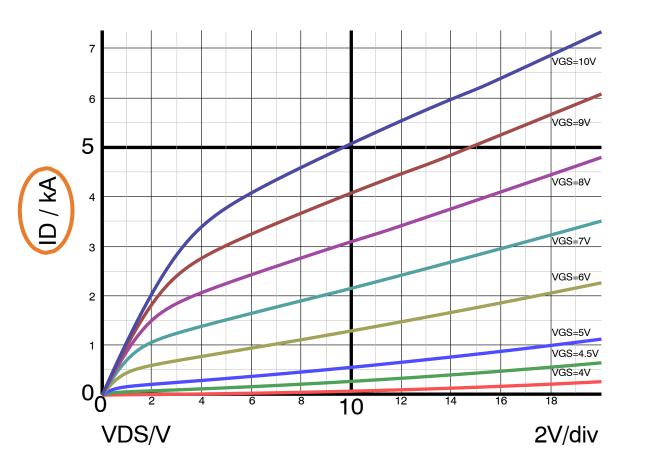
## **MOSFET On-Region - Schematic**

We re-use the same simulation schematic for a Medium Voltage MOSFET : NTMFS5C604N.





## **MOSFET On-Region - Results**



The results are far above maximum current capability given in the specification for the MOSFET

The active region is not really horizontal

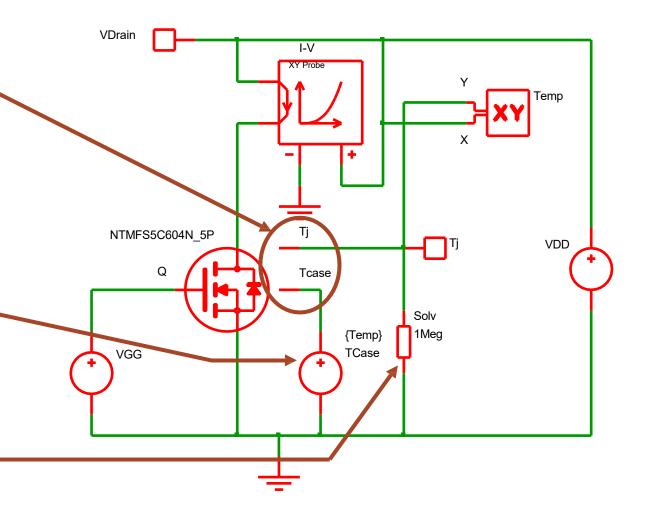


## **MOSFET On-Region with 5-pin model - Schematic**

We will use a 5-pin device to see the temperature behavior during this test.

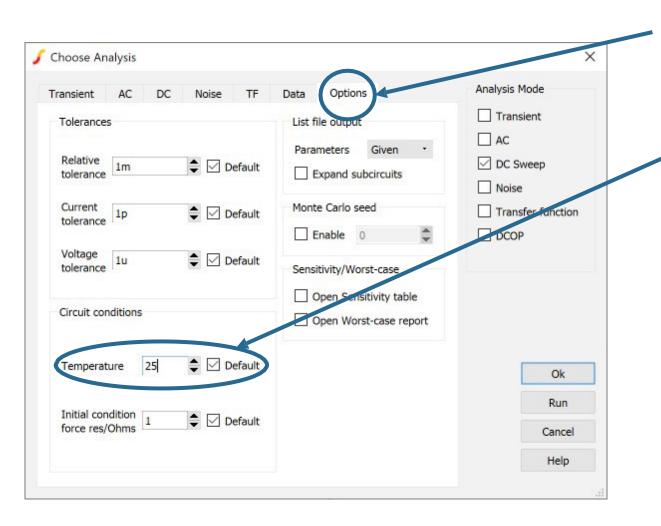
The model uses the electro-thermal equivalence where Voltage represents the Temperature and the Current represents the Power dissipated. The case temperature is set to the system temperature using a voltage source. The voltage-source value is set with the SIMetrix variable "Temp" storing the system temperature.

We need to add a  $1-M_{\nu}$  resistor on the "Junction Temperature" pin to help the solver to converge.





## **MOSFET On-Region with 5-pin model – Temperature Setup**

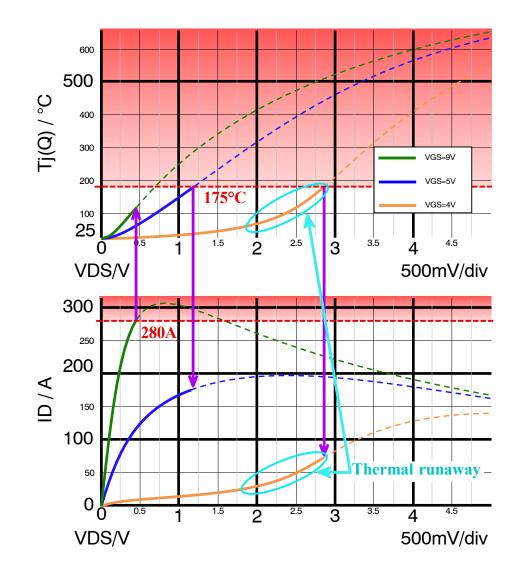


In the option tab inside simulation setup windows,

The system temperature can be set to 25 °C



### **MOSFET On-Region with 5-pin model - Results**



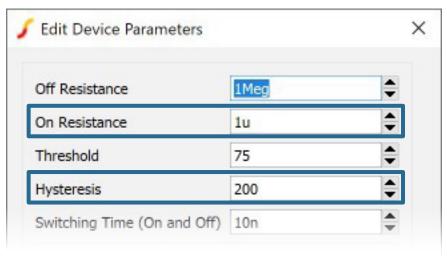
For  $V_{GS} = 4 V$ , we see a thermal runaway in the active region. The junction temperature rises above 175°C before the drain current reaches the 280 A specification limit.

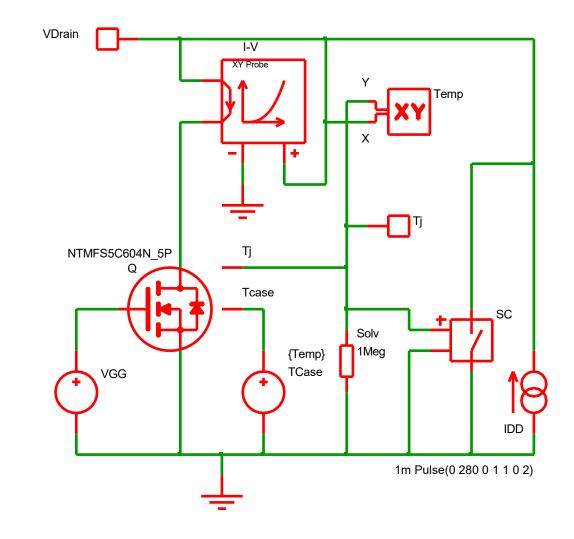
For  $V_{GS} = 5$  V, the device stays in the ohmic region, but the junction temperature rises to 175°C before it gets to 280-A drain current limit.

For  $V_{GS}$  = 9 V, the device stays in the ohmic region, but the drain current rises to 280 A limit before it gets to 175°C junction temperature.

## **MOSFET On-Region within the limits - Schematic**

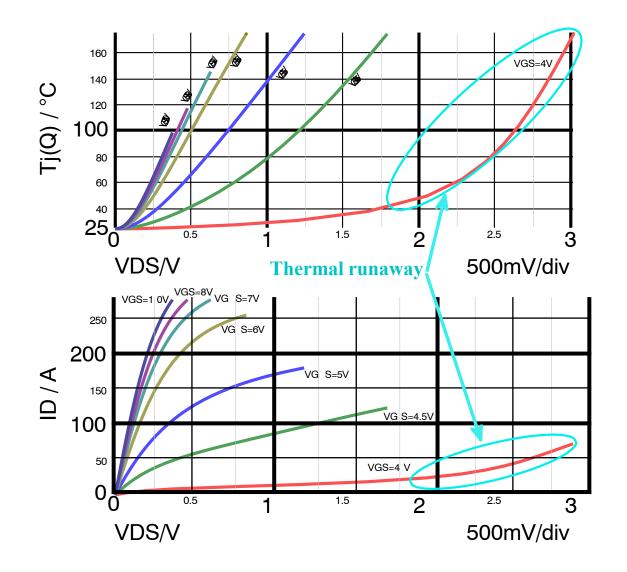
- We set IDD current source to 280 A.
- We use a switch with very low on-resistance driven by the junction temperature to short the current source when the temperature gets above 175°C.
- We implement a very large hysteresis to avoid a new turn on when the device cools down.







## **MOSFET On-Region within the limits - Results**



• This is the real useful curves for 25°C package temperature.

• Using simulation, we can have the real operating curves in real conditions.

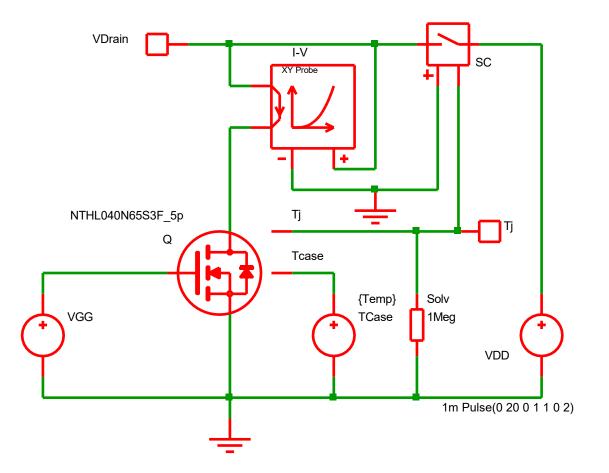


## **MOSFET On-Region within the limits - Schematic**

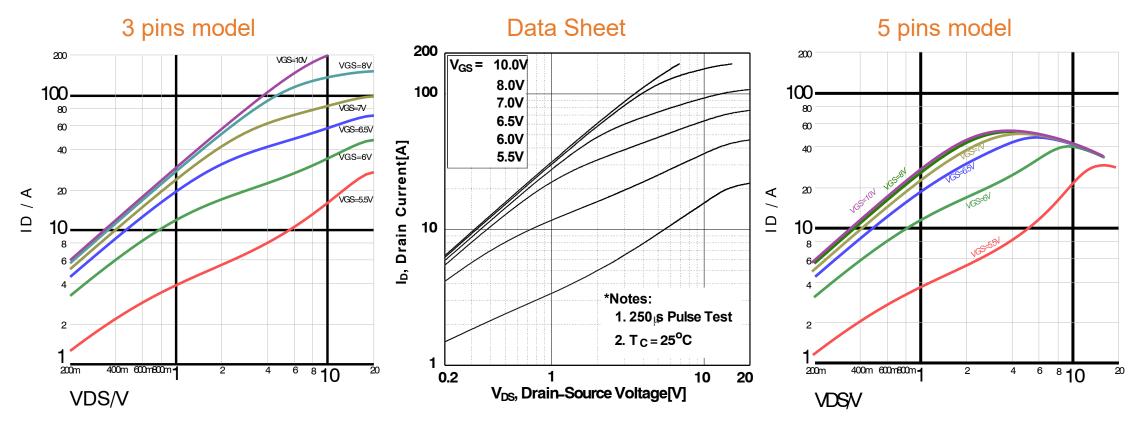
With the NTHL040N65S3F, we can applied the same setup.

We use a switch with very high offresistance driven by the junction temperature to open the voltage source when the temperature gets above 150°C.

We implement a very large hysteresis to avoid a new turn on when the device cools down.

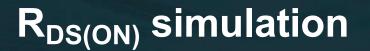


# Comparing $I_D$ - $V_{DS}$ graph for the NTHL040N65S3F



- 3 different results...
  - With 3 pins model, the die is "some how" maintained at constant temperature (or like if measurement was done with an infinite small pulse)
  - ► Data sheet use 250µs pulse for measurement.
  - ► With 5 pins model, measurement are done in DC (infinite long pulse)





#### vs Drain Current or Temperature or Time

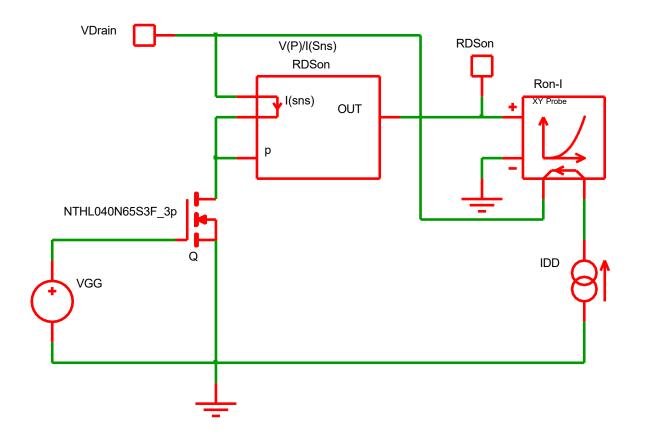


# **R**<sub>DS(ON)</sub> vs Drain Current - Schematic

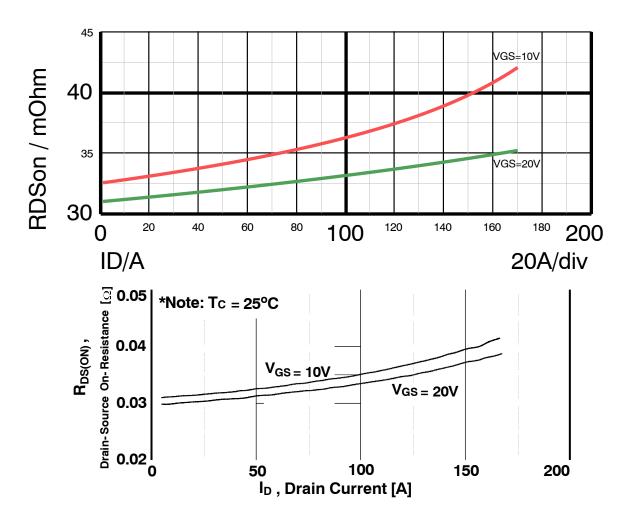
We connected a current source between the drain and source pin.

To calculate the  $R_{DS(on)}$ , we use an arbitrary source to make the division between drain-to-source voltage by the drain current. We obtain a voltage directly proportional to the "on" resistance.

We add a "X-Y Probe" pseudocomponent to pre-set the output graph.



# **R**<sub>DS(ON)</sub> vs Drain Current - Results



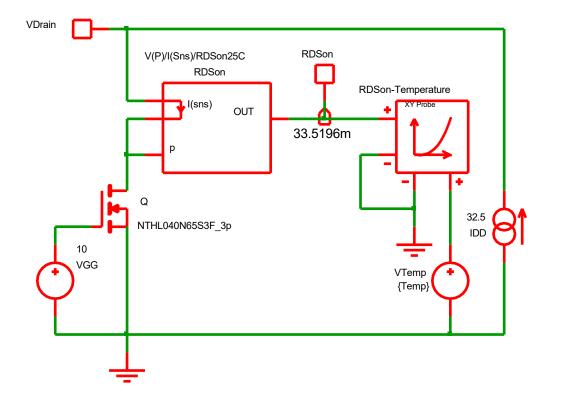
We can see a slight difference between simulation with the NTHL040N65S3F model and the data sheet curve.

In fact, for a 100-A  $I_D$  and a 10-V  $V_{GS}$ , the difference is almost 1.25 m $\Omega$ . This corresponds to a 3% relative difference.

This is acceptable.



## **R**<sub>DS(ON)</sub> vs Temperature - Schematic



We use almost the same schematic,

Except :

The current is fixed at 32.5 A,

A voltage source to represent the ambient temperature,

We add a "Bus annotation marker" to have the  $R_{DS(on)}$  at 25°C.

# R<sub>DS(ON)</sub> vs Temperature – Setup 1

Define Arbitrary Source Expression Enter an expression to define the output. Click ? button for more information V(P)/I(Sns)/RDSon25C	? × Local parameters Enter local parameters in form <b>name = expression</b> Click ? button for more information RDSon25C=1 4	Here is the arbitrary function definition with the parameter used to normalize the curve
Implementation      Arbitrary source      Compile to binary using Verilog-A.      Offers more functions and higher     performance for complex definitions.     (Requires Pro or Elite license)	Outputs  Outputs  Single ended voltage  Single ended current  Differential voltage  Differential current	
Ok Cancel Help		

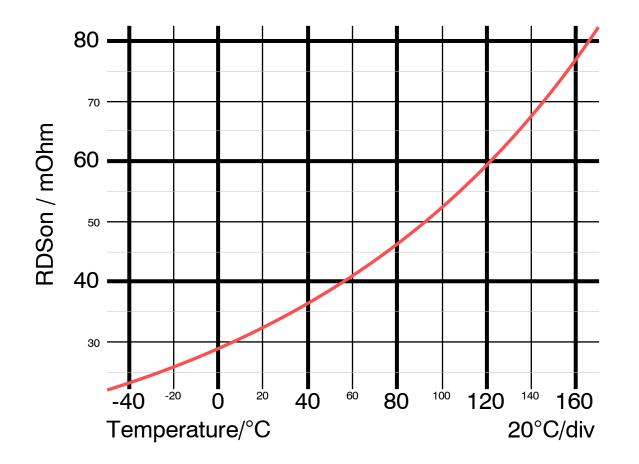


# **R**<sub>DS(ON)</sub> vs Temperature – Setup 2

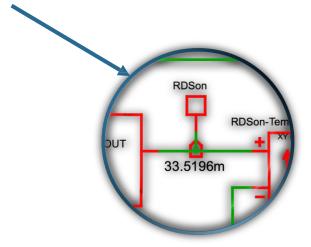
🕻 Choose Analysis			×
Transient AC DC Tolerances Relative 1m Current 1p Voltage 1u Voltage 1u Circuit conditions Temperature 25	Noise TF SOA	Data Options   List file output   Parameters   Given   Expand subcircuits     Monte Carlo seed   Enable   •	Analysis Mode Transient Ac DC Sweep Noise Transfer function Choose Analysis Transient AC DC DC Noise Transient AC DC Noise Transient AC DC Noise Transient AC DC Noise Transfer function Them, we define the analyze temperature range
Initial condition 1 force res/Ohms	🖨 🗹 Default		Sweep parameters Start temperature 50 O Deca
Verilog-HDL Options	Verilog simulator Icaru Timing resolution 1fs	s-10.1.1 •	Stop temperature 170

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## **R**<sub>DS(ON)</sub> vs Temperature – Results



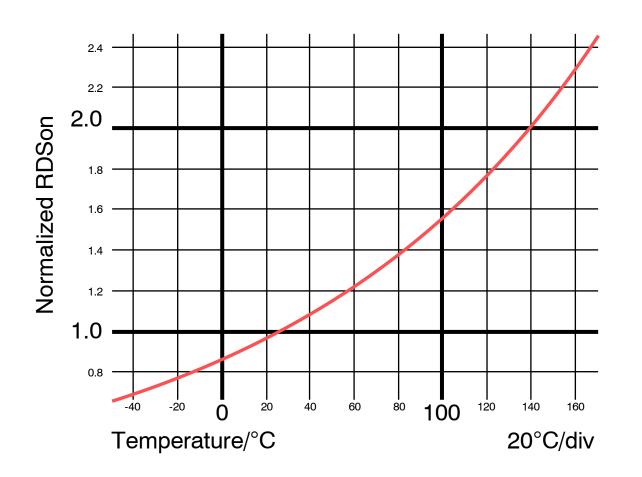
On the schematic, we can read the  $25-^{\circ}C$  value for the  $R_{DS(on)}$ .



This value will be used as parameter value for arbitrary function for the next simulation.



## **R**<sub>DS(ON)</sub> vs Temperature – Results Normalized



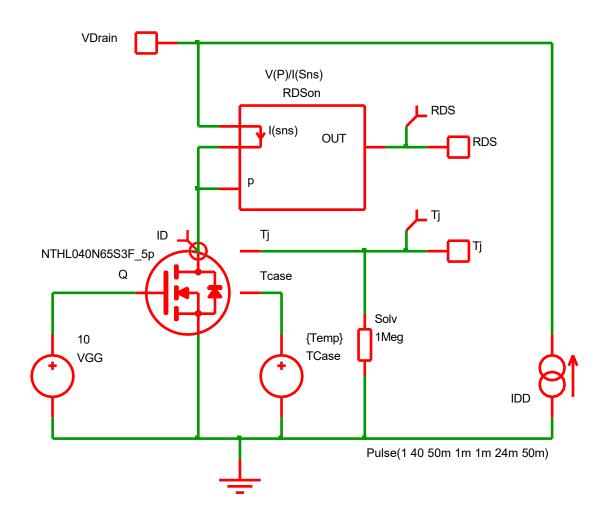
Around 140°C, the R<sub>DS(on)</sub> value is twice the 25-°C value.



# **R**<sub>DS(ON)</sub> vs Time - Schematic

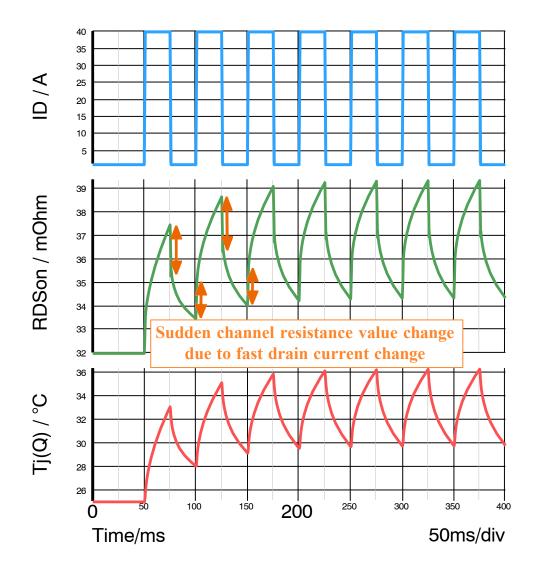
The 5-pin models are very useful when you want to know the junction temperature behavior depending on the mission profile.

Here, we analyze a low frequency switching schematic and the impact on junction temperature.





# **R**<sub>DS(ON)</sub> **vs Time - Results**



We can notice the sudden change in the channel resistance when the drain current changes rapidly from 1 A to 40 A and backward. This phenomenon was predicted by the curve Channel resistance vs Drain current.

We also see the effect of the self-heating or cooling of the device itself during the plateau phase of the current (1 A and/or 40 A).

The system is stable after a 200-ms transient. The maximum junction temperature is 36 °C and the minimum 30 °C. The junction temperature oscillates between those two values.



### **Transfer characteristic**

**Drain Current vs Gate-to-Source Voltage** 

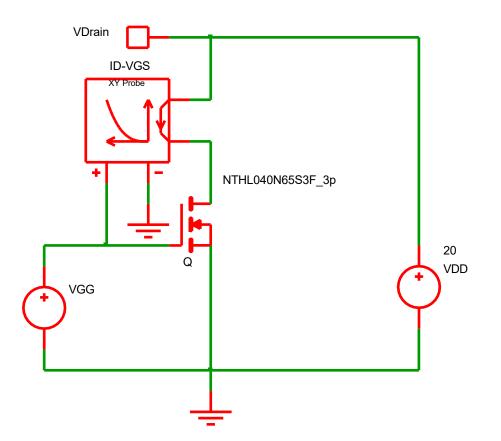


## **Transfer Characteristic - Schematic**

The transfer characteristic shows how the drain current changes with the gateto-source voltage.

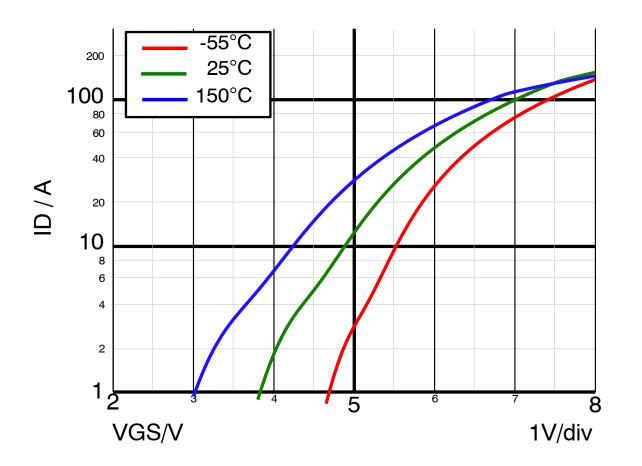
The simulation was done with a 20-V drain-to-source voltage and for various temperature values.

We will use a X-Y probe to plot the transfer characteristic and the temperature will be set via the "Multi-Step" simulation list.





## **Transfer Characteristic - Results**



We can see the difference for the gate threshold in function of temperature.



### **Output Capacitor**

Small Signal, Effective, Energy related or Charge related



## **Output Capacitor**

For switching application, the output capacitor called  $C_{oss}$  defined as

 $C_{!""} = (C_{\#\$} + C_{\%\#}) \quad @V_{\%\$} = 0 \text{ V}$ 

is an important parameter as it has an impact on the transistor switching losses. In fact, every time the MOSFET turn on, the energy stored in output capacitance is discharged and lost in the transistor. The lower  $C_{oss}$  is the better.  $C_{oss}$  is a non-linear capacitance and highly depends on the drain-to-source voltage.

There are 3 to 4 types of outputcapacitance values found in the specification.

The capacitance types are called:

Small-signal value,

Effective value,

Energy-related value,

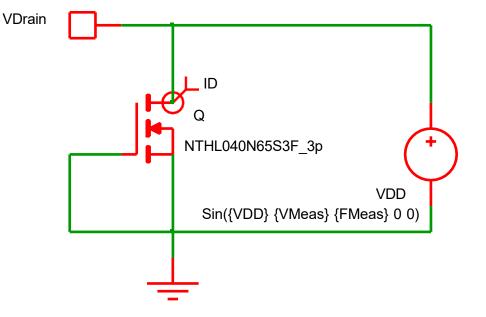
Charge-related value.



## **Output Capacitor Small-signal - Schematic**

For the signal signal value, we will use the following equation :

$$C_{!""} = \frac{\&}{(\times^{*})} \times \frac{(\#+,-.\ /0++1.2)_{!"\#\$-\&'-!"\#\$}}{(\#+,-.-2!-\$!0+41\ 5!62,71)_{!"\#\$-\&'-!"\#\$}}$$



We will use 20-mV peak-to-peak sinusoidal voltage source with frequency equal to 1 MHz in series with the drainto-source continuous voltage.

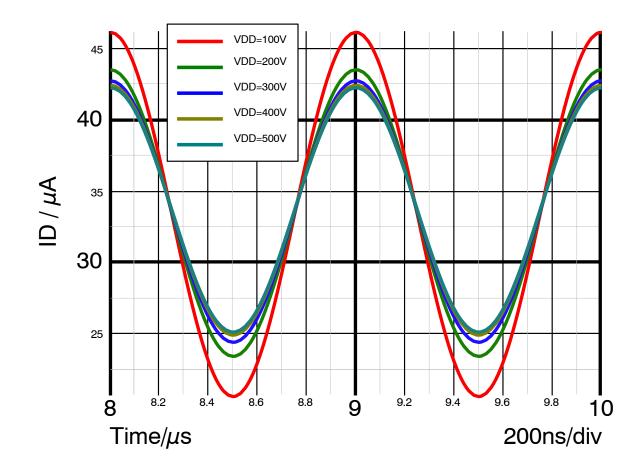


## **Output Capacitor Small-signal – Setup**

🥤 Define Multi Step An	alysis X	{VDD} is a parameter for the
Sweep mode Device Parameter Model parameter Temperature Frequency Monte Carlo Snapshot	Step parameters Start value 100	drain-to-source voltage continuous value. We will sweep this value
Parameters Device name Parameter name VDD	Ok Cancel Help	



#### **Output Capacitor Small-signal – First Results**



We show here only the two last milliseconds.

We can notice the continuous current offset (around  $32 \mu A$ ) corresponding to the Drain-to-Source leakage current.

The peak-to-peak value depends on the continuous Drain-to-Source voltage.

So, the output capacitor also...

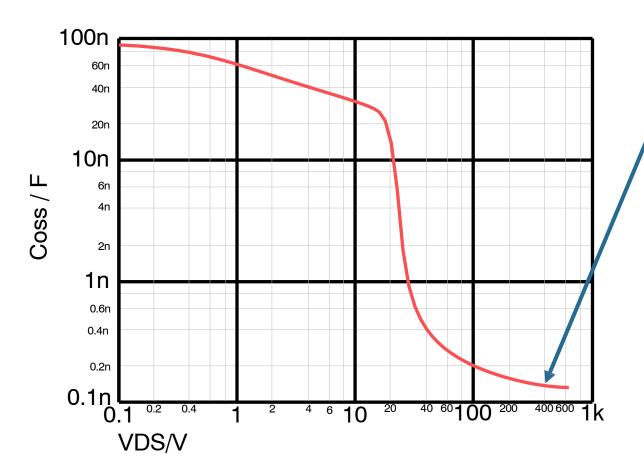


#### **Output Capacitor Small-signal – Setup 2**

To calculate the output capacitor, we use an arbitrary-function probe with the previous  $C_{OSS}$  equation.

🧲 Edit Probe				
Probe Options	Axis Scales	Axis Labels		PeakToPeak(I(sns))/PeakToPeak(V(p))/(2*GetDotParamValue('Pi')*GetDotPa
Probe expression Enter a goal function to define the probe. Use V( <i>nnn</i> ) for voltages and I( <i>sss</i> ) for currents. <i>nnn</i> and <i>sss</i> may be any string starting with a letter.		Multi-step mode Multiple curves Performance analysis	VDrain	
For example, the mean of a	For example, the following will plot the mean of a single input voltage vs the swept variable		<ul> <li>Histogram</li> <li>Histogram options</li> </ul>	Q NTHL040N65S3F_3p
Mean1(V(in))	Goal F	unctions	Number of 1 bins	Sin({VDD} {VMeas} {FMeas} 0 0)
amValue('Pi')*C	GetDotParamValu	ue('FMeas'))	Show advanced statistics	<u> </u>
Curve label			History	

#### **Output Capacitor Small-signal – Final Results**



These measurement are meet the datasheet results. As an example, for a drain-to-source equal to 400 V, we measured a  $C_{OSS}$  value of 142 pF in the figure.

This value matches with 140 pF given in the datasheet.

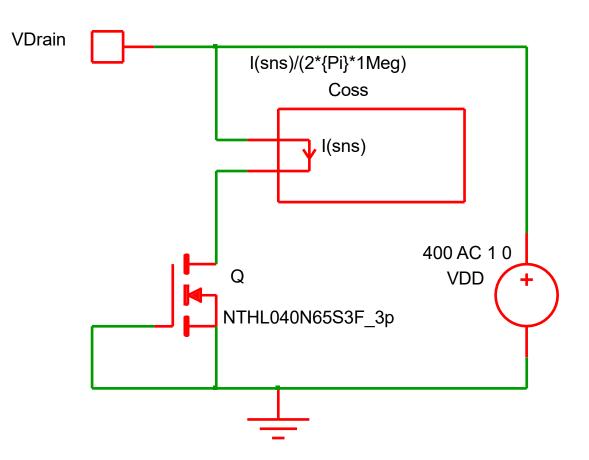
#### Output Capacitor Small-signal – Schematic / 2<sup>nd</sup> Method

In small-signal simulation, SIMetrix offers the possibility to sweep other parameters than frequency. Here, we will set the frequency to 1 MHz and sweep the drain-to-source dc voltage.

We will use the following equation to get  $C_{OSS}$  values :

$$C_{!""} = \frac{\#_{(\#)}}{\$\% \times ' \times ((^{*\#}))}$$

As the small signal is  $1 \vee (0 \text{ dBV})$ , it doesn't count in the equation.



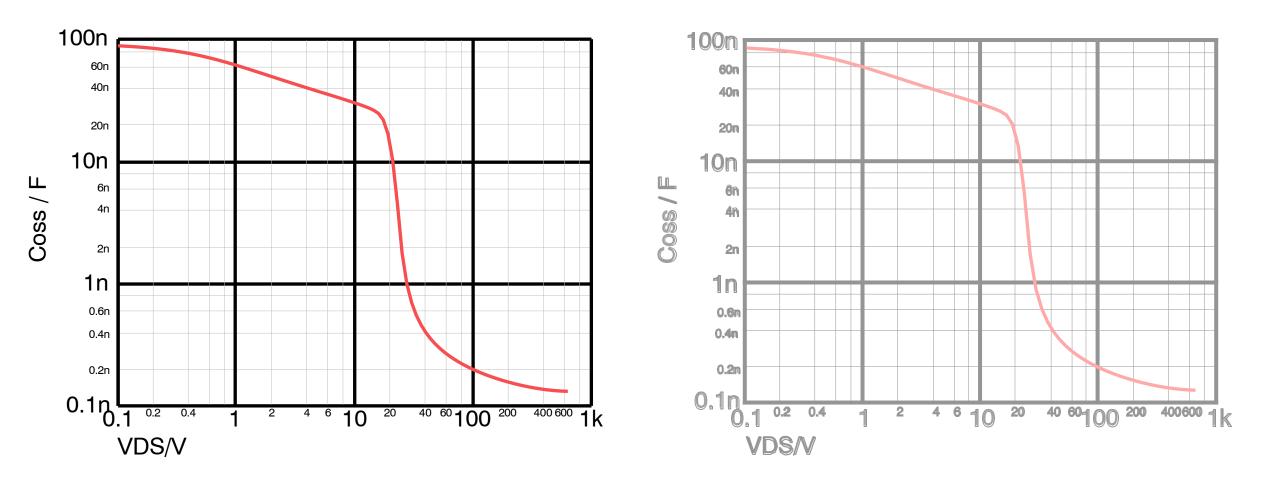
#### Output Capacitor Small-signal – Setup / 2<sup>nd</sup> Method

✓ Choose Analysis         Transient       AC       DC       Noise       TF       SOA       Data       Options         Sweep parameters       Start value       100m <ul> <li></li></ul>	×       The sweep values are for VDD (drain-to-Source) voltage and the frequency is fixed.         △ Ac       and the frequency is fixed.         □ Dc Sweep       Transfer function         □ DcoP       DcoP
Monte Carlo and multi-step analysis   Enable multi-step   Define     Selected mode: None     Data output   Save all currents   Check box to save currents in all devices including semiconductors. Note this may slow down simulation in some cases	<ul> <li>Define Sweep Mode</li> <li>Sweep mode</li> <li>Device</li> <li>Parameter</li> <li>Parameter</li> <li>Model parameter</li> <li>Temperature</li> <li>Frequency</li> <li>Mumber of points</li> </ul>
	O Monte Carlo Ok Cancel Help



#### Output Capacitor Small-signal – Results / 2<sup>nd</sup> Method

• 2<sup>nd</sup> Method



#### • 1<sup>st</sup> Method

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#### **Output Effective Capacitor - Definition**

The effective-capacitor value is defined as the equivalent linear capacitor storing the same amount of charge/energy with a voltage source equal to breakdown voltage value and a 100-k O series resistor to charge the output capacitor.

This value can be used to calculate the switching time in resonant topologies.

The charging equation for the linear capacitor in this configuration is given by:

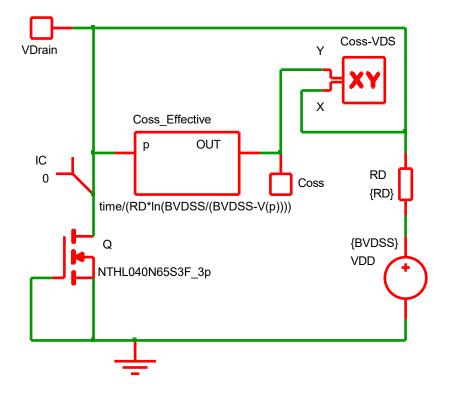
$$V_{j*}(Time) = V_{j} \left( 1 - e^{+, - . "} + /(\times 1_{2^{**}}) \right)$$

Solving this equation to get  $C_{OSS}$  gives:

$$C_{,**} = \frac{-./0}{1) \times 23 \left( \frac{3((-3))}{3((+3))} \right)}$$



#### **Output Effective Capacitor - Schematic**



We use an arbitrary function to get the  $C_{OSS}$  values and X-Y probe.

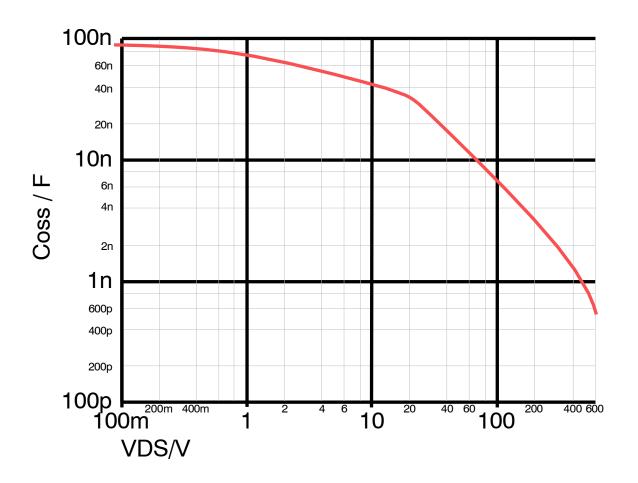
The values for the resistor (RD) and the voltage source (VDD) are set with parameters in the "Command Windows" (F11). The values are  $100 \text{ k}_{v}$  and 650 V respectively.

.Param RD=100k

.Param BVDSS=650

We set an initial condition for the drainto-source voltage using the "IC" pseudo-component.

#### **Output Effective Capacitor - Results**



In the "Dynamic Characteristics" table, the effective output capacitor is given for a drain-to-source voltage equal to 400 V.

On the side figure, we measure a  $C_{OSS}$  value equal to 1305 pF on the simulated curve.

This matches with 1366 pF given in the specification.



#### **Energy-related Output Capacitor - Definition**

The energy store in a capacitor is expressed by the following equation:

 $\mathsf{d}W = v(t) \times i(t) \times dt$ 

And the final energy for a constant capacitor can be express by the following equation:

$$W = \frac{1}{2}CV'$$

We can extract the capacitor value:

 $C_{8\$\$} = \frac{2\int_{9}^{:-;1} V_{\#\$}(t) \times I_{\#}(t) \times dt}{V_{\#\$}'(Time)}$ 

We use a current source to charge the output.

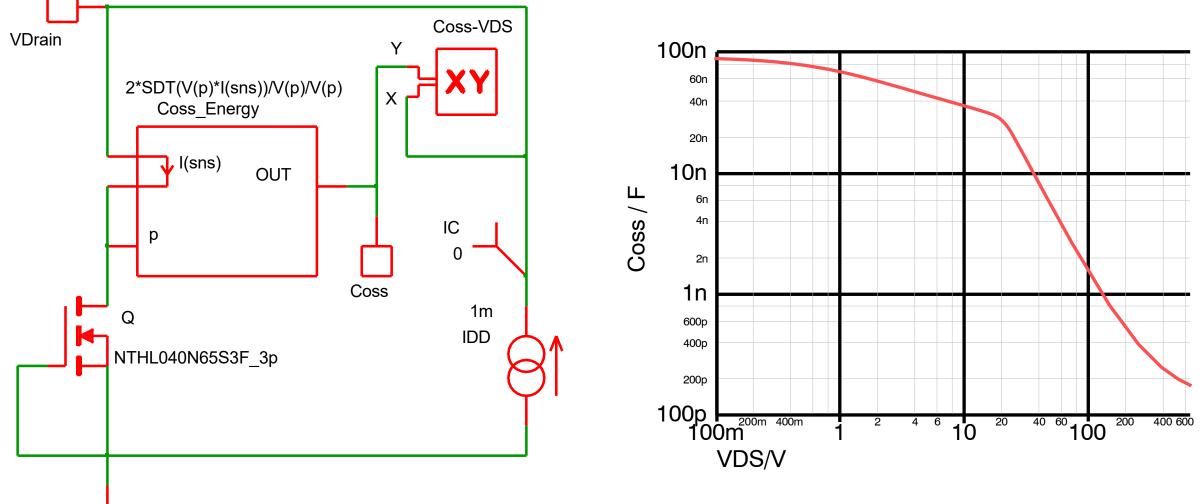
Here also, we use this formula in an arbitrary function to get the  $C_{OSS}$  value directly.

We use the integral function "SDT()" to calculate the numerator.

We set an initial condition for the drainto-source voltage using the "IC" pseudocomponent.



#### **Energy-related Output Capacitor – Schematic and Results**



In the "Dynamic Characteristics" table, the effective output capacitor is given for a drainto-source voltage equal to 400 V. We measured a  $C_{OSS}$  value equal to 245 pF on the simulated curve above and this matches with 247 pF given in the specification.

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#### **Charge-related Output Capacitor - Definition**

The charge store in a capacitor is expressed by the following equation:

 $dQ = i(t) \times dt$ 

And, the final charge for a constant capacitor can be express by the following equation:

Q = CV

We can extract the capacitor value:

$$C_{8\$\$} = \frac{\int_{4}^{, -. "} =_{(2) \times >2}}{5_{(*(:-; 1))}}$$

We use almost the same schematic.

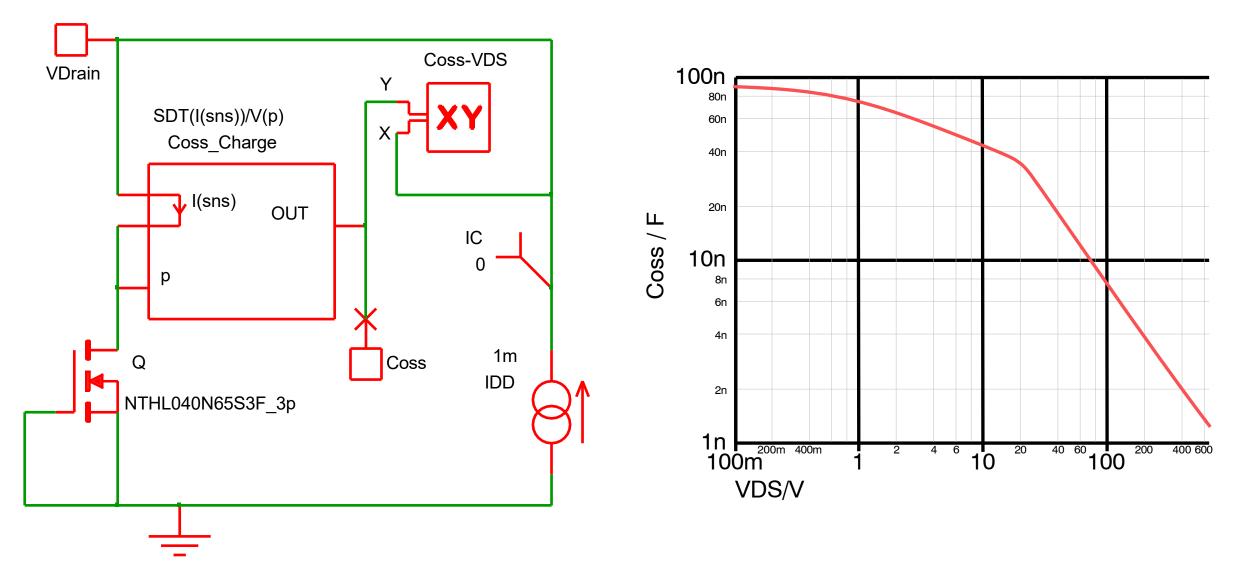
Here also, we use this formula in an arbitrary function to get the  $C_{OSS}$  value directly.

We use the integral function "SDT()" to calculate the numerator.

We set an initial condition for the drainto-source voltage using the "IC" pseudocomponent.



## **Charge-related Output Capacitor – Schematic and Results**



#### **Breakdown Voltage (and Drain Leakage Current)**

Simulation beyond the limits

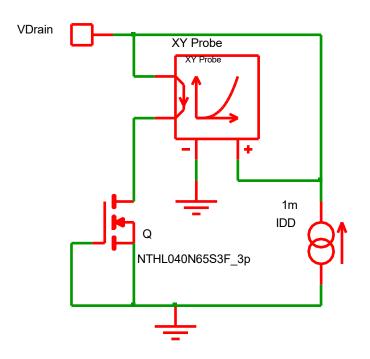


#### **Breakdown Voltage - Schematic**

The model gives the average values. The model is accurate inside the specification limits. Results outside specification limits are not warranted.

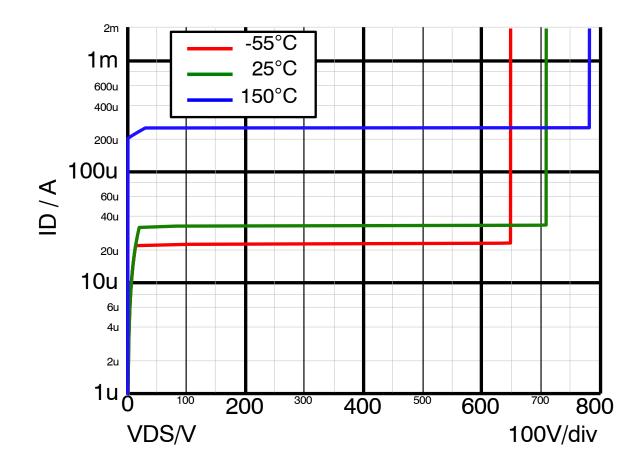
But, the model can operate above the limits with relatively good accuracy and can predict values like the average breakdown drain to source voltage (BV<sub>DSS</sub>).

To simulate the breakdown voltage depending on the temperature, we will use a ramp current source up to 2 mA and plot the "off" characteristic





#### **Breakdown Voltage - Results**



We can note the leakage current varies with temperature. We can measure  $23 \mu A$ ,  $33 \mu A$  and  $254 \mu A$  for respectively -55°C,  $25^{\circ}$ C and  $150^{\circ}$ C die temperature at a drain to source voltage equal to 400 V. We see a big leakage current increase between  $25^{\circ}$ C and  $150^{\circ}$ C.

The drain to source breakdown voltage is equal to 648 V, 708 V and 781 V for respectively -55°C, 25°C and 150°C die temperature.



#### **Device Simulation Conclusion**



Simulation is a much safer environment for testing the limits and above... All results in the data sheet can be obtained with those models.

As testing conditions in the data sheet are ideal (or not realistic),

- Simulation can provide more realistic characteristics,
- Parameters or Values in real conditions can be obtained.
- Parameters not in the data sheet can also be obtained.

Simulation models contain much more information than the data sheet.



#### **DC-DC Boost Example**

**Evaluate losses and junction temperature** 



#### **Application - Description**

We will simulate a boost stage (for a solar inverter).

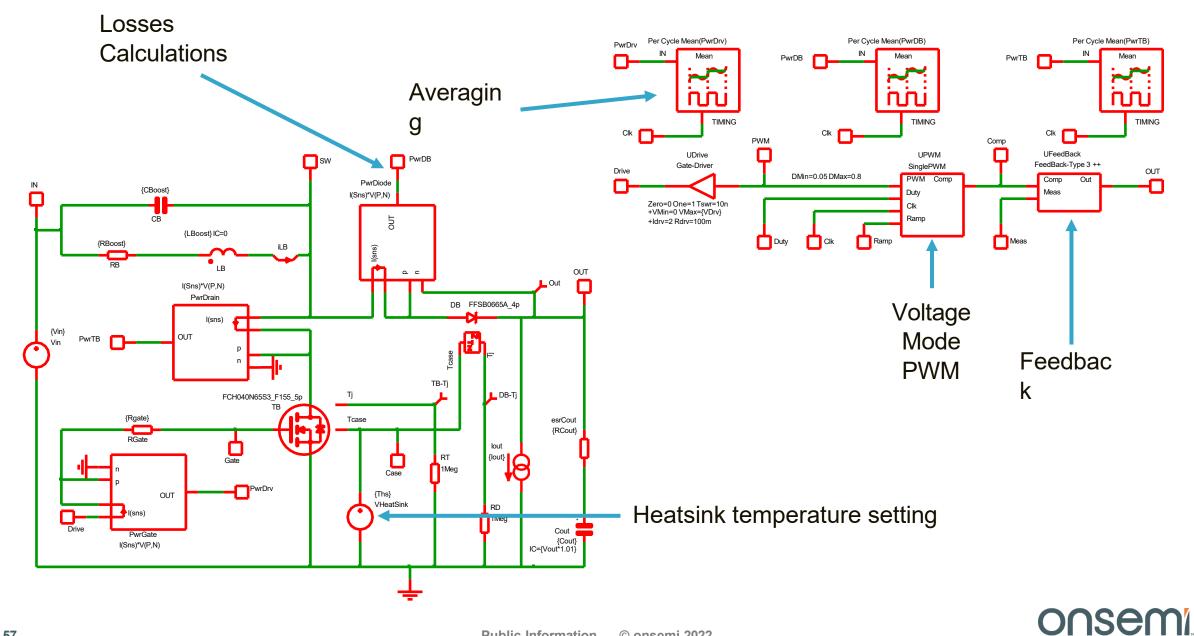
To avoid long stabilization time, we will close the loop. We will use a type 3 compensator with a voltage-mode pulse width modulator.

We will use arbitrary functions to calculate losses in the diode, in the MOSFET and the power to drive the MOSFET.

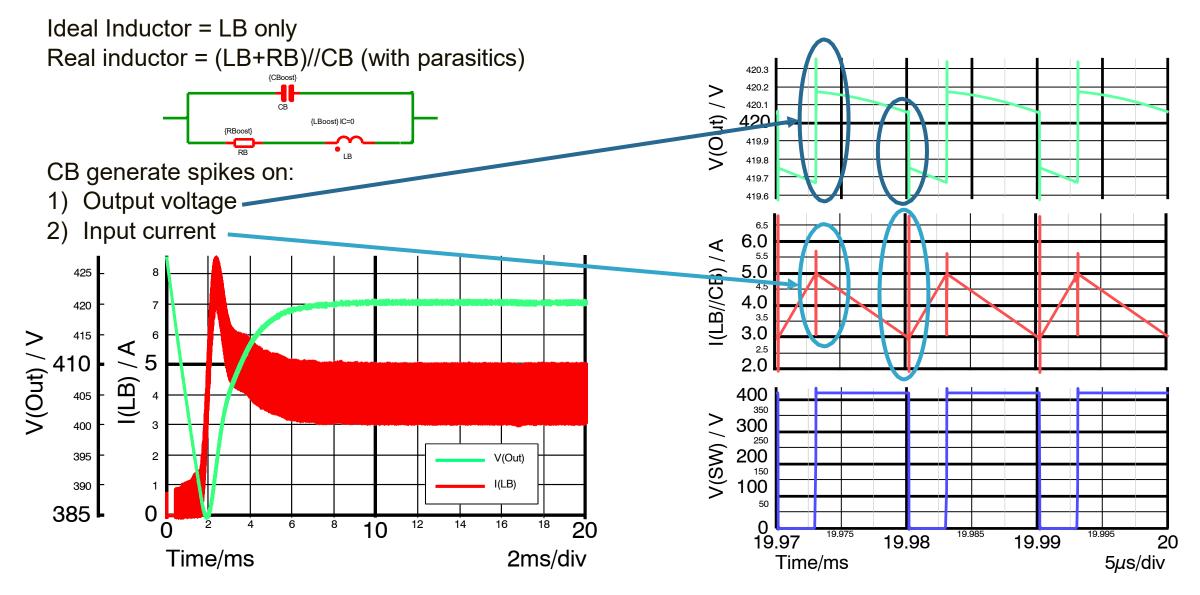
The "Per Cycle" measurement will be used to get the average losses for each cycle.

The specification for the power stage is the following: Input voltage: 300 V, Output voltage: 420 V, Inductor current: 4 A. Inductor current ripple: 2 A, Switching frequency: 100 kHz, Case temperature: 90 °C, Gate drive voltage: 10 V, Gate series resistor: 8 v.

#### **Application - Schematic**

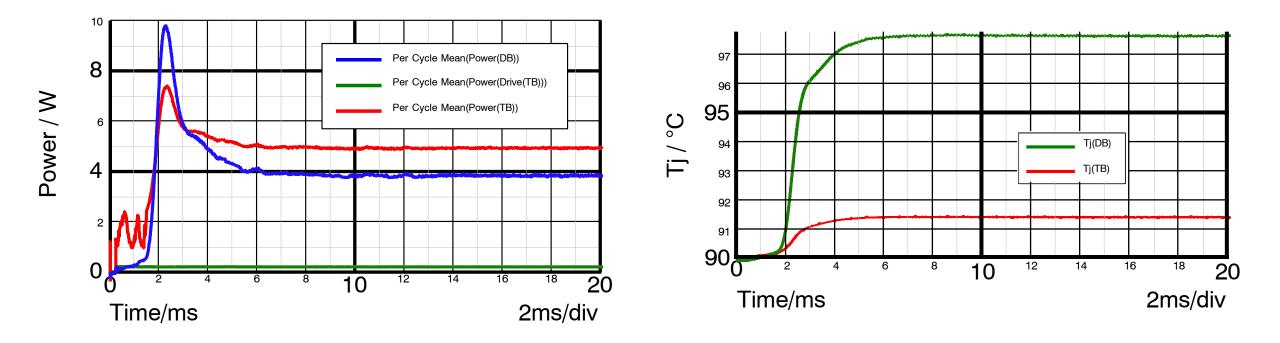


#### **Application - Waveforms**





#### **Application – Losses & Junction Temperature** For CB = 100 pF

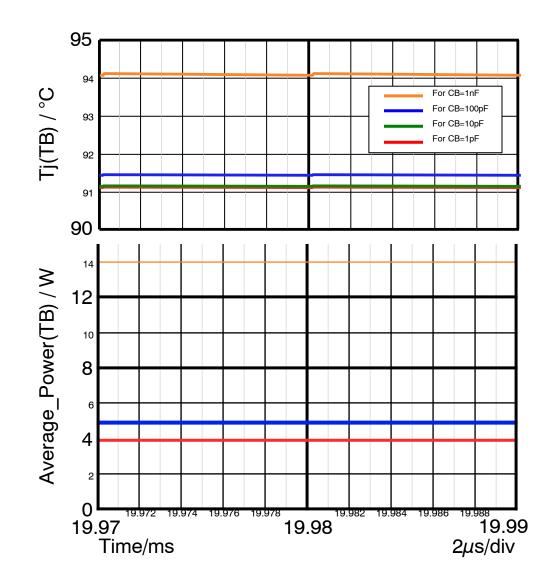




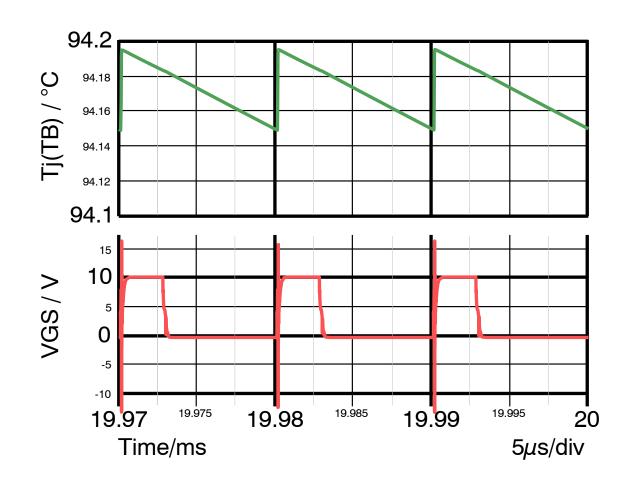
#### Application – Losses & Junction Temperature vs CB

The diode losses and the driving losses are not affected by CB values.

We can measure the following values for the transistor as a function of the parasitic capacitor: CB=1 pF => 3.9 W losses &  $\phi\lambda(T_J)=1.1^{\circ}C$ CB=10 pF => 4.0 W losses &  $\phi\lambda(T_J)=1.2^{\circ}C$  $\Rightarrow$  4.9 W losses CB=100 pF &  $\phi\lambda(T_J) = 1.4^{\circ}C$ CB=1 nF => 14.0 W losses &  $\phi\lambda(T_J)=4.1^{\circ}C$ 3.5 **3** Power / W Per Cycle Mean(Power(Drive(TB))) 2 Per Cycle Mean(Power(DB)) 1.5 0.5 <sup>19.988</sup> 19.99 **19.98**<sup>19.982</sup> 19.972 19.974 19.976 19.978 19.984 19.986 19.97 2µs/div Time/ms



#### **Application – Junction Temperature analysis**



There is a step in junction temperature waveform.

This step is synchronous with turn on.

So, there is a peak of power losses during turn on link to CB!

Performance can be jeopardized by your inductor (*parasitic capacitor*)!



### **Application – Optimization**

We keep the 100-pF inductor parasitic capacitor because this is a realistic value. The output power is equal to 1.2 kW. We obtain the following table after several trials using TO220 package for the diode and TO247 for the MOSFET.

MOSFET (TB)	Diode (DB)	τι <b>Τ</b> j	π <b>TJ</b>	Drive	MOSFET	Diode	Total
		MOSFET	Diode	Losses	Losses	Losses	Losses
FCH040N65S3	FFSP0465A	1,4 °C	7,3 °C	0,26 W	4,75 W	4,44 W	9,45 W
FCH040N65S3	FFSP0665A	1,5 °C	10,0 °C	0,26 W	4,98 W	3,88 W	9,12 W
FCH040N65S3	FFSP0865A	1,5 °C	4,1 °C	0,26 W	5,26 W	3,63 W	9,15 W
FCH040N65S3	FFSP1065A	1,6 °C	3,9 °C	0,26 W	5,46 W	3,41 W	9,13 W
FCH040N65S3	FFSP1265A	1,7 °C	3,7 °C	0,26 W	5,67 W	3,28 W	9,21 W
FCH040N65S3	FFSP0665B	1,4 °C	13,5 °C	0,26 W	4,80 W	3,80 W	8,86 W
FCH040N65S3	FFSP1065B	1,5 °C	6,6 °C	0,26 W	5,09 W	3,30 W	8,65 W
FCH067N65S3	FFSP0665B	1,6 °C	13,6 °C	0,15 W	3,90 W	3,80 W	7,85 W
FCH099N65S3	FFSP0665B	1,3 °C	13,6 °C	0,11 W	3,79 W	3,78 W	7,68 W
FCH125N65S3R0	FFSP0665B	1,7 °C	13,6 °C	0,09 W	3,85 W	3,79 W	7,73 W
FCH099N65S3	FFSP1065B	1,5 °C	6,6 °C	0,11 W	4,16 W	3,30 W	7,57 W

The last configuration with 10 A SiC new generation diode (FFSP1065B) and 99 mo EasyDrive SuperFET 3 (FCH099N65S3) gives less losses...

But a 10 A SiC diode for an average output current equal to 2.8 A could be consider oversized and, so, expensive.

#### **Application Simulation Conclusion**



- Simulation gives a more realistic losses values than an estimated analytic function.
- Simulation can help to understand parasitic influences on an application schematic
- Running several configurations can help to find a better compromise between performances and cost.







# Physical and scalable models can really help designers to analyze components characteristics and applications performances.



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