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TND6298/D

20 W T-lamp Direct AC LED Driver with Analog Dimming

This reference design covers specification, theory of operation and testing. This reference design can be applied to 20 W analog dimming using the NCL30170 driver, and accurate current calibration and low−THD performance can be implemented.

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REFERENCE DESIGN

Table 1. SPECIFICATIONS TABLE

Input Voltage	108–132 Vac	Low line
	198–264 Vac	High line
Line Frequency	50 Hz/60 Hz	
Input Power	20 W	
Power Factor	0.973	Min
THD	18.5%	Typ
Line Current Regulation	±0.1%	
Analog Dimming Range	< 5%	
Start Up Time	< 150 ms	Typ.
Lighting Surge	±2.0 kV (Line to Neutral)	ANSI/IEEE C62.41−1991 Class A
EMI	Conducted	150 kHz–30 MHz

Key Features

- Accurate Constant LED Current across Input Voltage Range
- Selectable LED Channel Counts using Advanced Topology
- Excellent Power Factor and THD with Sinusoidal Current Shape
- Wide Analog Dimming Range < 5%
- Excellent Phase−cut Dimmer Compatibility
- Protections
- Input Over Voltage Protection
- Thermal Shut Down
- Sensing Resistor Short Protection

April, 2020 − Rev. 2

Publication Order Number:
TND6298/D

SCHEMATIC

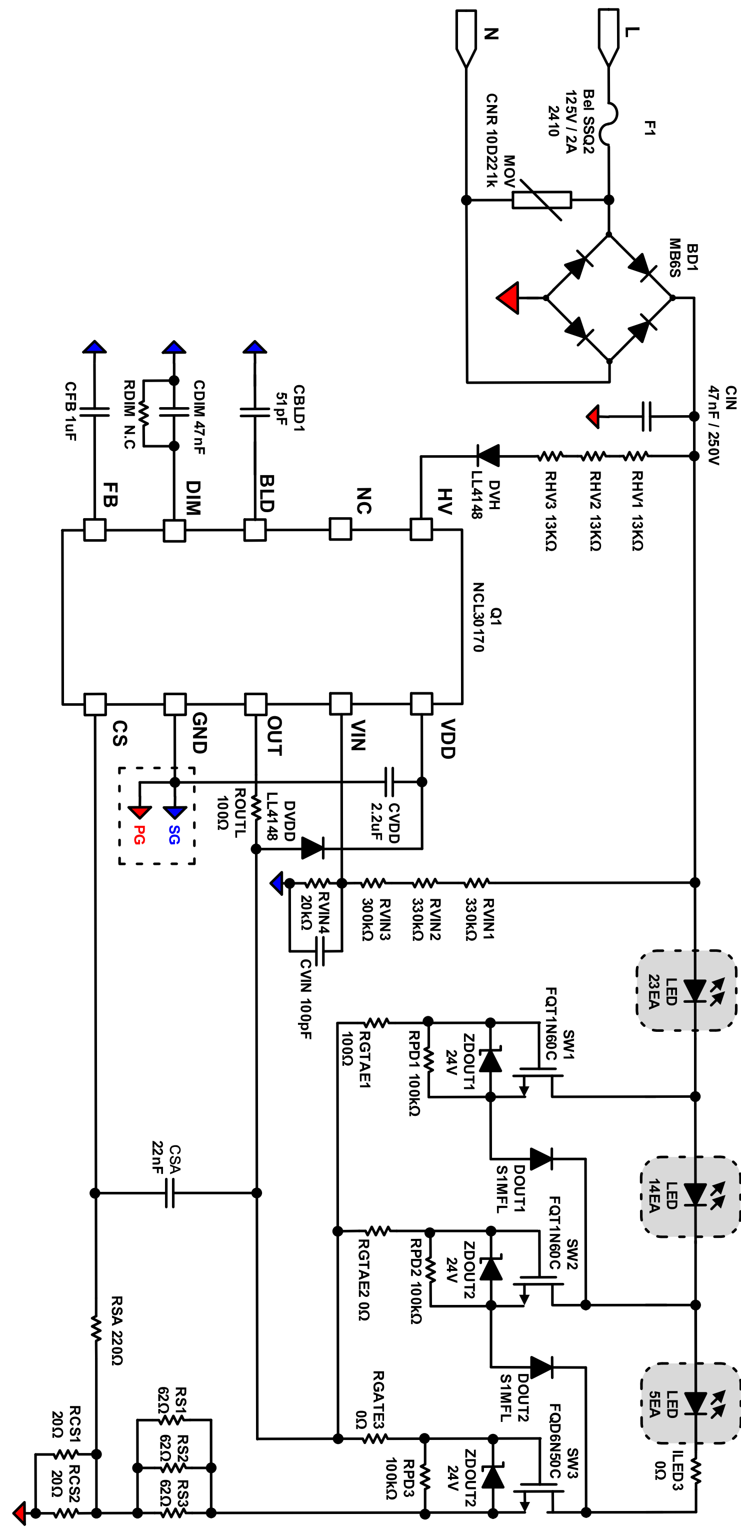


Figure 1. Schematic for Low Line 20 W ADIM

Table 2. BILL OF MATERIALS FOR LOW LINE (BOM)

Part Reference	Part Description	Qty	Vendor	Value
PCB	NCL30170 20 W ADIM EVB	1	ANY	
NCL30170	IC SOIC10	1	ON Semiconductor	Controller
F1	fast Acting 125 V 2 A SSQ2 2410	1	Bel fuse	
MOV	CNR10D221K	1	ANY	
BD1	Bridge diode 600 V 0.5 A, MB6S SOIC−4	1	ON Semiconductor	
ZOUT1−3	SMD 24 V Zener Diode, SOD−523	2	ON Semiconductor	
DHV, DVDD	SMD Diode LL4148 (LL−34)	3	ON Semiconductor	
SW1, SW2	MOSFET FQT1N60C SOT−223	2	ON Semiconductor	
SW3	MOSFET FQD6N50C D−PAK	1	ON Semiconductor	
DOUT1, DOUT2	SMD Diode, 1000 V, 1 A, Fast recovery, RS1M	2	ON Semiconductor	
RHV1, RHV2, RHV3	3216 Resistor, 13 kΩ	3	ANY	
ILED3	3216 Resistor, 0 Ω	4	ANY	
RVIN1, RVIN2	3216 Resistor, 330 kΩ	2	ANY	
RVIN3	3216 Resistor, 300 kΩ	1	ANY	
RVIN4	3216 Resistor, 20 kΩ	1	ANY	
RPD1−3	1608 Resistor, 100 kΩ	3	ANY	
RCS1, RCS2	3216 Resistor, 20 Ω	2	ANY	
RSA	2012 Resistor, 220 Ω	1	ANY	
RS1, RS2, RS3	3216 Resistor, 62 Ω	3	ANY	
ROUTL	2012 Resistor, 100 Ω	1	ANY	
RGATE1	1608 Resistor, 100 Ω	1	ANY	
RGATE2,3	1608 Resistor, 0 Ω	2	ANY	
CIN1	Axial Flim Capacitor, 47 nF/250 V	1	ANY	
CVDD	3216 Capacitor, 50 V 2.2 μF	1	ANY	
CBLD1	3216 Capacitor, 51 pF	1	ANY	
CVIN	3216 Capacitor, 100 pF	1	ANY	
CDIM	1608 Capacitor 47 nF	1	ANY	
CSA	2012 Capacitor 22 nF	1	ANY	
CFB	2012 Capacitor 1 μF	1	ANY	
LED Configuration	JK3030AWT−00−0000−000A0HL250E (3.2 V 400 mA 5000K)	42	Cree	

SCHEMATIC

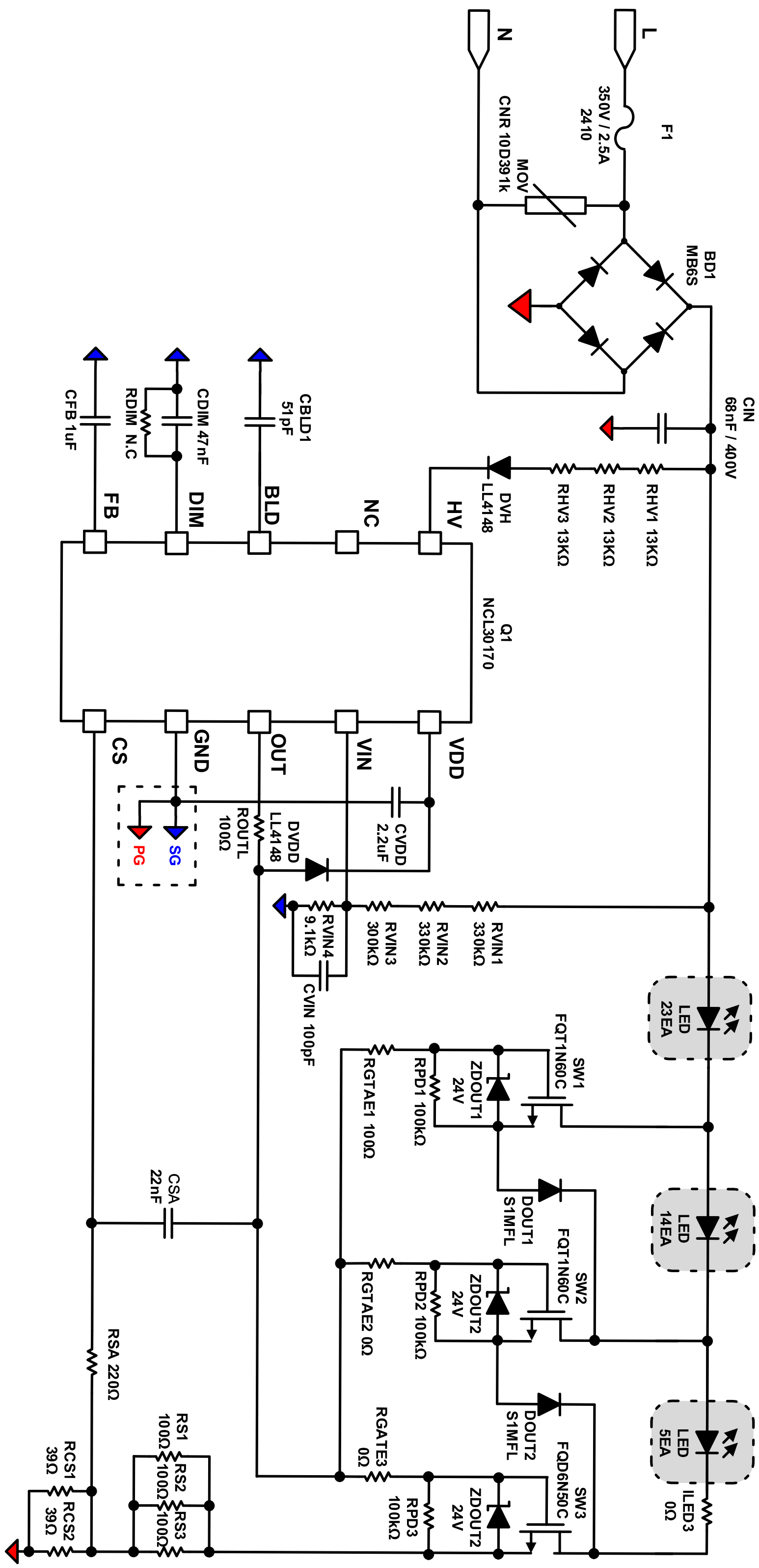


Figure 2. Schematic for High Line 20 W ADIM

Table 3. BILL OF MATERIALS FOR HIGH LINE (BOM)

Part Reference	Part Description	Qty	Vendor	Value
PCB	NCL30170 20 W ADIM EVB	1	ANY	
NCL30170	IC SOIC10	1	ON Semiconductor	Controller
F1	fast Acting 350 V 2.5 A SSQ2 2410	1	Bel fuse	
MOV	CNR10D391K	1	ANY	
BD1	Bridge diode 600 V 0.5 A, MB6S SOIC−4	1	ON Semiconductor	
ZOUT1−3	SMD 24 V Zener Diode, SOD−523	2	ON Semiconductor	
DHV, DVDD	SMD Diode LL4148 (LL−34)	3	ON Semiconductor	
SW1, SW2	MOSFET FQT1N60C SOT−223	2	ON Semiconductor	
SW3	MOSFET FQD6N50C D−PAK	1	ON Semiconductor	
DOUT1, DOUT2	SMD Diode, 1000 V, 1 A, Fast recovery, RS1M	2	ON Semiconductor	
RHV1, RHV2, RHV3	3216 Resistor, 13 kΩ	3	ANY	
ILED3	3216 Resistor, 0 Ω	4	ANY	
RVIN1, RVIN2	3216 Resistor, 330 kΩ	2	ANY	
RVIN3	3216 Resistor, 300 kΩ	1	ANY	
RVIN4	3216 Resistor, 9.1 kΩ	1	ANY	
RPD1−3	1608 Resistor, 100 kΩ	3	ANY	
RCS1, RCS2	3216 Resistor, 36 Ω	2	ANY	
RSA	2012 Resistor, 220 Ω	1	ANY	
RS1, RS2, RS3	3216 Resistor, 100 Ω	3	ANY	
ROUTL	2012 Resistor, 100 Ω	1	ANY	
RGATE1	1608 Resistor, 100 Ω	1	ANY	
RGATE2,3	1608 Resistor, 0 Ω	2	ANY	
CIN1	Axial Flim Capacitor, 68 nF/400 V	1	ANY	
CVDD	3216 Capacitor, 50 V 2.2 μF	1	ANY	
CBLD1	3216 Capacitor, 51 pF	1	ANY	
CVIN	3216 Capacitor, 100 pF	1	ANY	
CDIM	1608 Capacitor 47 nF	1	ANY	
CSA	2012 Capacitor 22 nF	1	ANY	
CFB	2012 Capacitor 1 μF	1	ANY	
LED Configuration	LED Luxeon 3030 2D 6 V 240 mA	42	Luxeon	

PERFORMANCE

Test Data – Analog Dimming Mode

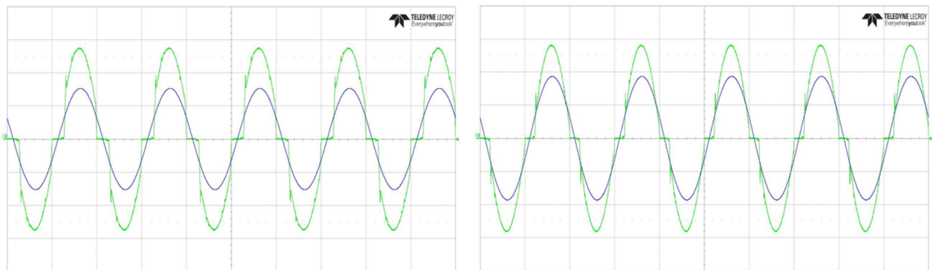


Figure 3. Normal Operation for Low Line ADIM

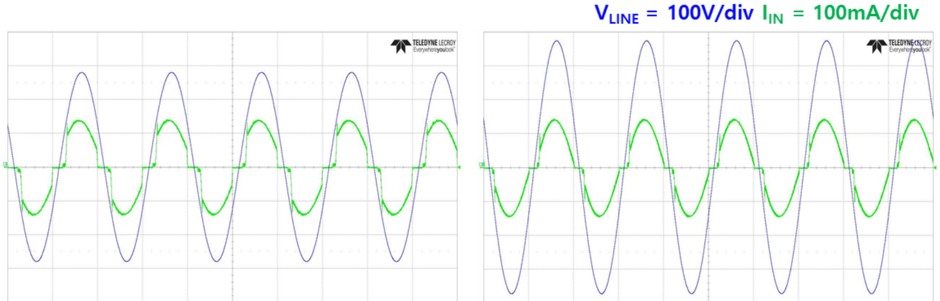


Figure 4. Normal Operation for High Line ADIM

Table 4. POWER FACTOR AND THD OVER INPUT VOLTAGE

20 W Low Line EVB				20 W High Line EVB			
Input Voltage [Vac]	Input Power [W]	PF	THD [%]	Input Voltage [Vac]	Input Power [W]	PF	THD [%]
108	19.6	0.977	21.5	198	18.4	0.973	21.4
120	21.7	0.982	18.5	220	20.4	0.979	18.0
132	23.9	0.984	17.5	264	24.4	0.982	15.6

NOTE: See LED configuration design guidance in the section 5.4 if PF and THD need to be further improved.

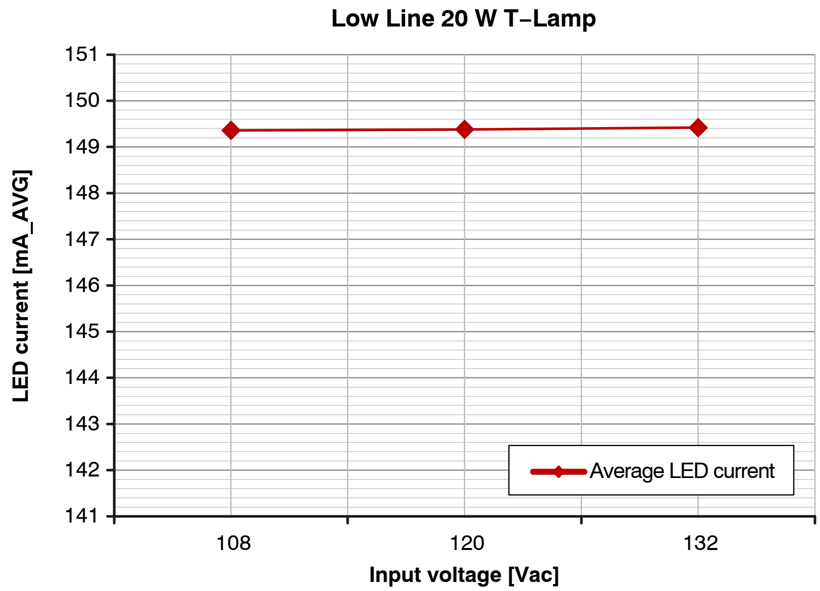


Figure 5. Line Regulation Performance for Low Line

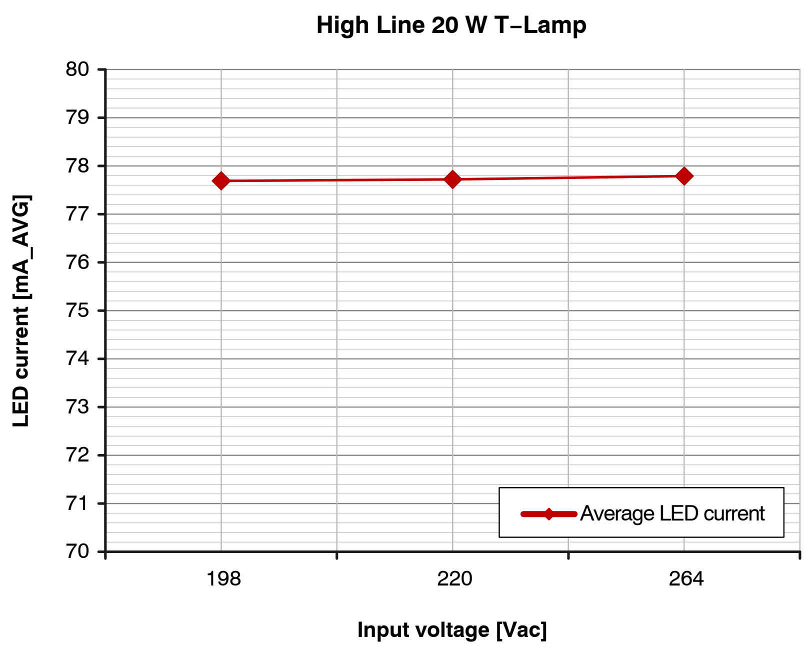


Figure 6. Line Regulation Performance for High Line

Start Up Performance

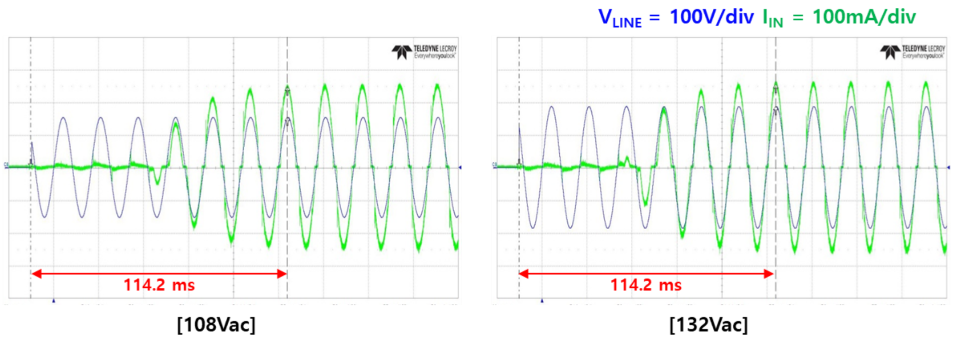


Figure 7. Start Up for Low Line ADIM

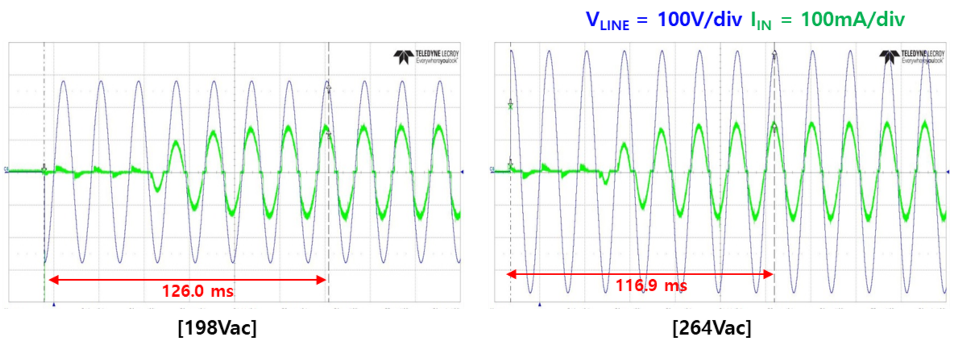
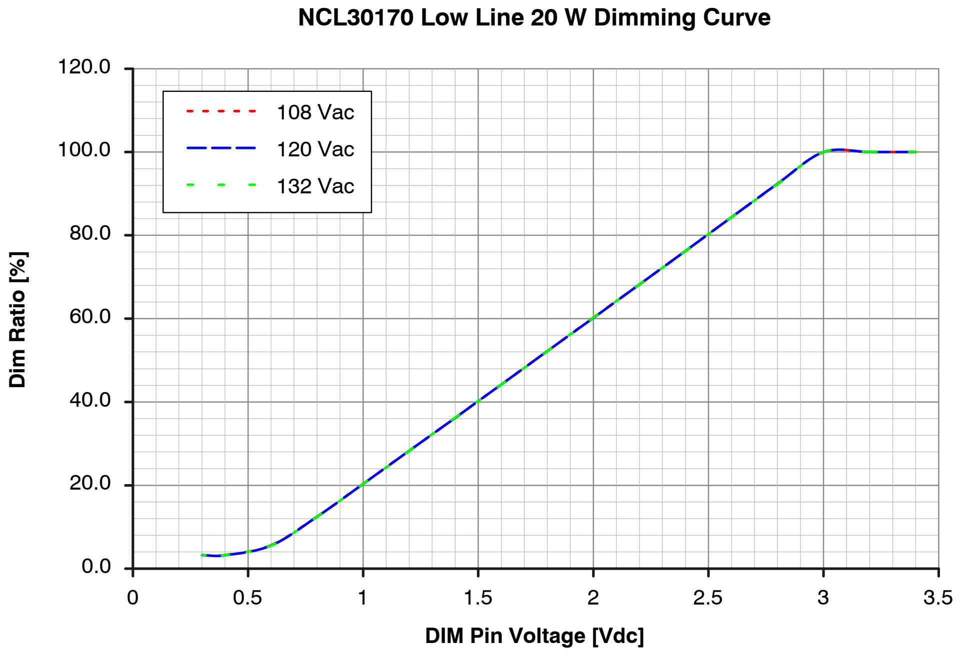


Figure 8. Start Up for High Line ADIM

Table 5. START UP TIME

20 W Low Line EVB		20 W High Line EVB	
Input Voltage [Vac]	**Start Up Time [ms]**	**Input Voltage [Vac]**	**Start Up Time [ms]**
108	114.2	198	126.0
132	114.2	264	116.9

Dimming Performance



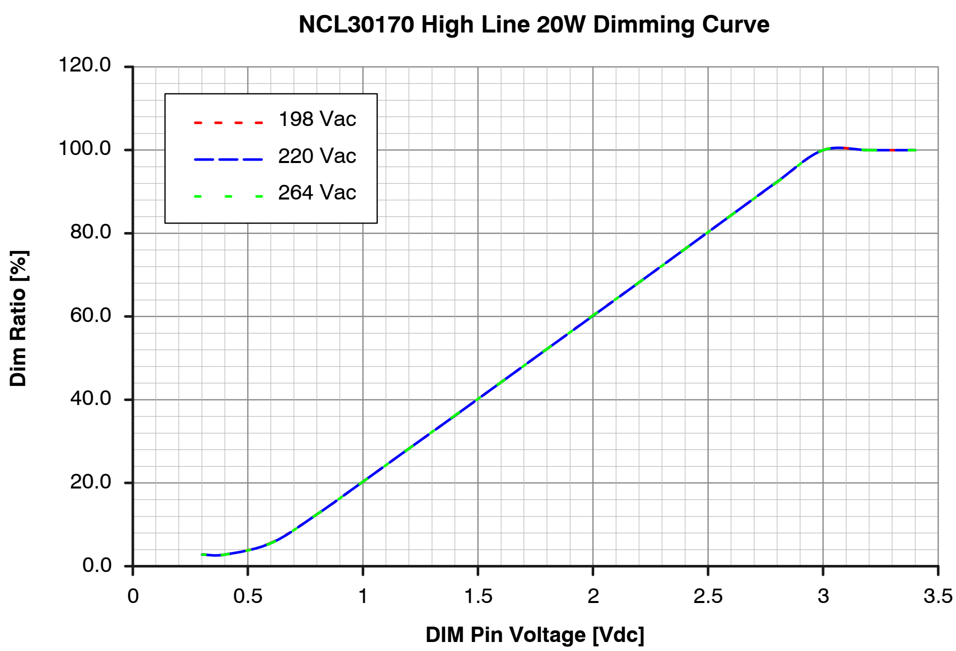


Figure 9. Dimming Curve for Analog Dimming

Current Balancing at Analog Dimming

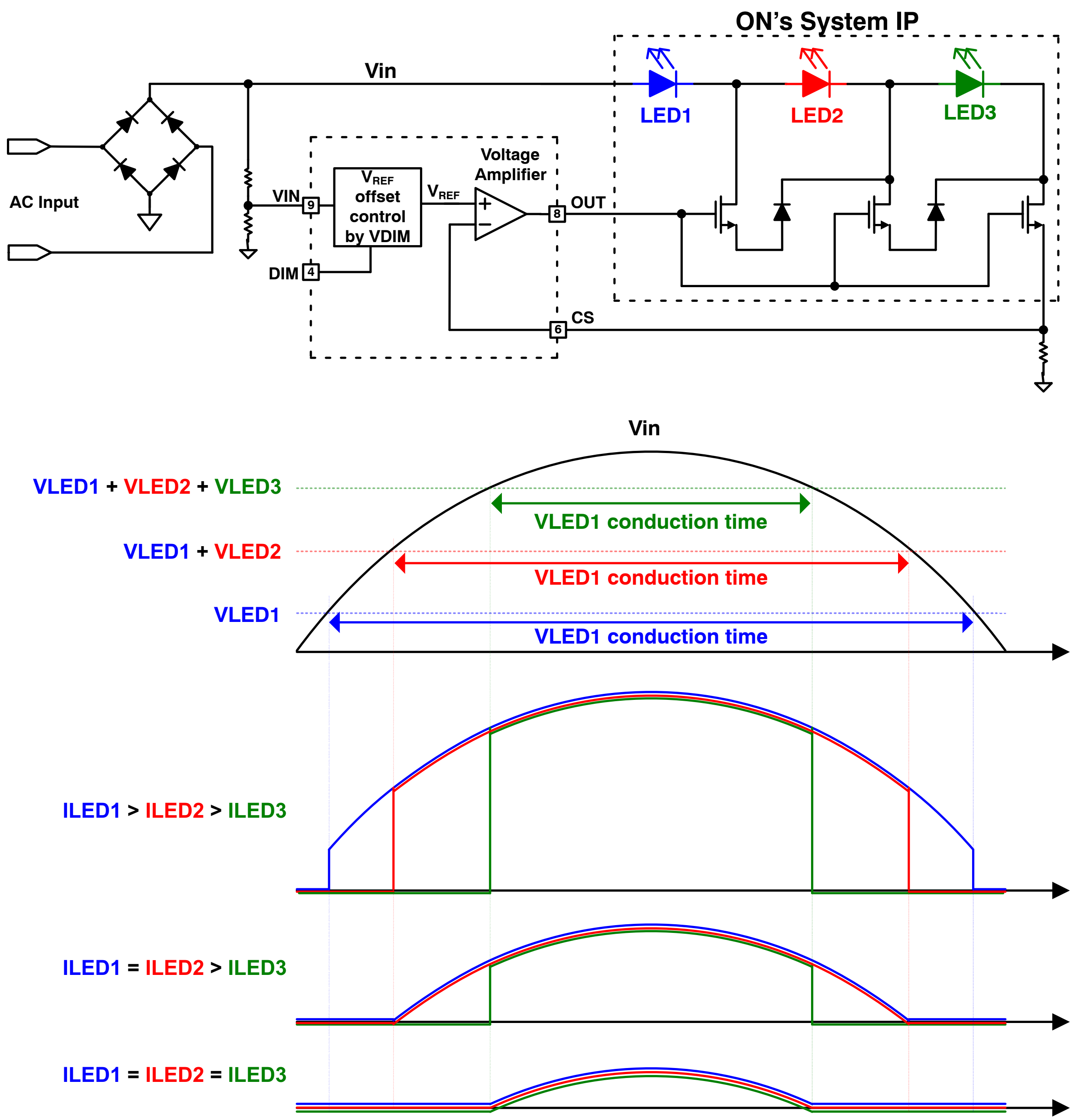


Figure 10. Uniform LED Channel Current Driving in Low VDIM Range

In the low V_{DIM} range, CC regulation reference, V_{REF} drops by a negative offset in the V_{REF} equation of "$V_{VIN} - V_{OFFSET}$". Therefore, the currents in each LED loads become closer so that the currents of each LED channels are finally equal thanks to NCL30170 V_{REF} generation method as shown in Figure 10.

In the high V_{DIM} range, the duration of LED current conduction in each channel is determined by adjusting the number of LEDs. Increasing the number of first channel LEDs and reducing the number of second and third channel LEDs can reduce the current unbalance. However, it degrades PF and THD.

The tradeoff of PF, THD, efficiency and current balance in each LED channel is described as below.

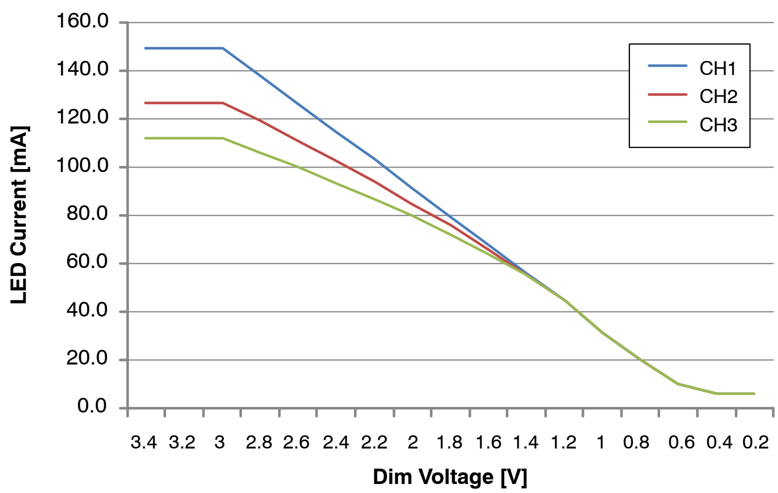
Table 6. LED CHANNEL DESIGN GUIDE

	PF/THD	Efficiency	Channel Current Balance	BOM Cost
Increasing the number of LED channels	Better (If 1st channel V_f is reduced by more number of channels)	Better	Worse	Worse (by more CC regulation FETs)
Increasing the number of series LEDs (total channel V_f)	Little worse (If 1st channel V_f is slightly increased by more series LEDs)	Better	Worse	Worse (by more LEDs)
Increasing the number of 1st channel LEDs (1st channel V_f)	Worse	Better	Better	Same

The number of LED channels would be less than 5 under 100 W design. At higher power design up to 200 W, the number of LED channels needs to be increased to reduce the thermal stress in CC regulation FETs.

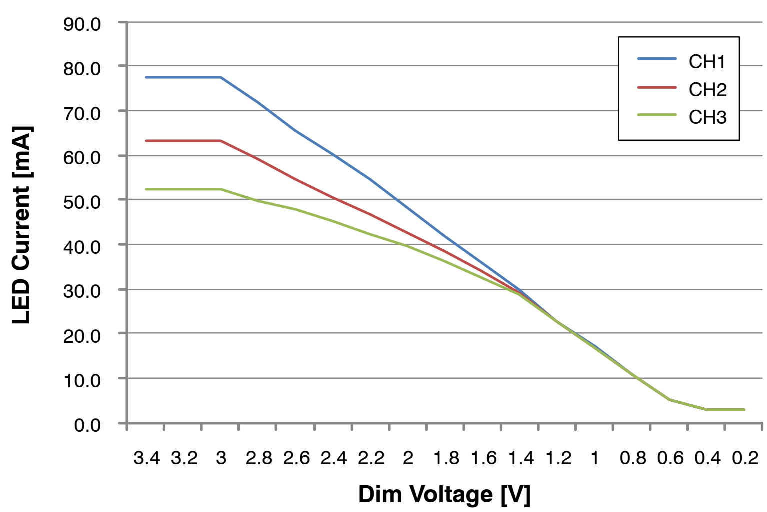
Figure 11 shows the current per channel of an application using 23 LEDs for channel 1, 14 LEDs for channel 2 and 5 LED numbers for channel 3.

Dim Voltage	LED Current [mA]		
	CH1	CH2	CH3
3.4	149.4	126.6	111.7
3.2	149.4	126.6	111.7
3	149.4	126.6	111.7
2.8	137.7	119.1	106.3
2.6	126.3	110.9	99.7
2.4	114.7	102.5	93.5
2.2	103.4	93.8	86.8
2	91.1	84.8	79.9
1.8	79.5	76.1	72.2
1.6	68.1	65.7	64.2
1.4	56.1	55.1	55.0
1.2	44.7	44.7	44.6
1	31.5	31.4	31.4
0.8	19.8	19.8	19.8
0.6	9.7	9.7	9.7
0.4	5.9	5.9	5.9
0.2	5.9	5.9	5.9



a) Low Line Performance for Channel Current at 120 Vac

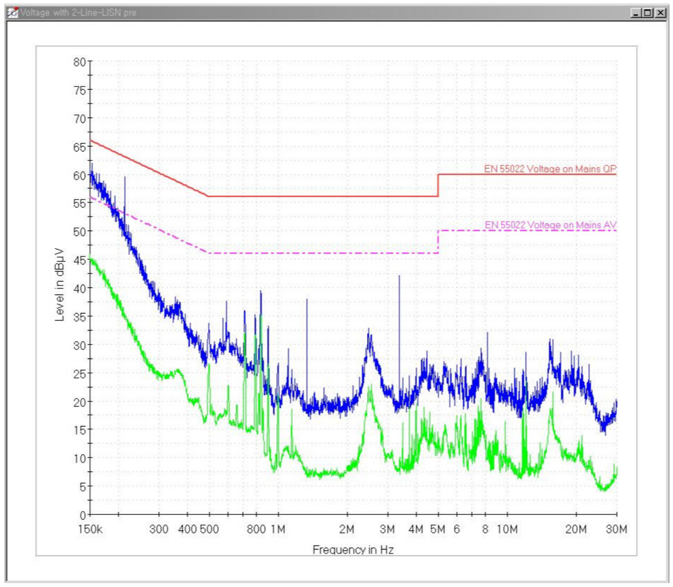
Dim Voltage	LED Current [mA]		
	CH1	CH2	CH3
3.4	77.7	63.3	52.5
3.2	77.7	63.3	52.5
3	77.7	63.3	52.5
2.8	71.8	59.3	49.9
2.6	65.6	54.8	47.7
2.4	60.3	50.6	45.3
2.2	54.6	46.7	42.4
2	48.3	42.6	39.5
1.8	42.0	38.4	36.2
1.6	35.9	34.0	32.6
1.4	29.7	29.1	28.6
1.2	22.9	22.7	22.7
1	17.2	16.8	16.7
0.8	10.7	10.7	10.7
0.6	5.1	5.1	5.1
0.4	2.7	2.7	2.7
0.2	2.7	2.7	2.7



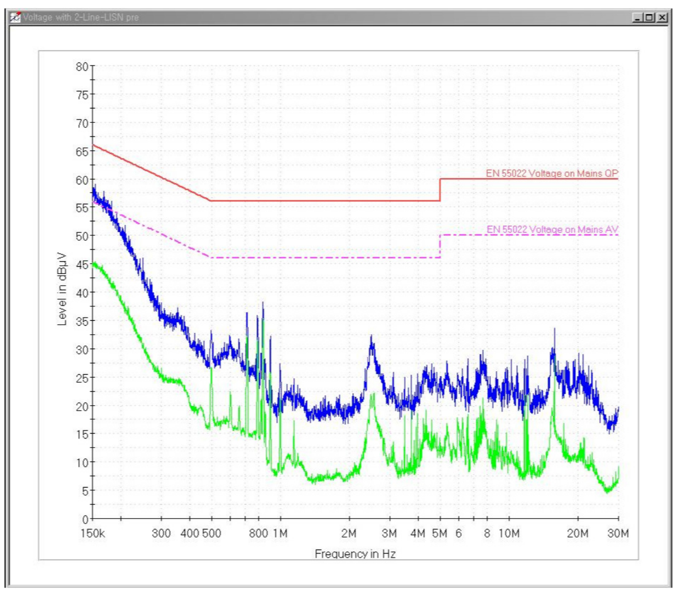
b) Low Line Performance for Channel Current at 220 Vac

Figure 11. Current Balancing at Analog Dimming

Conducted EMI



a) EMI for Low Line



b) EMI for High Line

Figure 12. EMI Test Result

Surge Test

Test Condition:
DM: Differential Mode test applies surge between Line and Neutral
Combination wave: 3strikes

Table 7. TEST RESULT FOR COMBINATION WAVE

Test EVB	Test Result	Surge Immunity Component
20 W Low Line	±2 kV passed	MOV 10D221K (10pi)
20 W High Line	±2 kV passed	MOV 10D391K (10pi)

LAYOUT GUIDANCE

PCB in T−lamp is designed in the form of a long bar. In order to stabilize the CC regulation, PG and SG are separated not to inject the powering noise into the IC control ground as shown in the below figure. Detail layout guidance for controller parts is described in the datasheet.

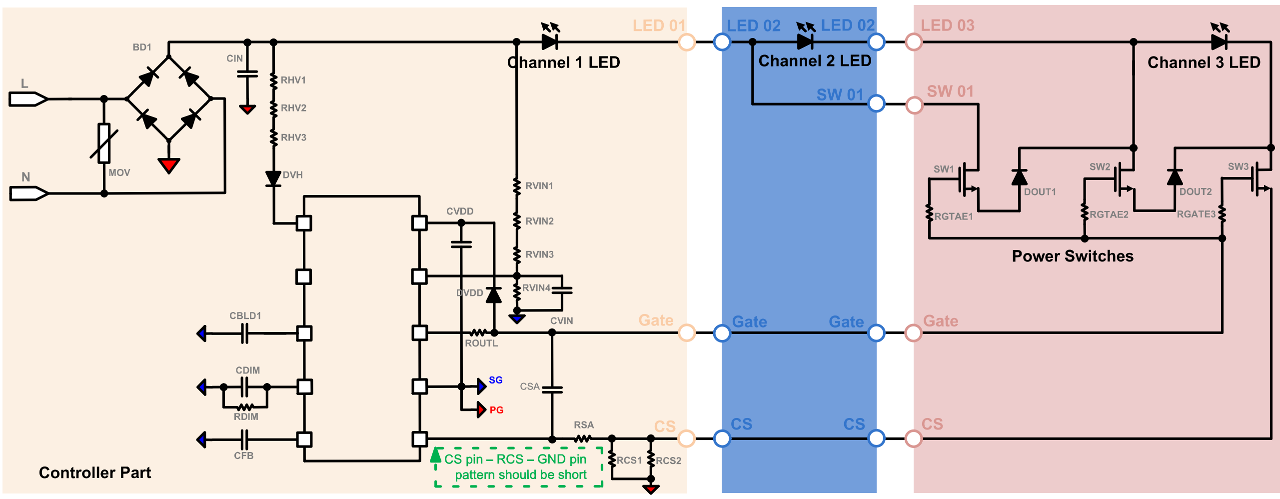


Figure 13. PCB Layout Guidance

Figure 13 is an example of three channels T−lamp design with three separate PCBs. First PCB contains controller part and first channel LEDs and second PCB contains only second channel LEDs. The last PCB is composed of CC regulation switches and third channel LEDs.

CS – RCS – GND distance should be as short as possible. The source of the last channel MOSFET is connected to the CS pin by jumper wires between PCBs which would induce the oscillation in the CC loop. When the CC oscillation happens, the gate resistor (R_{GATE}) of each channel MOSFET relieves the oscillation. When increasing R_{GATE}, THD should be monitored together not to seriously distort the input current by large R_{GATE}.

Figure 14 shows the PCB layout example based on the schematic in Figure 13.

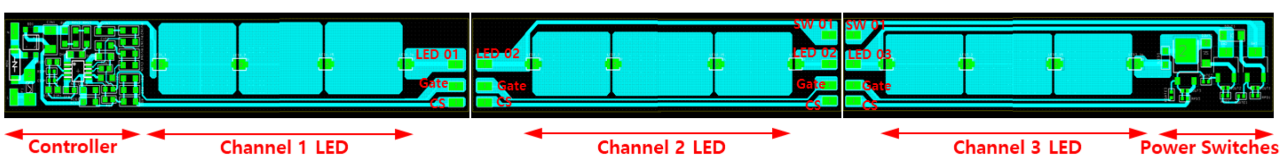


Figure 14. PCB Layout Example

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