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Dv/dt Induced False Turn–on Issue in 4-Switch Noninverting Buck-Boost Converters

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A Gate Drive Design Considerations

USB has evolved from a data interface capable of supplying limited power, to a primary provider of power with a data interface. The latest USB 3.x protocol supports power flow at a much higher level. With a default 5 V voltage, the USB−C port is capable of negotiating with a plugged-in device to raise the port voltage up to 20 V.

A unique challenge in the new power delivery requirement is how to use a 4.5 V−32 V battery voltage to provide a 5 V−20 V DC bus. A 4-switch buck-boost converter is a suitable topology to provide the buck or boost power conversion, because it provides a wide voltage conversion range, positive polarity, high efficiency and a small form factor solution size that designers and customers require.

The power stage of noninverting buck−boost converter consists of four switching devices and an inductor. As shown in Fig. 1, the four switches are grouped into a buck phase (S1 & S2) and a boost phase (S3 & S4). There is one active switch and one rectifying switch in each phase. When using a controller such as ON Semiconductor's NCP81239 controller, this topology can operate in either synchronous buck or synchronous boost mode.

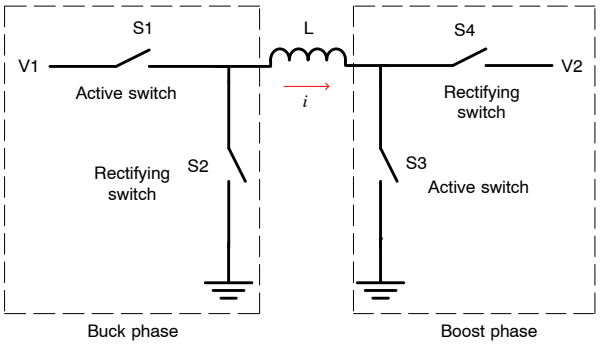


Figure 1. Diagram of a Noninverting Buck-boost Converter

dv/dt Induced False Turn On

In synchronous buck converters, there is a well−known phenomenon called “low side false turn−on,” or “dv/dt induced turn on”, which can be potentially dangerous for the switch itself and the reliability of the entire converter. It occurs when the high−side (active) switch turns on and the drain−to−source voltage of the low−side (rectifying) switch increases rapidly. This sudden voltage increase changes the voltage across the parasitic capacitance (Miller capacitance, C_{gd}) between the drain and the gate, and develops displacement current of $C \times dv/dt$. If a voltage exceeding $V_{gs(th)}$ develops between the gate and source due to the displacement current, it triggers a false turn on of the rectifying switch. The equivalent circuit is shown in Figure 2 and the waveform is shown in Figure 3.

There is limited published information on the dv/dt induced false turn−on problem in a noninverting buck−boost converter, so it is a topic that could benefit from some explanation and demystifying. Errors are made when designers simply copy the circuit parameters of a buck converter directly to the phases of a noninverting buck−boost converter. As this topology gains more popularity in applications, the dv/dt induced turn on issue is becoming more important to understand.

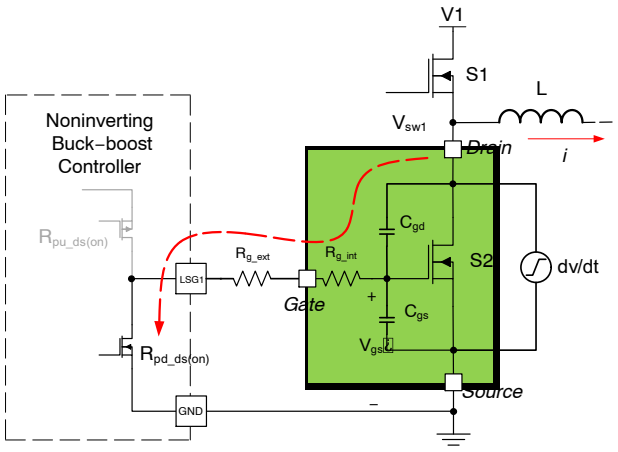


Figure 2. Buck Phase False Turn-on Equivalent Circuit of a Noninverting Buck-boost Converter

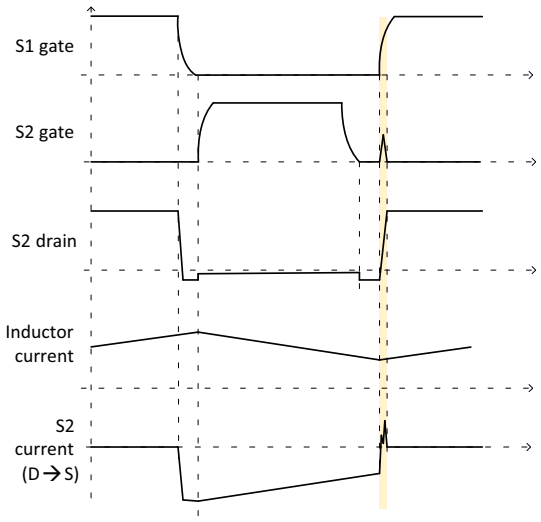


Figure 3. dv/dt Induced False Turn−On Waveform In Normal Operation

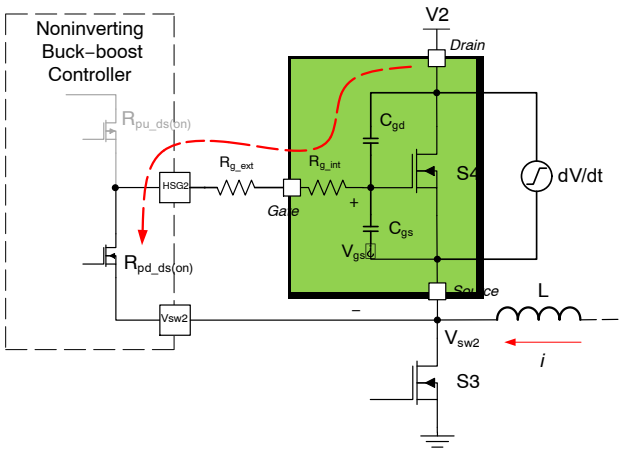


Figure 4. Boost Phase False Turn−on Equivalent Circuit of a Noniverting Buck−Boost Converter

Figure 4 shows a high−side MOSFET of the boost phase of a noninverting buck−boost converter at the moment a positive dv/dt transition appears across the drain−to−source junction. When the low−side MOSFET turns on, the voltage across the drain−to−source of the high−side MOSFET increases rapidly. In off state, a sudden increase in drain voltage changes the voltage across the Miller capacitance (C_{gd}) between the drain and the gate, and develops displacement current of C*dv/dt. If voltage exceeding $V_{gs(th)}$ develops between the gate and source due to the displacement current, it generates a false turn−on signal for the MOSFET. As a result, the MOSFET can be partially turned on, creating a low−resistance path between supply voltage and GND. In severe cases, high power dissipation can develop in the device and results in destructive failure.

Equation (1) shows the voltage across the gate and source in this mode. It is assumed that $dt/C_{gs} >> R_{pd\_ds(on)} + R_{g\_ext} + R_{g\_int}$, most of the displacement current through C_{gd} would ideally flow out of the gate into the gate driver resistors.

$$V_{gs'} \approx (R_{pd\_ds(on)} + R_{g\_ext} + R_{g\_int}) \times C_{gd} \times \frac{dV}{dt} \quad \text{(eq. 1)}$$

If $V_{gs'}$ is lower than the turn on threshold voltage $V_{gs(th)}$, the MOSFET will not turn on. Therefore, the design goal is to limit this dv/dt induced voltage to a maximum of $V_{gs(th)}$ under all conditions. Equation (2) shows the approach:

$$(R_{pd\_ds(on)} + R_{g\_ext} + R_{g\_int}) \times C_{gd} \times \frac{dV}{dt} < V_{gs(th)} \quad \text{(eq. 2)}$$

Note that there are several variables we can tune to satisfy (2). $R_{pd\_ds(on)}$ is from the controller. R_{g_int} and C_{gd} are from the MOSFET. They cannot be controlled once the parts are selected.

Therefore, to increase the converter's dv/dt immunity, a gate drive circuit with very low impedance should be used and higher $V_{gs(th)}$ is preferred. In a drive circuit with low impedance, the cost is high and increasing the $V_{gs(th)}$ is associated with rise in $R_{ds(on)}$. As $V_{gs(th)}$ has a negative temperature coefficient, the possibility of a false turn−on increases as the temperature rises. Typically, gate voltage doesn't go over the threshold voltage and the high device resistance limits the device current. Device destruction due to false turn−on is rare.

Special Case: Light Load and Low Ripple Current Condition

The analysis above is based on the assumption that the inductor current is large enough to discharge the its parasitic capacitor before the rectifying switch turns on, so that the active switch turn on is hard switching and the rectifying switch turn on is soft switching. The minimum inductor current to fully discharge the capacitor is given by:

$$I_{s\_min} \geq (C_{oss1} + C_{oss2}) \times V_1/t_{dead} \quad \text{(eq. 3)}$$

Where I_{s_min} is the inductor current when the active switch turns off. $C_{oss1/2}$ is the output capacitance of the switch and t_{dead} is the dead−time between active switch's turn−off and rectifying switch's turn−on.

A special case appears when (3) is not satisfied. That is when the input and output voltage are close to each other and the load is close to 0. In this situation, the inductor current is too small to fully discharge the output capacitor of the switches. Take the Buck phase for example, in this case, the drain−to−source voltage of the low−side (rectifying) switch is still high at the moment the synchronous rectifying switch turns on. Therefore this voltage is yanked down to 0 rapidly when the rectifying switch turns on. As a result, in complementary, the D−S voltage of the active switch increases to V1 rapidly. This sudden voltage increase (high dv/dt) applied to the parasitic capacitance (Miller capacitance, C_{gd}) between drain and gate develops a displacement current of $i = C_{gd} \times dv/dt$. If the gate voltage developed by the displacement current exceeds $V_{gs(th)}$, a false turn on of the active switch can be triggered.

Similarly, when the active switch turns on, the dv/dt induced false turn on issue still exists, which means we will see a false turn on bump on the gate of rectifying switch when the active switch turns on. The waveform is shown in Figure 5. The analysis is verified by simulation results shown in Figure 6.

The analysis of Boost phase in special case is similar. It will not be discussed in this paper.

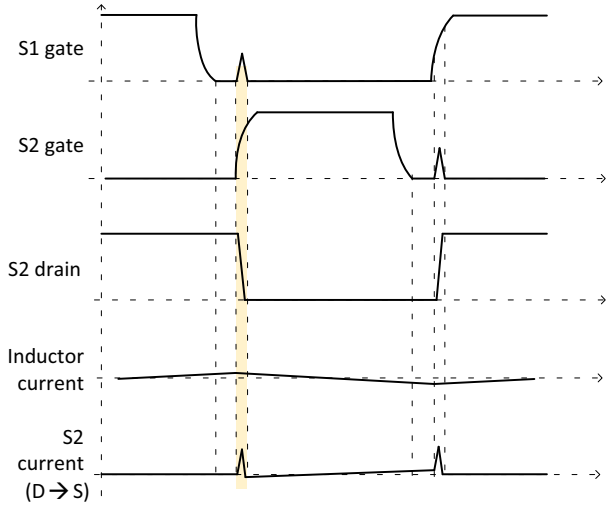


Figure 5. dv/dt Induced False Turn−On Waveform of Light Load and Low Ripple Current Condition

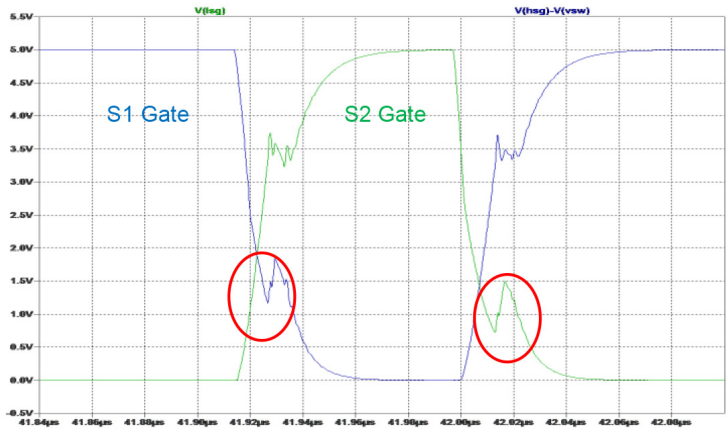


Figure 6. Simulation Results of Light Load and Low Ripple Current Condition

dv/dt slew rate reduction

Equation (2) has provided us the guidelines to resolve this issue. Since it is caused by dv/dt, a first intuitive method is to reduce the dv/dt. The implementation of dv/dt control can be easily done by tuning the gate driver circuit. The active switch's pull up resistance and external gate resistance should be larger than those of the rectifying switch. This would slow down the turn on of the active switch, thus effectively decreasing the dv/dt component of (2).

Figure 7(a) shows a false turn on voltage of 1.9 V at the switching node dv/dt equals to 1.5 V/ns. Figure 7(b) has a reduced false turn on peak voltage to 1.0 V with a 0.75 V/ns dv/dt. It is verified that the magnitude of the false turn on issue can be mitigated by tuning the external gate resistor which affects the dv/dt.

A second solution is to add an RC snubber circuit to the switching node V_{sw1} and V_{sw2}. This is the most direct way to decrease the dv/dt value. The side effect of the method is that the losses will increase.

Last but not least, the dead−time of the rectifying switch turn−off edge to active switch turn−on edge should be also taken care of although it is not shown in (2). Although the dead−time doesn't directly affects the magnitude of the false turn on, it helps to guarantee that the rectifying switch gate voltage drops to zero before turning on the active switch. Noted that even if you set it long enough, the dv/dt induced turn on is still there when the active switch turns on.

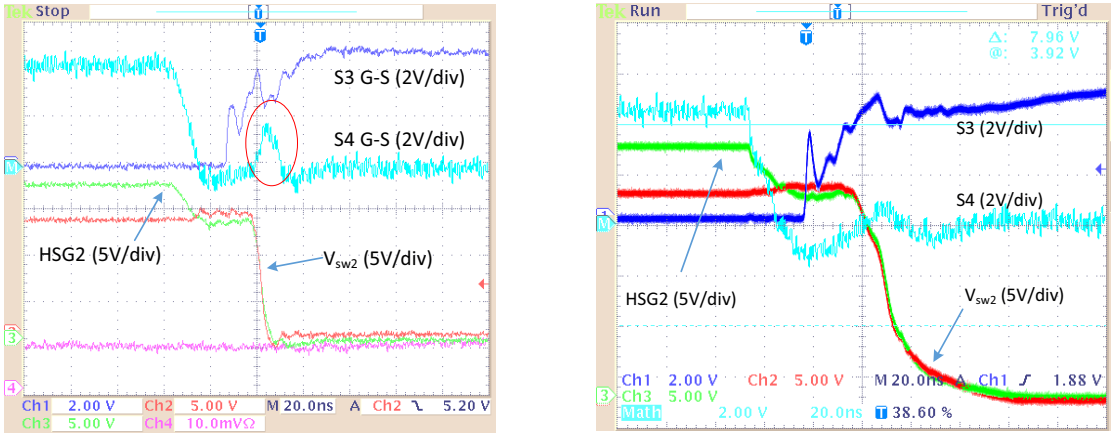


Figure 7. Gate Signal and Switching Node dv/dt with Different External Gate Resistors (a) R_{g_s3} = 0 Ω, R_{g_s4} = 3.3 Ω; (b) R_{g_s3} = 3.3 Ω, R_{g_s4} = 0 Ω

MOSFET Selection

Selecting the right MOSFET can also help to reduce the effect of the dv/dt induced turn−on problem. One solution would be to select the MOSFETs with high gate threshold voltage, but this may lead to increased $R_{ds(on)}$.

In order to prevent dv/dt induced turn−on, the criteria for selecting a rectifying switch would be based on the $Q_{gd}/Q_{gs(th)}$ ratio. $Q_{gs(th)}$ is the gate−to−source charge before the gate voltage reaches the threshold voltage. According to (2), lowering C_{gd} will reduce dv/dt induced voltage magnitude. Moreover, it also depends on dt/C_{gs}, V_{ds} and threshold voltage V_{th}. One way of interpreting the dv/dt induced turn−on problem is when V_{ds} reaches the input voltage, the Miller charge should be smaller than the total charge on C_{gs} at the V_{th} level, so that the rectifying switches will not be turned on. Then we will have the following relation:

$$V_{gs} = \frac{C_{gd}}{C_{gd} + C_{gs}} \times V_{ds} < V_{gs(th)} \quad \text{(eq. 4)}$$

$$Q_{gd} < Q_{gs(th)} \quad \text{(eq. 5)}$$

We can simply use gate charges to evaluate the rectifying device's immunity to dv/dt induced turn on. Ideally, the charge Q_{gd} should not be greater than $Q_{gs(th)}$ in order to leave enough margin.

Alternative Driver Circuit Design

According to (2), the gate drive resistance R_{g_ext} should be kept small in order to make the magnitude of the dv/dt induced false turn−on voltage low. As a result, the rectifying switch turn on and off fast, which is not an issue if it is soft switching. However, as discussed above in the special case, it will cause a false turn on bump if soft switching is not realized.

Some controllers provide an open drain and open source configuration, as shown in Figure 8. It enables customers to control the turn on and turn off speed independently.

In addition to the external gate resistance, the gate drive circuit inside the controller should be reviewed too. Similar to the consideration of R_{g_ext}, the internal pull down resistance for the rectifying switch should be small as well.

There are several other complicated drive circuit techniques such as negative turn off voltage which need extra components. They are not covered in this article.

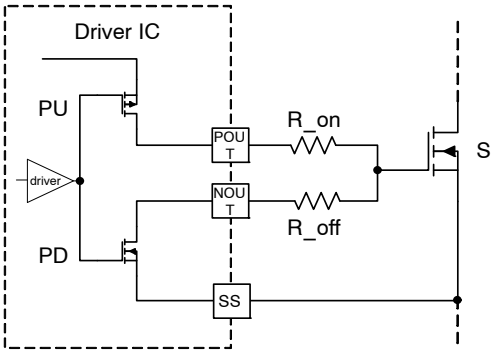
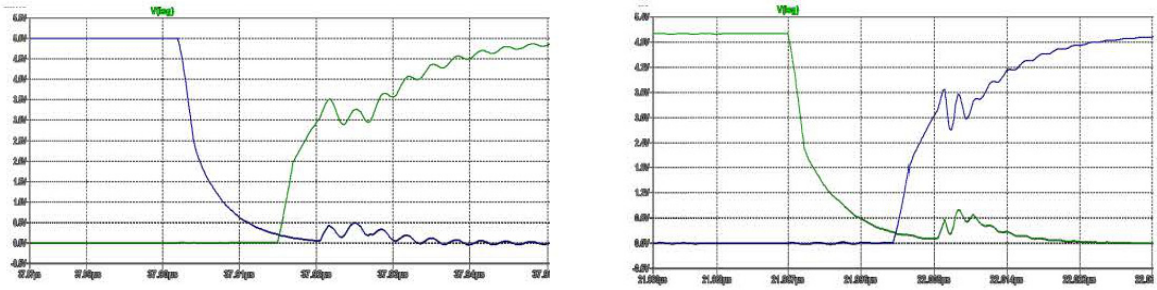


Figure 8. Different Gate Resistance for Turn on and Turn off

Gate Drive Design Considerations for Special Case

As discussed in previous sections, the gate drive circuit for light load and low current ripple condition requires small HS gate resistor and large LS gate resistor, which is right the opposite of the requirement for normal operations. Therefore a tradeoff between normal and special case operation should be considered. The HS gate resistor can be replaced by a resistor in series with the boost−strap capacitor. The LS gate resister should be kept 0. Moreover, the MOSFET selection for active switch should also follow the instructions given in the MOSFET selection section.

Figure 9(a) shows the simulated HS turn off to LS turn on waveform. Figure 9(b) shows the simulated LS turn off to HS turn on waveform. None of the dv/dt induced false turn−on bump exceeds the MOSFET turn on threshold.



(a) (b)

Figure 9. Simulated Improved Switching Waveform of Light Load and Low Ripple Current Condition

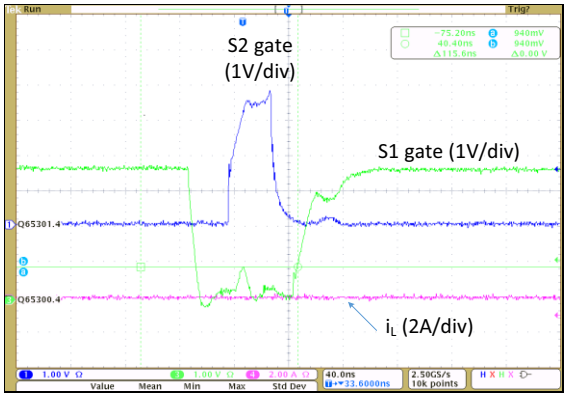


Figure 10. Experimental Improved Switching Waveform of Light Load and Low Ripple Current Condition

Conclusion

Dv/dt induced turn on in a noninverting buck−boost converter is caused by a rapidly rising drain−source voltage at the synchronous rectifying MOSFET in both the buck phase and boost phase. To make things worse, both the active and the synchronous rectifying switch can suffer from this issue in the case where the load current and ripple current are small. As a result, the overall system efficiency deteriorates because of the undesired shoot through currents flowing in either phase leg. Several economical circuit solutions are available to the power supply designers, these include: minimizing rectifying switch turn off gate drive resistance, increasing the active switch turn on gate drive resistance, or adding RC snubber circuit to the switching nodes. Choosing MOSFETs with small $Q_{gd}/Q_{gs(th)}$ ratio and high threshold voltage can also decrease dv/dt induced false turn on possibility.

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[2] Jon Klein. Application Note AN−6003/D, “Shoot−through” in Synchronous Buck Converters, Fairchild Semiconductor.
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[5] Thomas Wu. “CDV/DT induced Turn−on in Synchronous Buck Regulators”, International Rectifier.

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