Drive and Layout Requirements for Fast Switching High Voltage MOSFETs
• Introduction
• Super-Junction Technologies
• Influence of Circuit Parameters on Switching Characteristics
  – Gate Resistance
  – Clamp diodes
  – Ferrite Bead
  – Drive IC
  – External $C_{gd}$
  – Source Inductance
• Practical Layout Requirements
• Summary
E-Field Distribution of SJ Technology

SJ Technology Allows Twice BV for Same Doping

- Planar MOSFET
- Super-Junction MOSFET

- Si limitation: On resistance and BV is trade-off
- On resistance is in linear relation on BV

Area is proportional to BV
Area is twice so BV is twice for same doping thanks to charge balance
Silicon Limit of HV MOSFETs?

\[ \text{Ron, } sp = 6 \times 10^{-9} \text{ BV}^{2.5} \]

- A near linear relation between Rds(on) and Breakdown Voltage
- A significant reduction of conduction and switching losses
- High power density for high-end application.

\begin{align*}
\text{Specific Rds(on) [mohm-cm}^2] & \\
\text{Rds(on) is linear relation on BV} & \\
\text{Breakdown Voltage (V)} & \\
\end{align*}

Results in 10 times lower Rds(on) at 600V

Area is proportional to BV

Area is twice so BV is twice for same doping thanks to charge balance

- Planar MOSFET
- Super-Junction MOSFET

\text{ON Semiconductor®}
Non-linear Coss in SJ MOSFET

• Coss curve of super-junction MOSFET is highly non-linear
  → Extremely fast dv/dt and di/dt and voltage and current oscillation

SJ MOSFET @ Ron=1200, Roff=30Ω vs Planar MOSFET @ Ron=220, Roff=100(Ref.)
## SuperFET3 vs SuperFET2

<table>
<thead>
<tr>
<th>DUTs</th>
<th>SuperFET 3</th>
<th>SuperFET 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FCH040N65S3</td>
<td>FCH041N60E</td>
</tr>
<tr>
<td>BV&lt;sub&gt;DSS&lt;/sub&gt; @ T&lt;sub&gt;j&lt;/sub&gt;=25°C</td>
<td>650 V</td>
<td>600 V</td>
</tr>
<tr>
<td>I&lt;sub&gt;D&lt;/sub&gt; @ T&lt;sub&gt;C&lt;/sub&gt;=25°C</td>
<td>68.0 A</td>
<td>77.0 A</td>
</tr>
<tr>
<td>R&lt;sub&gt;DS(ON)&lt;/sub&gt; max. I&lt;sub&gt;D&lt;/sub&gt;=34A</td>
<td>40mΩ</td>
<td>41mΩ</td>
</tr>
<tr>
<td>V&lt;sub&gt;GS(th)&lt;/sub&gt;</td>
<td>2.5V ~ 4.5V</td>
<td>2.5V ~ 3.5V</td>
</tr>
<tr>
<td>V&lt;sub&gt;GSS&lt;/sub&gt; @ DC</td>
<td>±30V</td>
<td>±20V</td>
</tr>
<tr>
<td>*Q&lt;sub&gt;g&lt;/sub&gt; @ V&lt;sub&gt;dd&lt;/sub&gt;=400V, I&lt;sub&gt;D&lt;/sub&gt;=34A, V&lt;sub&gt;gs&lt;/sub&gt;=10V</td>
<td>* 158 nC  -52%</td>
<td>* 330 nC  0%</td>
</tr>
<tr>
<td>*R&lt;sub&gt;g&lt;/sub&gt; @ f = 1 MHz</td>
<td>* 0.7 Ω</td>
<td>1.2 Ω</td>
</tr>
<tr>
<td>*E&lt;sub&gt;OSS&lt;/sub&gt; @ 400V&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>* 13.7 uJ  -47%</td>
<td>* 25.7 uJ</td>
</tr>
<tr>
<td>*Q&lt;sub&gt;OSS&lt;/sub&gt; @ 400V&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>* 521 nC  -13%</td>
<td>* 596 nC</td>
</tr>
<tr>
<td>Peak diode recovery dv/dt</td>
<td>20V/ns</td>
<td>20V/ns</td>
</tr>
<tr>
<td>MOSFET dv/dt</td>
<td>100V/ns</td>
<td>100V/ns</td>
</tr>
</tbody>
</table>
Gate Charge Characteristic
SuperFET3 - Low Gate Charge and Input Capacitance

Notes:
1. $V_{GS} = 0$ V
2. $f = 1$ MHz

$C_{iss} = C_{gs} + C_{gd}$ ($C_{ds}$ = shorted)

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<th>DUTs</th>
<th>FCH040N65S3</th>
<th>FCH041N60E</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{gs}$</td>
<td>39.8</td>
<td>57.1</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>63.8</td>
<td>121.0</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>157.9</td>
<td>330.2</td>
</tr>
</tbody>
</table>
Clamped Inductive Switching Circuit & Waveforms and Loss Definition

- Test Circuit which is used for the following measurements.
Effects of Gate Resistance at Turn On Transient
Effects of Gate Resistance at Turn Off Transient

- Gate-Source Voltage [V]
- Drain-Source Voltage [V]
- Drain Current [A]
- Poff [W]

For different values of $R_g$: 3.3 ohm, 6.8 ohm, 10 ohm, 27 ohm, 47 ohm.

- Time [ns] range from -100 to 60.
- Voltage and current values are shown for each resistance value.
Effects of Gate Resistance

- Critical control parameter in gate-drive design is external series gate resistor (Rg).
- From an application standpoint, selecting the optimized Rg is very important.
  - Efficiency vs dv/dt or voltage spikes.
Reverse Recovery Effect

Si Diode vs SiC Schottky Diode

- MOSFET Q, Waveforms
- Boost Diode D, Waveforms
- MOSFET Switching Losses

![Diagram showing reverse recovery effect for Si diode vs SiC Schottky diode](image-url)
Effect of Clamp Diodes at Turn On
Si Diode vs SiC Schottky Diode

Diode & MOSFET waveforms @ Turn-on with SiC Schottky diode

Diode & MOSFET waveforms @ Turn-on with Si diode
Effect of Clamp Diodes at Turn Off
Si Diode vs SiC Schottky Diode

Turn off @ $I_d=1\text{A}$, $R_g=4.7\ \Omega$ with 6A SiC SBD (Ref: 8A Si Diode)
Effect of Clamp Diodes
Si Diode vs SiC Schottky Diode

• SiC Schottky diode is optimized device for extremely fast switching MOSFET.
Effects of Ferrite Bead

(a) Vgs at Turn-on Transient
(b) Vgs at Turn-off Transient
Equivalent Circuit of Ferrite Bead

\[ Z = R + jX \]
Effects of Current Capability of Driver IC

TABLE I. Comparisons of Critical Specification of Gate Drivers

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>CONDITION</th>
<th>IPK_SINK</th>
<th>IPK_SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN3122T</td>
<td>C_LOAD=1.0uF, f=1kHz, Vdd=12V</td>
<td>11.4[A]</td>
<td>-10.6[A]</td>
</tr>
<tr>
<td>FAN3224T</td>
<td>C_LOAD=1.0uF, f=1kHz, Vdd=12V</td>
<td>5.0[A]</td>
<td>-5.0[A]</td>
</tr>
<tr>
<td>FAN3111C</td>
<td>C_LOAD=1.0uF, f=1kHz, Vdd=12V</td>
<td>1.4[A]</td>
<td>-1.4[A]</td>
</tr>
</tbody>
</table>

* DUT : FCP16N60N with 6A SiC SBD
Effects of Gate Drive Circuit

- PNP Tr turn-off can reduce gate ringing.
- It’s possible to reduce parasitic components in PCB.
- Keep loop area as small as possible to avoid worse EMI and switching behavior.

* Ron=10hom, Roff=4.7ohm
Probes are circuits composed of distributed R, L, and C for AC signals. → A total probe impedance varies with switching frequency.

The probe ground lead adds inductance to the circuit.
Keep the Loop Probe Small!

- Measurement with standard setup
- Measurement with Probe Tip
Package and Layout Parasitics

A lot of layout parasitic has to be considered!

1cm / 0.25mm trace \((L/W) \approx 6-10nH\)

\[ L=10nH, \frac{di}{dt}=500A/\mu s \rightarrow V_{ind}=5V \]
\[ L=10nH, \frac{di}{dt}=1,000A/\mu s \rightarrow V_{ind}=10V \]
MOSFET Oscillation Circuit

A lot of layout parasitic has to be considered!
Layout Capacitance
Example with High External $C_{GD}$

$$A = x \cdot y$$

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}$$

Capacity between trace pitches

(a) Single layer PCB

(b) Double layer PCB

External $C_{GD}$ too high!!
Layout Capacitance
Examples with Reduced External $C_{GD}$

Both solutions allow use of SJ Devices

(a) double layer PCB

(b) multi layer PCB
Layout Example Large External $C_{GD}$

$V_{gs}$ Shows Higher Spikes During Turn Off

PCB example with large external $C_{GD}$
Layout Example Small External $C_{GD}$
Vgs Shows Lower Spikes During Turn Off

PCB example with small external $C_{GD}$

Coupling area
Gate
Drain

$V_{DS}$
$V_{GS}$
$D_{VGS} \sim 4V$
Turn-off Gate Oscillation Mechanism

During T<sub>2</sub>

- Keep the commutation loop as small as possible!
- Minimize the source inductance and sensing resistor inductance
Effects of Source Inductance
LS=1n and 10nH

(a) $V_{gs}$ waveform for low $L_S$

(b) $V_{gs}$ waveform for High $L_S$

(c) $V_{ds}$ and $I_d$ waveform

* Topology : 500W Interleaved CRM PFC
* MOSFET : FCPF13N60N
* Diode  : FFPF20UP60DN
* Gate Resistor : Ron=51ohm, Roff=10ohm
### Gate oscillation vs Package

**Through hole vs SMD vs Kelvin source SMD**

<table>
<thead>
<tr>
<th></th>
<th>600V/199mΩ, Power88</th>
<th>600V/199mΩ, D2PAK</th>
<th>600V/199mΩ, TO220</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_D=8A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Kelvin Source SMD</td>
<td><img src="image1.png" alt="Graph" /></td>
<td><img src="image2.png" alt="Graph" /></td>
<td><img src="image3.png" alt="Graph" /></td>
</tr>
<tr>
<td>SMD</td>
<td><img src="image4.png" alt="Graph" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Through hole</td>
<td><img src="image5.png" alt="Graph" /></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Turn-off Transient**

- **Gate Oscillation**
- **Gate Oscillation**
Design Tips - Practical Layout Example – Boost PFC

**Bad Layout:**
- Increased external G-D capacitance
- Driver and gate resistor far away from gate pin of MOSFET
- Long gate path

**Good Layout:**
- Connect the driver-stage Gnd directly to the source pin to achieve best performance
- Driver & Rg as close as possible to the gate pin of MOSFET
- Separate Power GND and gate driver GND
Design Tips - Practical Layout Example
- Paralleling MOSFETs

Two independent totem pole drivers very close to MOSFET gate

Minimized source inductance to reference point for gate drive minimized

Minimized Cgd:
Gate and Drain trace at 90° angle
Summary
How to Use Super-Junction MOSFET in Practical Layouts

• To achieve the best performance of Super-Junction MOSFETs, optimized layout is required

• Gate driver and $R_g$ must be placed as close as possible to the MOSFET gate pin

• Separate POWER GND and GATE Driver GND

• Minimize parasitic $C_{gd}$ capacitance and source inductance on PCB

• For paralleling Super-Junction MOSFETs, symmetrical layout is mandatory

• Slow down $dv/dt$, $di/dt$ by increasing $R_g$ or using ferrite bead