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The Quest for Power Density

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ABSTRACT

In recent days, power density has become an important and increasingly universal figure of merit of power supply and power system innovation and performance. Achieving high power density implies the utilization of the latest topological advances in power conversion, employing state-of-the-art control methods and using the best semiconductor technology available for the designer.

This paper outlines the reasons designers should consider high power density as a general goal and the fundamental principles high power density designs are based on, including topology and semiconductor selections.

A closer look at GaN power devices, their key characteristics, drive and layout requirements, impact on topology selection and their best application areas will also be discussed.

INTRODUCTION

Power supply designers working in virtually any market segment strive to meet four basic objectives in their every day work. These are:

- high efficiency,
- high reliability,
- small size and
- low cost.

High efficiency is often required to meet certain government or industry standards and expectations. Reliability is a fundamental requirement demanded by all customers across the board. Small size is mandated by many applications with space constraints and low cost is just the way financial objectives are managed in today's competitive business environment.

The power supply industry is capable of meeting all of these requirements. Efficiency figures in the high 90th percentiles are reported regularly in literature and can be found easily in product offerings from major manufacturers. Reliability of power supplies and especially redundant power systems can meet the most stringent constraints, providing life span beyond the existence of the technology itself they are powering. In addition to these tremendous improvements in performance, the industry has also managed to reduce power supply prices on the \$/Watt scale and provide even bigger savings in total cost of ownership in power management applications by reducing electricity usage, cooling needs and installation footprint.

The challenge for the power supply industry and the designer is to satisfy all four of these design objectives at the same time.

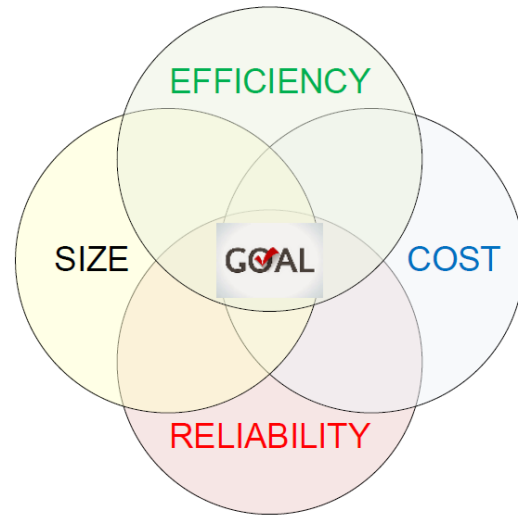


Figure 1. The Ultimate Optimum Trade-off

The antagonistic relationships among these areas are clear to even the casual observer; heightened efficiency and reliability requirements, for example, might negatively impact the cost target and, in many cases, the size of the power supply as well.

In addition, market forces and advances in applied technologies further muddle the tradeoffs in front of the power supply designer. The constant cost pressure of the market can be mitigated by minimizing the risks and time-to-market or utilizing mature technologies where component and material prices offer year-on-year price reduction. Re-using proven circuit solutions optimized through previous product cycles might also lead to cost effective solutions. On the other hand, customer expectations in performance and functionality, competition and the need for differentiation call for innovation and might lead to a more expensive approach.

POWER DENSITY

The importance of power density is not obvious; it is rather well hidden behind other factors. As a matter of fact, this very important figure of merit cannot be explained or justified when it is considered as a standalone number.

High power density is often a “nice to have” feature to the users or the manufacturers of power supplies, or both. But implementing higher power density designs often costs more due to complex mechanical designs, potentially more expensive active and passive components and the need for state-of-the-art control algorithms. The increased cost of the power supply must be offset somewhere else to make high power density financially viable.

The most noticeable benefit of high power density is the resulting size reduction of the power delivery solutions.

Miniaturization of the power supplies enables new markets and applications where size is a paramount concern, for example portable electronics and medical applications such as implantable or swallowable diagnostic and therapeutic devices.

Smaller size leads to reduction of raw material consumption which can significantly reduce component cost and ultimately the cost of the power supply. Furthermore, fewer and smaller components imply weight reduction. Lighter weight could be an important convenience factor for mobile applications, not just in portable consumer electronics but also any power delivery solutions which are not stationary. A great example is transportation where weight reduction can be directly measured in fuel savings or extended operating range.

In stationary applications such as data centers and telecommunication, and industrial applications, the smaller footprint of the power supply frees up valuable board or cabinet space for the primary, useful purpose of the installation or solution. Additional features can be realized without the penalty of increased size.

The fact to be recognized behind these examples is that all of these benefits create value on the system level which can be measured monetarily only if the entire system is examined. This financial gain, achieved by creating new markets, increasing functionality and lowering the total cost of ownership, is the ultimate force to drive the industry for higher and higher power densities in today's power delivery solutions.

ENABLING HIGH POWER DENSITY

When power density is increased, the size – the volume and the surface area – of the power supply will decrease. To maintain a safe temperature rise of the system, the amount of heat dissipation has to be decreased which means that the power supply's efficiency must be increased. The relationship among an object's temperature rise above the ambient, the area available for heat removal and the amount of heat dissipated is governed by Newton's law of cooling:

$$q = h \times A \times \Delta T \quad (\text{eq. 1})$$

where q is the amount of heat transferred via convection, h is the heat transfer coefficient, A is the available surface area and ΔT is the temperature rise of the object.

The maximum amount of heat generated in the power supply is a function of its efficiency and rated output power, and the surface area is a function of the volume of the power supply. Therefore, Equation 1 can be modified to express the relationship between efficiency and power density:

$$\eta = 1 - \frac{h \times r_{VA}(V) \times \Delta T}{\text{Power Density}} \quad (\text{eq. 2})$$

where $r_{VA}(V)$ is the ratio between the volume and surface area of the power supply. Note, that the $r_{VA}(V)$ ratio is

strongly dependent on the shape and the total volume of the enclosure of the power supply. In addition, h is a function of material, surface smoothness and the properties of the cooling agent. Forced convection – forced air cooling – will also change the values of many of the parameters.

Figure 2 shows the required efficiency of a small USB charger as a function of power density. In this example, the size, shape and maximum allowable temperature rise of the unit are kept constant to demonstrate the relationship between power density and efficiency exclusively.

As it can be seen, efficiency is the gate keeper to denser integration and to achieve high power density. As higher efficiency reduces heat dissipation, it consequently also decreases cooling requirements.

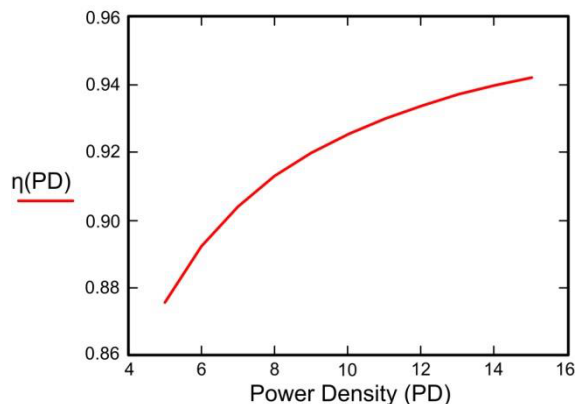


Figure 2. Efficiency as a Function of Power Density

EFFICIENCY

Even without considering its effect on power density, efficiency is an important parameter which can not be ignored. Energy prices, government regulations, differentiation in the market place – just to mention a few motivations – are all creating a need for high efficiency. The efficiency of power delivery solutions are continuously inching higher and higher. This trend can be attributed to many factors such as strict enforcement of efficiency and power quality guidelines, persistent improvement in component performance and the maturing of the industry.

Achieving state-of-the-art efficiency results, which are imperative to push power density significantly higher in a power supply, is more complex than selecting the best available components.

TOPOLOGY

Topology selection and choosing the optimum operating principle are the first key tradeoffs in front of the designers. To facilitate high efficiency, soft-switching or resonant power conversions are often favored over hard-switching solutions. In many cases, the same topology can be operated either in hard-switching, soft-switching or resonant modes of operation. Figure 3 shows the schematic diagram and

current waveforms of a full-bridge converter working in three different operating modes; hard-switching, soft-switching and resonant power conversion.

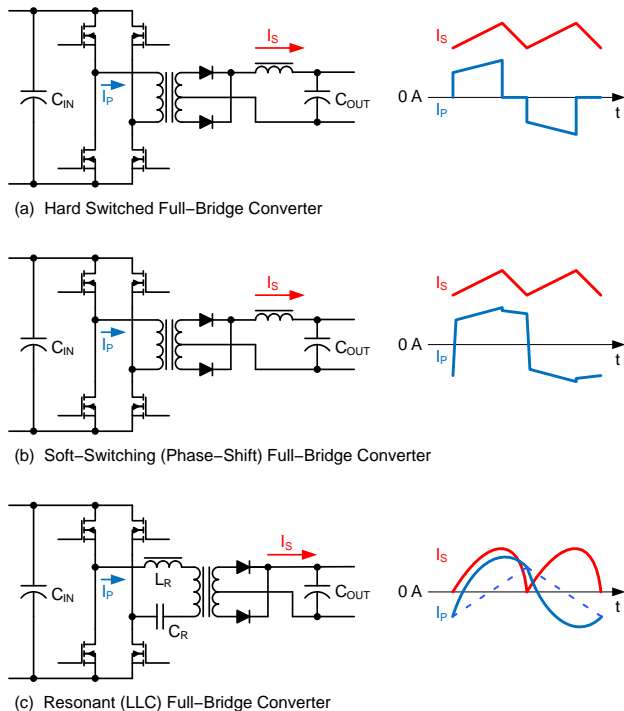


Figure 3. Three Operating Modes of a Full-bridge Converter

Soft-switching or resonant mode operation might require careful balancing of conduction losses and switching losses as these modes of operation might necessitate higher ripple currents to maintain efficient operation (soft switching at light load or sufficient resonant energy for rated output power). Resonant mode of operation could further increase the RMS current and voltage stresses, impacting component selections. To mitigate the problem, mixed mode operation can be introduced where the controller would select the optimum operating mode based on the operating conditions.

The main benefit of soft-switching and resonant converters is the significant reduction in switching losses through zero voltage (ZVS) and/or zero current (ZCS) switching. The resulting efficiency improvement can be utilized to raise the switching frequency and/or reduce cooling requirements. The outcome in both cases – or as a

combination of the two – is increased power density. The higher operating frequency also allows size reduction in the passive components of the system.

FAST SEMICONDUCTOR DEVICES

Fast switching devices such as the latest generation super junction MOSFETs, SiC MOSFETs or GaN power switches are essential to reduce switching losses and to accommodate higher frequency operation with low losses. These devices are capable of switching between their on – off states in the fraction of the time of the older generation semiconductor devices yielding much lower E_{ON} and E_{OFF} energy losses.

To take advantage of the faster switching characteristics of these devices, semiconductor companies introduced low parasitic inductance packaging to ensure proper operation. In addition, the power supply designer – primarily the PCB layout designer – must use the best practices available for reducing parasitic inductances. The all around low-inductance approach eliminates unwanted resonances and provides a much tighter control of timing delays that were traditionally acceptable for lower speed solutions.

In particular, common source inductance can have a very negative impact on switching performance as it will be shown later in Chapter Gate Drive Design.

CONTROL ASPECTS

The importance of advanced control algorithms have been highlighted earlier when considering operating mode changes and optimization of light-load behavior. But another aspect of high performance control solutions must be pointed out as well, as it can influence power density in an indirect but significant manner.

Advances in process technology and abundant availability of relatively small feature size, affordable CMOS processes opened up the path towards much more accurate threshold tolerances, timing accuracies and faster speed in today’s high performance power supply controllers. The benefits of this tighter control can be measured by the reduced requirement to “over design” our power supplies in power handling capability and consequently from a thermal dissipation point of view. Hence, tighter control could be an important tool to further enhance power density. Table 1 highlights the impact of tolerances of the most significant control aspects on the system parameters and corresponding components.

Table 1. TIMING AND ACCURACY IMPACT OF CONTROL ON POWER SUPPLY DESIGN

	Function	Parameter	Impact	Components
Timing Accuracy	Oscillator	Switching frequency	Output ripple, EMI	C_{OUT} ; TR; L
	D_{MAX} Clamp	Max. on-time	Max. V·s	TR; L
Propagation Delay	Current Limit	Peak currents	Max. I_D ; I_L	TR; L; Q; D
	Compensation	Phase margin	Stability	

Table 1. TIMING AND ACCURACY IMPACT OF CONTROL ON POWER SUPPLY DESIGN (continued)

	Function	Parameter	Impact	Components
Threshold Accuracy	Current Limit	Peak currents	Max. I_D ; I_L	Cooling
	Protection	Voltage stresses	Max. V_s ; V_{DS} ; etc.	C_{IN} ; C_{OUT} ; Q; D; TR; L

Note that at higher switching frequencies, propagation delay becomes much more important as it could become a significant fraction of the switching period. Accordingly, its impact on stability could be more severe and it requires much more attention.

As it is shown, enabling high power density designs can be a complex task where the choice of topology, component selections, advanced control, and physical implementation details all play a critical role in achieving the ultimate goal. Ignoring any of these aspects and their interactions might doom the entire effort.

Table 2. WIDE BAND GAP CHARACTERISTICS

	Si	SiC	GaN	Units
Band Gap Energy	1.1	3.3	3.4	eV
Breakdown Field	0.3	2.1	2.1	MV/cm
Saturation Velocity	10	22	25	$\times 10^6$ cm/s
Thermal Conductivity	1.5	5	1.3	W/cmK

Band gap energy is the measure of energy needed to unbind an electron from an atom and make it move freely in the material, i.e. to carry electric current. The higher band gap energy generally indicates more predictable behavior and better performance over temperature variations.

The distance required to withstand a given potential difference – referred to as breakdown voltage in semiconductors – is proportional to the breakdown field strength. As can be seen, wide band gap materials are seven times better than silicon in this respect. That means that devices with similar voltage ratings can be smaller, and the electrons must travel a shorter distance during conduction.

Electron mobility, primarily electron saturation velocity, is basically the average speed of the current carrying electrons in the material. In a simplified, first-order approximation, a higher number implies faster switching speed and lower on-resistance.

Finally, thermal conductivity relates to how high the operating temperature of the device can be pushed. This comparison explains why silicon-carbide is our primary choice of material for high-temperature applications, easily surpassing the performance of other semiconductor options shown in Table 2.

Fundamental capabilities are summarized in Figure 4 for popular semiconductor materials.

WIDE BAND GAP TECHNOLOGY

One of the most promising emerging technologies leading towards high power density solutions is wide band gap semiconductors. This entirely new breed of power devices offers higher electric field strength and electron mobility compared to traditional silicon technology. Table 2 shows the basic characteristics of these new semiconductor materials with respect to silicon.

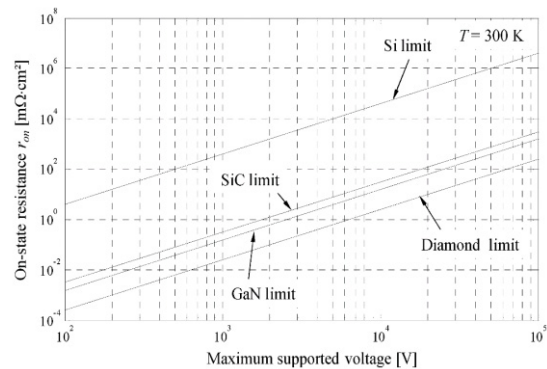


Figure 4. Theoretical Voltage and on Resistance Limits

Wide band gap devices – SiC and GaN – are showing very similar improvements over silicon power transistors. But in reality, the two wide band gap technologies are very different.

SiC MOSFET devices are very similar in structure and operating principle to their silicon counterparts. In a SiC device, the applied gate voltage causes free electrons to move to the depletion region and form a conducting channel. SiC MOSFETs can be built either as planar or trench devices

just like Si MOSFETs. They are vertical devices which mean that current is flowing through the device between the top and bottom surfaces.

On the other hand, the operation of the GaN devices is based on the naturally-present two-dimensional electron gas (free moving electrons available to carry current) between the undoped GaN layer and the n-doped AlGaIn layer of the transistor. Therefore, the basic structure of the device had to be modified to create a normally-off transistor – called eMode GaN – which is the preferred device for power applications. Another huge difference is that the GaN device structure dictates a lateral arrangement of the terminations – at least for now. This means that current is flowing parallel to the surface of a GaN device and because there is no practical likelihood to create overlap among the drain, source and gate electrodes, the intrinsic C_{DS} , C_{GS} and C_{GD} capacitances are drastically reduced.

Bearing in mind high power density requirements, the extremely low capacitances of GaN power switches set them apart from competing solutions and make them a perfect fit for high efficiency, high frequency and fast switching power conversion applications.

GaN POWER TRANSISTORS

The application area for GaN power transistors is divided into two distinct voltage domains. Low voltage GaN devices have a breakdown voltage up to 200 V and this market segment is dominated by the normally-off, eMode devices. High voltage applications refer to the 200 V to 650 V range and offer either a “cascoded GaN” or eMode solution.

Figure 5 depicts the cascoded GaN implementation, where a normally on GaN transistor is connected in series with a low voltage, low $R_{DS(on)}$ silicon MOSFET forming a normally-off arrangement.

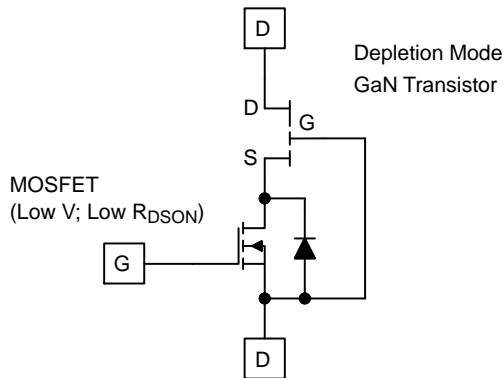


Figure 5. Cascodes GaN Power Switch

This solution has a few fundamental disadvantages. Using two discrete semiconductor devices will increase packaging complexity, negatively impact on-resistance and increase the minimum achievable parasitic inductance. The control electrode is the gate of the low $R_{DS(on)}$ (large die size) MOSFET which offers margin for gate drive amplitude

transients but increases gate drive losses due to larger capacitance. This larger gate capacitance in combination with the higher packaging inductances might impact the switching speed of the device, making it very difficult to realize the true capability of the GaN technology. Other problem areas might include the potential avalanche breakdown of the silicon MOSFET transistor during the turn off transition and oscillations frequently observed at the gate of the GaN device.


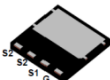
Even though the cascoded GaN implementation was introduced first for high voltage GaN applications, eMode devices are catching up quickly and becoming the preferred devices for the 650 V node as well.

Because of its popularity and ease of use compared to cascoded GaN solutions, the rest of this paper will focus on the device characteristics and applications of eMode GaN power transistors.

GaN vs. Si ON THE DEVICE LEVEL

The comparison of a potential GaN power switch to its Si counterpart can be done by looking at the critical parameters of their respective datasheets influencing the switching performance of the device. Starting at the high-voltage node (650 V rated devices), Table 3 gives a quick contrast between the two technologies. The numbers in the ratio column indicate how much better (green) or worse (red) certain parameters of the GaN power switch are relative to a close equivalent silicon MOSFET transistor.

Table 3. PARAMETRIC COMPARISON FOR 650 V DEVICES

	Gan Systems	ON	Ratio
Package			
$B_{VDSS}(V)$	650	650	1
$I_D(A)$	15	30	2
$R_{DS(on)}(m\Omega)$	100	99	1
$C_{ISS}(pF)$	130	2270	17.5
$C_{O(ER)}(pF)$	44	74	1.7
$C_{O(TR)}(pF)$	71	500	7.0
$C_{RSS}(pF)$	1	no data	–
$Q_G(nC)$	3	56	18.7
$Q_{GD}(nC)$	0.84	23	27.4
$V_{GS,MAX}(V)$	+7 / -10	+/- 30	4.3
$V_{GS,TH}(V)$	1.3	3.5	2.7
$R_G(\Omega)$	1.35	0.5	2.7

The first thing to notice is the reduced continuous current rating of the GaN device. But it is important to understand

that this is primarily caused by the package thermal resistance from junction-to-case, which shows the same ratio as the continuous current ratings (not true for wafer level CSP).

As it can be observed, all capacitances and gate charge figures exhibit a tremendous improvement compared to silicon technology. The lowest improvement across the board is being in C_{OSS} which is not even half of silicon. On the other hand, the reverse transfer capacitance between the gate and the drain of the GaN devices is almost completely eliminated. The gate-to-source capacitances of the GaN devices – especially the high-voltage GaN devices – are much lower, facilitating very fast turn-on and turn-off transitions even with a relatively weak driver.

The gate isolation of the GaN devices seem to be much more fragile and the voltage rating has dropped significantly compared to silicon. Depending on the proprietary technologies of different vendors, the GaN devices require a 4.5 V to 6.5 V gate drive amplitude. In any case, the maximum gate drive voltage the device can withstand is only about 2 V higher than their respective gate drive amplitudes. This will be further discussed when we analyze gate drive requirements for these devices.

Continuing with the gate characteristics, the threshold voltage is also reduced which is advantageous considering the lower gate-source voltage rating. It is also important to highlight that the GaN device thresholds have negligible variation over temperature due to the larger band gap energy.

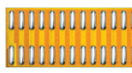
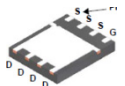
Internal gate resistance of any switching device is an important parameter because the gate drive current is limited by this intrinsic impedance associated with bringing the control signal to the die and distributing it on the die itself. The two examples in Table 3 and Table 4 demonstrate that this parameter is very much package and device layout dependent and it can be better or worse depending on the actual implementation rather than on the technology itself.

Table 4 confirms that the low-voltage GaN technology offers similar pros and cons as the high-voltage node.

There are additional differences between GaN and Si devices which are not that obvious based on the datasheet parameters. The user might have to dig deeper and study the principles of operation, physics and parametric graphs of the datasheet of the devices.

GaN power transistors are capable of bi-directional current flow. When the device is turned on, the $R_{DS(ON)}$ is the same, independent of the direction of the current. When the device is off, it is blocking positive current flow – from the drain towards the source terminal – as it is expected. In reverse direction – from the source towards the drain – current can flow similarly to current flowing through the body diode of a MOSFET. But in GaN devices there is no parasitic pn junction like the body diode of a MOSFET. The current does flow through the same conduction region which is utilized for positive current flow. The difference is that the voltage drop across the drain-source terminals is approximately 3 V in the third quadrant operation. Furthermore, because there is no pn junction, there is no stored charge, and consequently no reverse recovery effect when the current is removed from the device.

Table 4. PARAMETRIC COMPARISON FOR 40 V DEVICES

	EPC	ON	Ratio
Package			
$B_{VDSS}(V)$	40	40	1
$I_D(A)$	90	290	3.2
$R_{DS(ON)}(m\Omega)$	1.2	1.2	1
$C_{ISS}(pF)$	1920	12500	6.5
$C_{O(ER)}(pF)$	2050	3430	1.67
$C_{O(TR)}(pF)$	2240	no data	–
$C_{RSS}(pF)$	29	136	4.70
$Q_G(nC)$	18	173	9.6
$Q_{GD}(nC)$	2.4	18	7.5
$V_{GS,MAX}(V)$	+6 / -4	+/- 20	3.3
$V_{GS,TH}(V)$	2.1	1.5	1.4
$R_G(\Omega)$	0.3	1	3.3

It is worthwhile to mention that GaN devices have the highest gain (transconductance) among all power switches. This is important for two reasons; close to the threshold voltage, a very small change in V_{GS} can cause a large and rapid change in the device current. For fast-switching applications, this is a great benefit of the GaN devices. The large gain also poses a danger if the control voltage (V_{GS}) doesn't pass through the so called "linear region" quickly. In linear mode, V_{GS} controls the current in the transistor and when V_{GS} lingers around this voltage level too long, the device might be susceptible to oscillations. Therefore it is imperative that the gate drive signal of a GaN power transistor has very fast rise and fall times.

A somewhat disadvantageous property of the GaN technology is that the device's $R_{DS(ON)}$ has a larger positive temperature coefficient than silicon MOSFETs. That means that the $R_{DS(ON)}$ of the device increases more rapidly with increasing junction temperature. Also, note that positive temperature coefficient of the $R_{DS(ON)}$ is imperative for paralleling devices and higher TC leads to better current sharing among parallel connected transistors.

The most negative characteristic of GaN technology is the extremely limited avalanche energy capability of these devices. For all practical purposes, the maximum drain-source and gate-source voltage ratings of the GaN devices should never be exceeded. In almost all cases in power management applications, incidents creating over voltage across the drain-source or gate-source terminals have enough energy to cause a single-event failure in GaN power transistors.

GATE DRIVE DESIGN

Many of the requirements of the proper gate drive circuit for GaN applications have been described in previous chapters, at least indirectly. For completeness, let's mention them again:

- 4.5 V to 6.5 V gate drive amplitude depending on the specific GaN device used
- precisely regulated bias for the driver to prevent over voltage on the gate–source terminals
- fast rise and fall times to quickly pass through the threshold level of the device in order to avoid oscillations

The schematic diagram shown in Figure 6 depicts a typical implementation meeting these requirements.

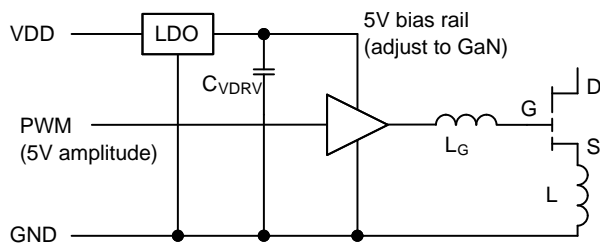


Figure 6. Simplified Driver Schematic

Figure 6 emphasizes the need for a tightly regulated bias regulator which is placed in close proximity to the driver and the power switch being driven by the circuit. The location is important because any distance between the driver, regulator and the power device increases parasitic inductance in the gate drive loop.

The driver itself should take advantage of the low voltage operation and should utilize low-voltage, high-speed transistors. Lower voltage devices have faster speeds and smaller sizes in IC technology which would be extremely beneficial to provide short propagation delays, fast rise and fall times and an economical solution. Many of the repurposed MOSFET drivers used for driving GaN transistors today make use of a larger than necessary die size and are working below their optimized voltage range (10 V to 16 V) introducing extra delays.

The bias regulator – if properly designed – can also act as an over voltage protection clamp to ensure that the bias rail could not be subjected to overvoltage due to external influences, such as absorbing energy coupled into the gate drive circuit during operation. In order to realize this dual functionality, the regulator should not be an ordinary, source only LDO design but rather a source sink regulator. Ideally, the bias regulator would be able to deliver current to the output when needed but it would also be able to act as a clamp and draw current from the bypass capacitor in case of a potential over voltage.

Beyond these requirements, the most important task is to minimize the inductance between the driver output and the gate of the GaN transistor (gate inductance – L_G) and the inductance between the source of the GaN device and the ground connection (source inductance – L_S).

For easier understanding, the effects of these inductances will be analyzed one at a time. Figure 7 shows the simplified equivalent circuit assuming no gate inductance. Further assumptions are ideal voltage sources for the bias rail and for the V_{GS} threshold and a lumped resistor equal to the combined resistance of the output of the driver, the potential external gate resistor and the R_G of the device. The reason we can make these simplifications is because the inductor only influences the operation when the current is changing in the circuit. When the drain current is changing, the gate–source voltage is constant around the threshold voltage level thus the gate current is near zero. The resistive voltage drop across the equivalent gate resistor (R_e) is also near 0 V.

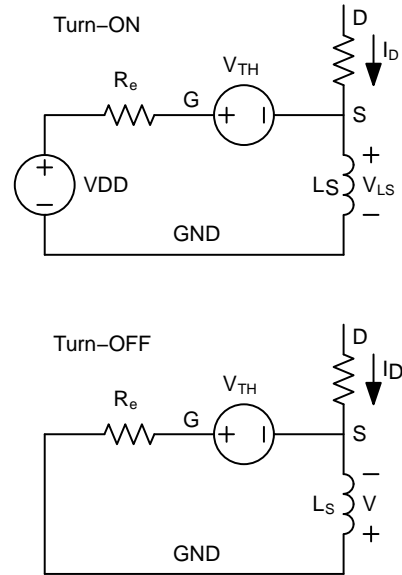


Figure 7. Turn-on turn-off Effect of L_S

Based on the equivalent circuits, we can estimate the maximum voltage across L_S and determine the maximum dI/dt the device can support.

$$dI/dt = \frac{V_{DD} - V_{TH}}{L_S} \quad (\text{eq. 3})$$

and during turn-off:

$$dI/dt = \frac{-V_{TH}}{L_S} \quad (\text{eq. 4})$$

Considering the low gate drive amplitude, only a very limited voltage can be applied across the source inductance. This impacts the ability of the system to quickly ramp the load current, effectively slowing down the switching transitions. The situation is worse during turn-off as the voltage across the source inductance will approximately be limited to the threshold voltage. This phenomenon is well known and similarly present in MOSFET gate drive circuits. The difference is that in the case of the MOSFET gate drive circuits, the gate drive amplitude is significantly higher and the negative feedback of the source inductance is less pronounced.

The gate inductance imposes a different kind of problem which can be explained looking at the equivalent circuit in Figure 8.

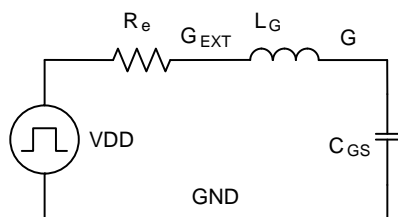


Figure 8. Gate Drive Loop Equivalent Circuit

The gate drive circuit and input terminal of the GaN transistor form a RLC resonant network. The behavior of this circuit greatly depends on the damping. In an extreme case, assuming completely de-energized initial state and $R_e = 0 \Omega$, applying a gate drive signal with the required 5 V amplitude would result in a 10 V peak ($2 \times V_{DRV}$) voltage stress and an undamped oscillatory waveform across the gate source terminals of the device on the die level. This is clearly unacceptable as it could result in the destruction of the transistor.

Fortunately, the output impedance of the driver and the intrinsic internal gate resistance of the device provide ample damping for the resonant network. To achieve optimum performance without ringing, the network should be critically damped ($\zeta = 1$). This condition is satisfied when:

$$R_e = 2 \times \sqrt{\frac{L_G}{C_{GS}}} \quad (\text{eq. 5})$$

Usually, the sum of the resistive impedances in the gate drive loop (R_e) provides a resistance which is larger than the critical resistance defined in Equation 5. The resulting gate drive waveforms for typical component values are shown in Figure 9 where L_G has been varied between zero and 2 nH to generate the group of waveforms.

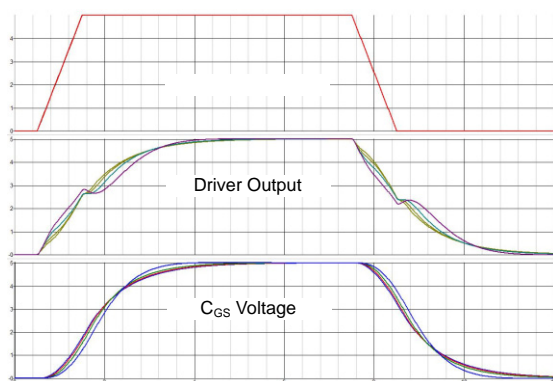


Figure 9. RLC Response to 1 ns Rise and Fall Time Drive Waveform with Typical Component Values ($C_{GS} = 130 \text{ pF}$; $R_e = 6.5 \Omega$; $L_G = 0 \dots 2 \text{ nH}$)

However, it is still practical to keep the gate drive loop inductance at a minimum because increasing L_G dictates a larger R_e to maintain optimum damping. Eventually, the

larger R and L values start to slow down the gate drive and impact the switching performance of the system.

In the end, the only negative effect of a well controlled, moderate value gate inductance is a couple of nano-seconds of additional delay and a minor pulse width distortion which is proportional to the value of the gate inductance. From a driver design point of view, it is important not to waste money using an extremely high peak current driver as the very low output impedance might reduce the damping and cause over voltage at the gate electrode of the GaN device.

For high-side drive applications, the previous considerations remain. The only complication is to provide a floating power source for the driver circuit. This can be accomplished by employing a dedicated floating bias power supply to power the high side driver. In this case the designer's main concern should be to ensure extremely low capacitance between the windings of the bias power supply. Power stages utilizing GaN switches are capable of producing very high dV/dt at the switch node. Since the floating winding of the bias supply is referenced to the switch node, this high dV/dt is directly applied across the two windings of the bias transformer. Capacitive currents in the transformer during switching transitions are proportional to the inter-winding capacitance and it should be reduced as much as possible. This will help to ensure signal integrity and to avoid EMI issues further down the road.

Another popular method to provide power for high-side drivers is the bootstrap technique. For driving MOSFETs, there are plenty of integrated half-bridge drivers where the ground referenced input logic, the level shifter for signal communication to the floating section, the high side driver and sometimes even the bootstrap diode are all integrated monolithically and offered as a complete solution.

For GaN power devices, similar stand alone, integrated half-bridge drivers are not yet available. One significant architectural difference is that for GaN, a local bias regulator must also be included in the floating section of the driver. It is necessary because the voltage built across the bootstrap capacitor varies greatly by operating conditions and diode temperature. Therefore, the accuracy of the floating bias rail could not be guaranteed. For that reason it is desirable to separate the bootstrap and regulation functions as shown in Figure 10.

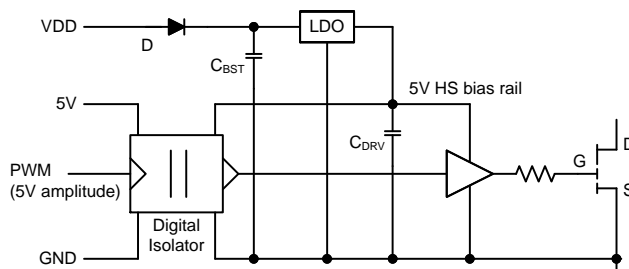


Figure 10. Discrete Bootstrap Drive for High Side GaN Transistor

This solution can be used with GaN devices at lower power levels and at moderate switching frequencies,

typically below 400 W and 500 kHz. The bootstrap diode must be a carefully selected high-speed, low junction capacitance diode, suitable to handle the high dV/dt applied across it during switching.

As a final point, it must be mentioned that for high-power applications above the kW+ range, the designer might have to consider providing a small negative voltage (-2 V) at the gate during the off time. This decision depends on the device and topology selection. In hard-switching converters, this negative bias is avoidable in most cases but in soft switching or resonant converters it is more likely to be necessary to avoid unintentional turn-on when the drain voltage rises. However, applying the negative bias during off time comes with a price. The voltage drop in third quadrant operation will increase. While $V_{GS} = 0$ V will result in approximately -3 V voltage drop across the device in third quadrant operation, negative bias will increase this voltage drop exactly the same amount as the negative bias amplitude (i.e. using $V_{GS} = -2$ V will cause $V_{DS} = -5$ V).

TOPOLOGY CHOICES AND APPLICATION AREAS

Now that the GaN device and its drive requirements are understood, let's turn our attention to find the most suitable topologies and applications for GaN power switches. As mentioned earlier, one of the disadvantages of the GaN technology lies in its limited avalanche capability. It means that voltage stresses beyond the rated voltage of the device should be prevented in all situations – short circuit, input voltage transients, temperature variations, etc. – not just under normal conditions when worst case operating voltage levels and potential switching transient overshoots are more or less predictable.

This is one of the most important but not the only reason that GaN applications favor the fully-clamped half-bridge structure shown in Figure 11.

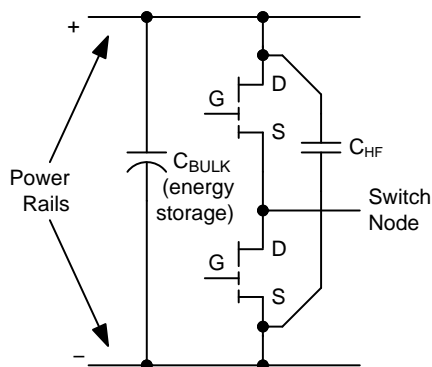


Figure 11. Fully Clamped Half-bridge Structure

This arrangement provides the best protection for the GaN devices against potential over voltage situations. The upper-side transistor provides the clamping function for the low-side transistor. The maximum voltage stress for the low-side transistor is limited to approximately 3 V higher than the voltage present across the large energy storage capacitor (C_{BULK}). This excess voltage is the result of the voltage drop across the source-drain terminals of the upper-side GaN power transistor in third quadrant operation when current is flowing from its source to its drain electrodes with $V_{GS} = 0$ V. Since the clamping device is a GaN transistor, the clamping action is extremely fast. Remember that reverse conduction in a GaN does not utilize a pn junction or a parasitic component; therefore, there is no forward recovery which could delay limiting the voltage across the protected complementary device in the half-bridge topology.

Even more beneficial is the total lack of reverse recovery effect in the GaN transistors when the current is removed from a device conducting in the third quadrant. In MOSFET applications this is called forced commutating the body diode. Operating a power MOSFET this way generates severe losses which eventually could lead to the failure of the device. Fast recovery body diode options have been introduced to power MOSFETs to mitigate this problem but those devices have a slightly higher $R_{DS(ON)}$ for the same die size.

A side benefit of employing two GaN switches in the half-bridge circuit is the automatic reduction of parasitic inductances in the loop where switched currents are flowing. That loop is formed by the two switches and the high frequency bypass capacitor (C_{HF}). The small dimensions and low inductance of the GaN transistor packages help to minimize the loop inductance for best possible switching performance.

Accordingly, the most popular topologies for GaN applications exhibit this half-bridge structure quite prominently. Figures 12 through 17 illustrate a compilation of some of these topologies. The half-bridge structures are highlighted in red color.

Bridgeless Totem-Pole PFC

For power factor correction (PFC) applications, the most popular implementation is the bridgeless totem-pole PFC depicted in Figure 12. One leg (half-bridge) of the input stage operates at line frequency and can be implemented with diodes as shown, or MOSFETs. The other leg runs at higher frequency, determining the converter's operating frequency and the size of the boost inductor. When small size and high efficiency is desired, this half-bridge is often implemented by GaN power switches.

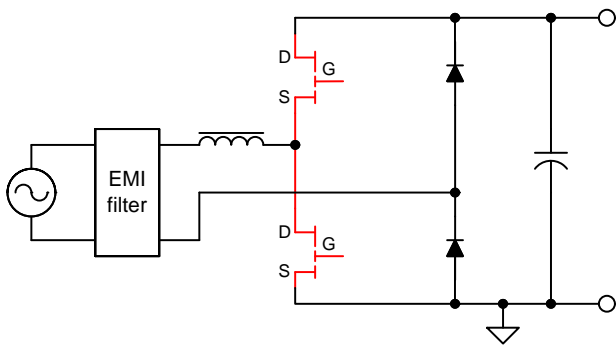


Figure 12. Bridgeless (Totem-pole) Boost PFC Converter

The circuit might be operated in boundary conduction mode with variable frequency. This mode allows a smaller input inductor but operates with higher ripple current for a given output power. With proper control algorithm, the fast leg can achieve zero voltage switching for both GaN devices. The smaller inductor and soft switching operation enables higher frequency operation without increasing the losses of the converter, thus power density can be higher.

When low inductor ripple current is desired, the circuit runs at a fixed frequency and the boost inductor remains in CCM mode for the majority of the line cycle. This mode results in hard-switching, meaning the rectifier switch (in a positive line cycle, the lower switch is the main switch and the upper switch acts as the rectifier) still conducts when the main switch turns-on. This would be very undesirable with MOSFETs as it would cause forced commutation of the body diode. Since GaN transistors do not suffer from stored charge and recovery effects, hard switching is possible even at high switching frequencies.

Dual Active Bridge (DAB) Converter

The next example shown in Figure 13 is a bi-directional converter called dual active bridge (DAB). It uses two full-bridge circuits and it is a prime candidate for high density on-board charger applications with GaN power transistors. Depending on the desired direction of the power flow, either one of the bridge circuits could be the controlled bridge or the rectifier bridge.

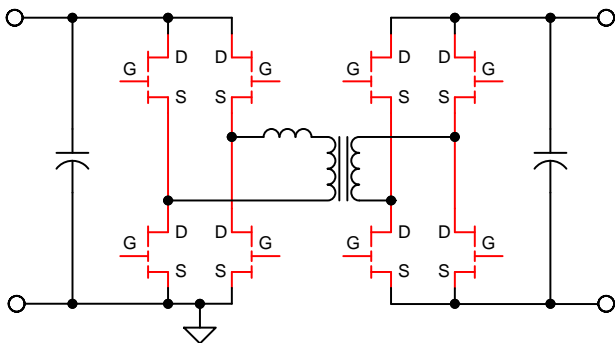


Figure 13. Dual Active Bridge (DAB) Converter

This converter also provides fully clamped operation for all semiconductors. The transformer is relatively simple with only two windings with similar number of turns which can be optimized easier for high frequency operation.

It is not shown in Figure 13, but worth mentioning that GaN based bridge solutions are also very popular in wireless charging applications as those circuits are typically operate in the 6.5 MHz and 13 MHz frequency range. At those frequencies, GaN offers significant efficiency improvements over silicon. In some cases, GaN implementation enables direct drive of the charging coil from high voltage which might eliminate an intermediate conversion stage, boost efficiency and lead to even higher power density.

LLC Resonant Half Bridge Converter

Figure 14 is the well known LLC converter which utilizes a half-bridge structure on the primary side to drive the LLC resonant network. In steady state, normal operation, this converter offers zero voltage switching for the primary side half-bridge and zero current switching for the synchronous rectifiers on the secondary side. Even with silicon MOSFETs, this converter can be operated with high efficiency at moderately high frequencies because of the soft-switching nature of the circuit.

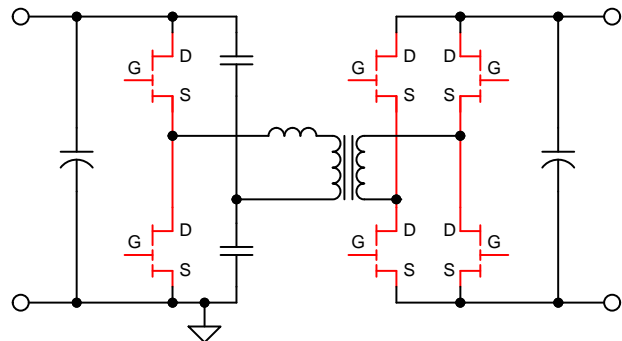


Figure 14. Half-Bridge LLC Resonant Converter

Applying GaN devices on the primary side and complementing them with GaN based synchronous rectifiers on the secondary side can further increase the efficiency and/or the operating frequency to allow further size reduction. Popular application areas for the LLC converter are high density power adapters and low profile power supplies such as the ones used in large TV screens. At higher power level, LLC converters are also favorites for telecom rectifiers and server power solutions.

Active Clamp Flyback Converter

Active clamp converters have been known for a long time but were not widely used because of the added complexity of a second controlled switch and the limited improvements they offered over the simpler, traditional implementations. The active clamp flyback converter in Figure 15 has gained renewed interest since the availability of GaN technology.

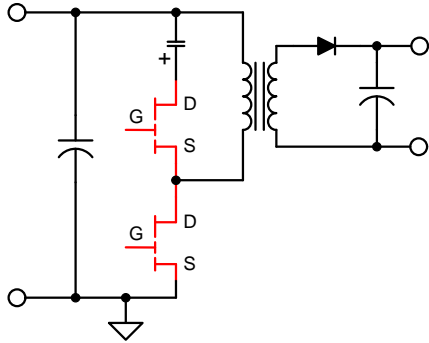


Figure 15. Active Clamp Flyback Converter

The active clamp flyback is ideally suited for a GaN half-bridge structure as both devices will be clamped to the series combination of the input energy storage and clamp capacitor. The low capacitances of the GaN semiconductors make it easier to achieve zero voltage switching for a wider input voltage and load range. With zero voltage switching and a matching GaN based synchronous rectifier, operating frequency can be pushed into the MHz range. The transformer and capacitor sizes can be significantly reduced by such a drastic frequency change, and advanced controllers can take care of light-load efficiency requirements to meet industry standards. The active clamp flyback is now a prime candidate for high power density mobile chargers and small power adapters.

Very High Frequency Resonant Converters

Another area where GaN technology can be considered is resonant power conversion, especially in the 20 MHz – 100 MHz frequency domain. Figure 16 introduces one of the topologies suitable for GaN applications, the Class DE circuit which takes advantage of the extreme speeds offered by GaN. This implementation provides the desired clamping for the GaN half-bridge and ensures that the devices do not see the high voltages sometimes unavoidable in resonant circuits during abnormal operating conditions.

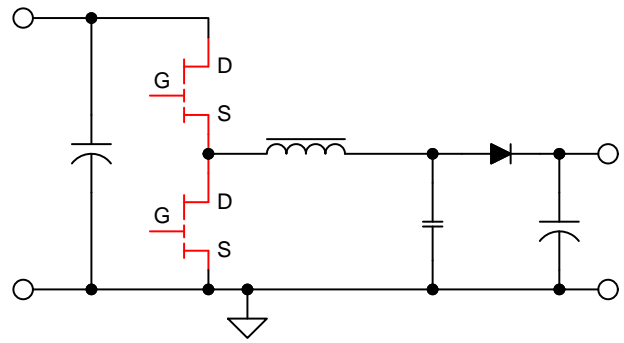


Figure 16. Class DE Resonant Inverter

Although the Class DE inverter shown in Figure 16 is not isolated, the circuit can be built with an isolation transformer allowing it to be used in off-line application. The most popular application area for this solution is high performance lighting applications.

Synchronous Buck Converter

The synchronous buck converter, an eternal favorite is shown in Figure 17. It also provides ideal operating conditions for a GaN half-bridge by placing it parallel with the input energy storage capacitor.

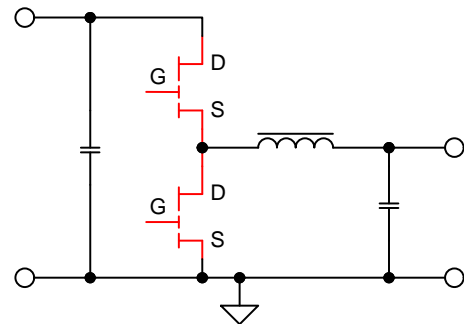


Figure 17. Synchronous Buck Regulator

The best high frequency synchronous buck applications for GaN are the ones where large step down ratio, i.e. very low duty ratio is needed or at high input voltages, from 48 V and above, including off-line solutions.

GaN Power Switches as Synchronous Rectifiers

In Figure 18, synchronous rectifier switches are highlighted in red.

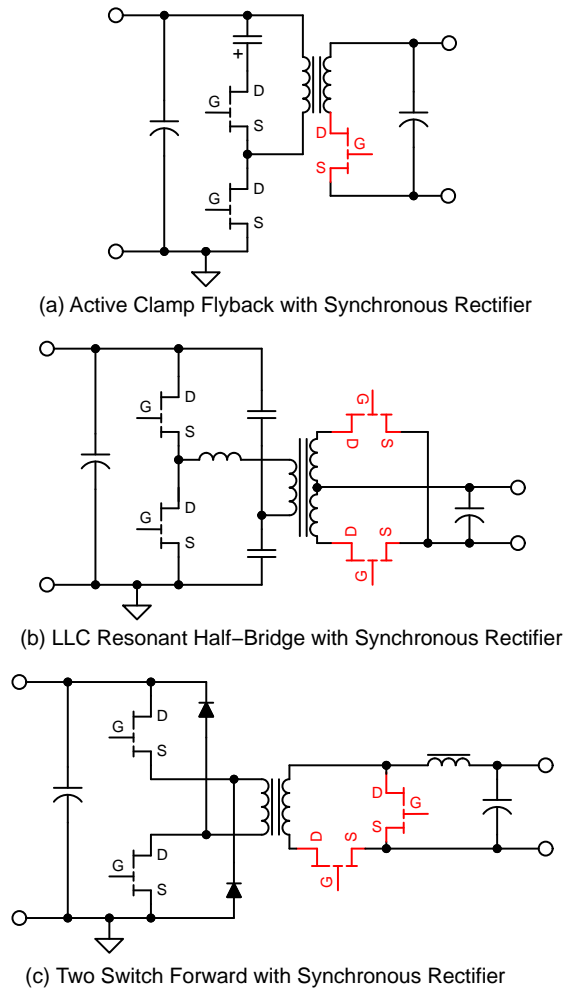


Figure 18. Synchronous Rectification Examples

In many topologies, synchronous rectification is a special case for GaN transistors as it does not conform to the desired fully clamped circuit structures. Nevertheless, GaN switches are popular for synchronous rectification because they offer the shortest turn-on, turn-off delays and allow the best timing accuracies. In many cases the need for speed supersedes the desire to be completely protected against overshoot in the system although the near perfect timing accuracy which can be achieved with GaN switches helps to avoid, or at least reduce, voltage stresses for synchronous rectifiers.

LAYOUT RECOMMENDATIONS

GaN semiconductors are high performance devices that offer the fastest speed and highest efficiency if they are used properly. To realize the full potential of this technology, one must use the best passive components and the best layout design practices. Needless to say that a single layer printed circuit board layout and traditional through hole

components are not capable of supporting low inductance, high speed circuit design techniques. GaN technology requires high performance packaging for the transistors themselves, and those requirements translate directly to the passive components and printed circuit boards accompanying the GaN devices in our designs. In most cases, a four layer, fine pitch PCB will have to be utilized and a few key points need to be addressed during the layout design. With respect to the devices and drivers, the designer must pay attention to:

- the distance between the input capacitors and GaN switches shall be short and direct (try to avoid vias)
- Switch node must be kept small, direct and isolated
- Switch node and PGND act as heatsink for the GaN devices – use lots of thermal vias if other layers are involved in cooling
- control and gate drive signals should be short, direct and equal length; out and return path should overlap and be placed on neighboring layers (minimum distance)

Another critical area is the grounding system and the location and routing of the power planes. Even with four layers at our disposal, the separation of power and signal grounds, identifying and separating high current loops (DC) and switched current loops (AC) can be a difficult task. A few of the key points with respect to power routing are listed below:

- use separate signal and power ground planes and tie them together at a single point only (star connection)
- minimize the power loop whenever possible, use adjacent planes for power and its return path
- provide “tip and barrel” test points for key signals

Figure 19 shows the power plane routing of a high voltage input synchronous buck converter.

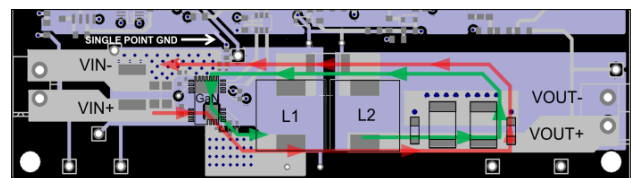


Figure 19. Power Stage Layout Example

This example demonstrates how the current flow is optimized and it is practically flowing in the same locations all the time (green arrow = freewheeling state; red arrow = forward state). The switched current loop of the buck converter is constricted to a tiny area under the GaN power switches and the high frequency bypass capacitors next to them on their left. The result of a well executed, careful design is shown in Figure 20 below. The switching waveforms of this 1.55 MHz, high voltage (off-line), synchronous buck converter are picture perfect.

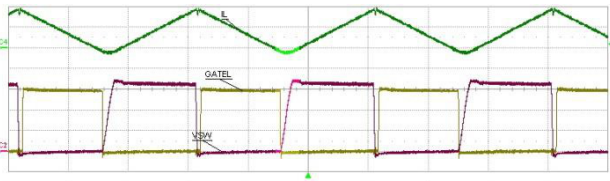


Figure 20. Waveforms of the Example Circuit

Among the waveforms, the most notable is the switch node waveform (VSW – pink trace). Synchronous buck circuits are notorious for all kinds of ringing at the switch node but with the low-inductance packaging of the devices, careful, RF-like PCB design and optimized timing of the gate drives, the ringing has been completely eliminated. Actually, the switch node waveform is so clean that the additional voltage drop across the high-side switch in reverse conduction – before its gate turns on – is clearly recognizable.

CLOSING REMARKS

Power density is emerging as the most important “measuring stick” or figure of merit for today’s power supplies. It encompasses all important performance attributes and it is a good indicator for innovation. Power density implies meaningful economical values as its impact is always measurable in cost savings somewhere along the life of the product.


Power conversion technology is going through an inflection point by the introduction of wide band gap semiconductors. SiC and GaN technologies provide new

ways of architecting power converters and systems. Their impact will be long lasting and revolutionary, similar to how power MOSFETs shaped our industry in the past few decades and IGBTs and bipolar transistors before them.

These technologies are still relatively young, and we must be patient. But it would be a mistake not to pay attention to their persistent march towards becoming a major player in power conversion.

As they become more and more accepted for various applications, power supply manufacturers and their customers can expect a significant progress in power density, with the largest improvement probably coming from GaN based power converters. Welcome to the GaN era!

Laszlo Balogh is a Corporate Fellow, Member of the Technical Staff at ON Semiconductor with more than 30 years of experience in power supply design, power system engineering and power management integrated circuit architecture development. His professional interests include all aspects of switch mode power conversion technology. In recent years, Laszlo focuses on wide band gap semiconductor echo systems and their impact on converter topologies and control algorithms. Laszlo has authored many conference papers and application notes, has numerous granted and pending patents. He is most well known through his contributions to industry leading power supply design seminars since his early days at Unitrode, Texas Instruments, Fairchild and recently at ON Semiconductors.

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