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High-Dynamic Range (HDR) Image Signal Processor (ISP)

AP0102AT M61.00 Firmware Release Notes



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TECHNICAL NOTE

Introduction

This firmware release note summarizes the M61.00 patch configuration set for ON Semiconductor's AP0102AT companion chip and attached AR0142AT Rev1 sensor.

Patch Classification

Patches should be in three categories, Critical, Feature-recommended, and Custom. If a patch is Critical it must be loaded by the customer. If a patch is

feature-recommend, and the customer is using that feature then this patch must be loaded, otherwise it is not required. A custom patch is one that is specific to a customer, and fixes or works-around a customer issue with the usage of the device.

Table 1 summarizes the patches of M61.00 for AP0102AT Rev. 2 silicon. The patches must be loaded before starting streaming in order to operate the sensor properly.

Table 1. M61.00 PATCH CONFIGURATION

Patch ID	Patch Classification	Description
0061	FEATURE-RECOMMENDED	This patch adds support for new sensor models and corrects several issues found with older models. This patch must be loaded before the sensor discovery operation is performed. This includes sensor discovery initiated by host command or by first change-config.
0161	FEATURE-RECOMMENDED	This patch fixes an issue that can cause unstable timing adjustments when keepsync is enabled and the sensor's output pixel clock and the AP0102AT CPIPE clock have different frequencies, including small differences due to clock drift when using different input clocks. This patch is only needed when keepsync is used.
0261	FEATURE-RECOMMENDED	This patch fixes some auto exposure functions when manual or synchronized modes (cam_mode_select = 3) are used or when CAM_AET_DISABLE_FLICKER_AVOIDANCE_AT_TARGET_GAIN is set in CAM_AET_AEMODE
0361	FEATURE-RECOMMENDED	<p>This patch supports a programmable sensor embedded data alignment by adding a variable to configure the embedded data bit shift register. This new variable must be configured to properly transmit embedded data originally received from the sensor.</p> <p>Set RXMGR_EMBEDDED_SHIFT to 20 – sensor_bit_width. For example, for 12 bit parallel and HiSPI input (HDR or SDR mode) set this to 8. For 14 bit HiSPI set this to 6. This patch will initialize this new variable to 8. Changes take effect during change-config.</p> <p>This patch is feature-recommended, only needed when sensor embedded data is enabled.</p>
1161	Critical	This patch fixes an issue where the sensor per channel gain can fall below the specified minimum value. This patch must be applied for correct white balance operation.
1361	FEATURE-RECOMMENDED	This patch allocates a buffer large enough to avoid using memory past the buffer end.
1461	FEATURE-RECOMMENDED	<p>This patch fixes an issue where various overlay operations are not actually performed when a long delay STE transform is active. The overlay operations include enabling overlay layers and updating bitmap properties of active bitmaps.</p> <p>To address the issue of updating bitmap properties of active bitmaps, a new host command, value 0x9001. The command arguments and results status values are identical to the ROM host command, 0x8203 (OVL_SET_BITMAP_PROP). The new host command, 0x9001, does not allow changing a bitmap property of an actively displayed bitmap. This request is rejected with an EBUSY (9) result code. Customers should use the new host command to change overlay bitmap properties to ensure proper operation. The original ROM host command, 0x8203, is retained to allow existing host software to operate.</p> <p>This patch is feature-recommended, only needed when using overlays and STE together.</p>

Table 1. M61.00 PATCH CONFIGURATION

Patch ID	Patch Classification	Description
1561	Custom	<p>This patch checks the line count in the CO_LINE_COUNT register to ensure that the expected number of output lines from the CPIPE block is output for short frame detection usage. If not, then an error is signaled.</p> <p>This error is uniquely signaled by setting the MCU_BOOT_MODE.MCU_INFO_CODE (R0x001C[15:8]) to 0xF6. Also, FW fatal errors are generally indicated by setting bit 0 of the MON_WATCHDOG_STATUS variable, and setting bit 15 of the ERRORS (R0x0060) register. The HW response to the ERROR register bits can be configured by the host in the ERROR_RESET_MASK (R0x0064) and ERROR_STOP_IMAGING_MASK (R0x0066) registers.</p> <p>The FW is halted on FW fatal errors, so host commands will not be processed and the MON_WATCHDOG_COUNT variable will not increment. The AP0102AT must be reset to recover.</p> <p>This patch also fixed an issue when crop and scaler functions erroneously signaled an error.</p>
1761	Custom	<p>This patch adds a new host command, CALIB_STATS_READ_BINS (0x8B02) to read out and return calibration statistics bin data for all 16 bins (8 horizontal and 8 vertical). This is similar to the CALIB_STATS_READ command, which allows reading results of various measurement types, including raw bin data. But CALIB_STATS_READ will only return one bin's data per command, requiring 16 host command transactions to read all bins. This new command only returns raw bin data, and requires only one host command transaction to get all 16 bins.</p> <p>This patch does not add any new variables.</p> <p>This synchronous command retrieves the raw bin accumulator results of a previously-issued CALIB_STATS_CONTROL command with "Capture type" parameter value of 1. Use this command instead of CALIB_STATS_READ to retrieve the complete bin results.</p>
1961	Critical	This patch inserts a delay between starting an OTPM auto-read and polling for its completion. During auto-read host I2C accesses could cause register content corruption
2161	Critical	Bayer images are two pixel too wide or too high when mirrored or flipped, respectively. This patch fixes the sensor configuration to get the correct size image. Note that the sensor field of view is offset by one pixel to the right (mirror) and down (flipped) and is output this way from the AP0102.
2361	Critical	This is the sensor driver patch for AR0143
2461	FEATURE-RECOMMENDED	<p>In network mode, the ISP FW unconditionally disables the output parallel port pads – Dout, FV, LV, and pixclk. Image data is instead routed to pads connected to an Ethernet PHY. However, if the Ethernet GTX clock mode is selected, that clock signal is output on the pixclk pad. During network configuration, a one-time operation, the pixclk pad is enabled if the GTX clock is selected. However, a subsequent change-config will disable the pixclk pad. This patch changes the behavior by not disabling the pixel clock if it's already enabled.</p>

Table 2. M61.00 COMMAND

Patch ID	Value	Mnemonic	Description	Pre/Post Loading
0361	0x0114[11:8]	RXMGR_EMBEDDED_SHIFT	<p>Left-shift bits for embedded lines: value = 20 (output width) – input data width; For example, set to 8 for 12-bit input. D fault is 8.</p> <p>Legal values: [0,15].</p>	Post

Table 3. M61.00 COMMAND


Patch ID	Value	Mnemonic	Description	Pre/Post Loading
1761	0x8B02	CALIB_STATS_READ_BINS	Retrieve all raw bin results	Post

Table 4. M61.00 COMMAND RESULT STATUS

Result Code	Description
ENOERR	Command completed successfully.
ENOENT	There is no result to read because the requested capture data has not been run or is no longer valid.
EBUSY	CALIB_STATS_CONTROL is still running or the system is not in the SYS_STATE_STREAMING state.

Table 5. M61.00 COMMAND RESPONSE PARAMETERS

Byte Offset	Field	Type	Value	Description
+0	Col_0	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 0.
+4	Col_1	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 1.
+8	Col_2	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 2.
+12	Col_3	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 3.
+16	Col_4	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 4.
+20	Col_5	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 5.
+24	Col_6	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 6.
+28	Col_7	UINT32	Luma	This is the sum of the luma values for each pixel in column bin 7.
+32	Row_0	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 0.
+36	Row_1	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 1.
+40	Row_2	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 2.
+44	Row_3	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 3.
+48	Row_4	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 4.
+52	Row_5	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 5.
+56	Row_6	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 6.
+60	Row_7	UINT32	Luma	This is the sum of the luma values for each pixel in row bin 7.

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