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# **Designing LED Drivers for the Challenges of Phase Cut Dimmers**

# Designing LED Drivers for the Challenges of Phase Cut Dimmers

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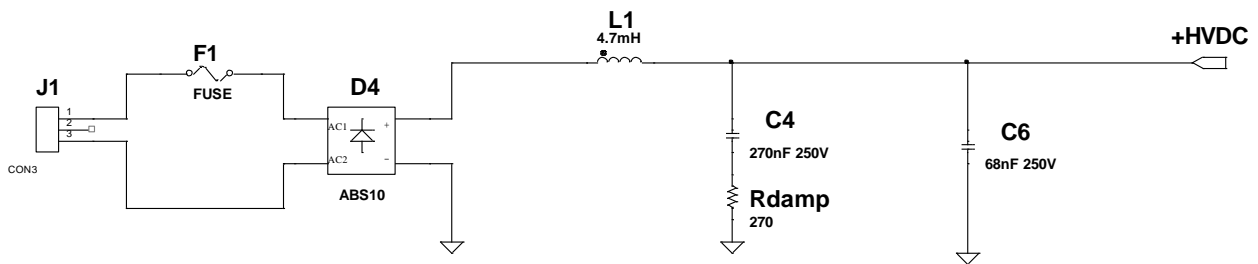
LED replacement bulbs are now firmly entrenched in the mainstay of lighting worldwide. Replacement bulbs are available in all major household fixtures. LED bulb performance has always been excellent from their introduction solving almost all of the CFL bulb issues from slow starting to temperature sensitivity. Except for some specialty bulbs, CFL bulbs are not dimmer compatible. A majority of LED bulbs are dimmer compatible to the extent claimed by the manufacturers. The CEC is moving to make dimmer compatibility a standard feature of LED bulbs for the California market. Dimmer compatibility is the single biggest challenge facing the LED driver designer. Operational requirements with and without a connected dimmer are difficult to meet with a single design approach. Good dimmer compatibility does not lend itself to high power factor and low THD. The optimum design needs multiple personalities depending on the operating state and enough intelligence to recognize the different operating states. Semiconductor manufacturers such as ON Semiconductor® are releasing new LED drivers that ease the challenges of dimmer compatibility.

Such is the case with the ON Semiconductor® NCL30095 and NCL30167. NCL30095 is a fully integrated switcher solution phase-cut dimmable LED driver in a boost configuration. Phase-cut may be either leading edge (typical for most TRIAC based dimmers) or trailing edge (dimmers compatible with electronics transformers). The internal HV MOSFET has a nominal  $R_{ds(on)}$  of  $4.5\Omega$ . The NCL30167 has the same functions as the NCL30095 except that the HV MOSFET is external allowing for higher power applications. The cascoded FET arrangement is one of the unique features of these LED drivers. The output current is regulated for SSL7a compliance. Included functions of the NCL30096/NCL30167 are: closed loop current regulation, thermal foldback, conduction angle sensing, mode changes, and ZCD sensing. The power stage operates in CrM.

This article will cover the following topics:

- Dimmer Compatibility

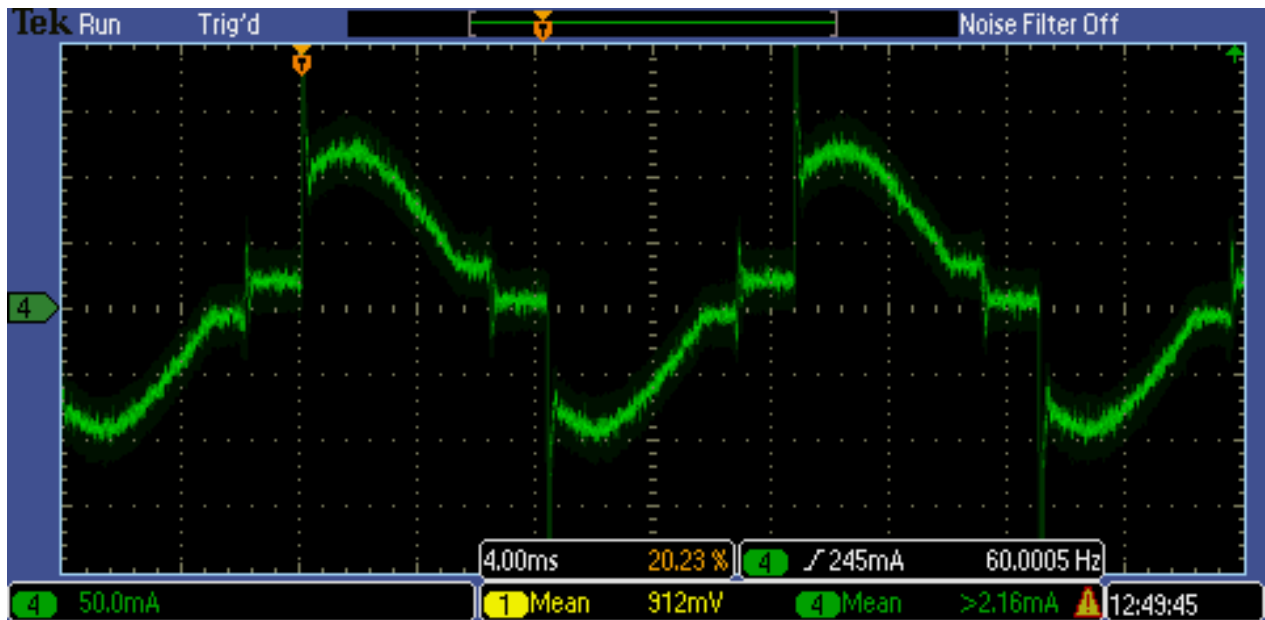
- NCL30095 / NCL30167 Features & Setup
  - Current Set Point and regulation
  - Mode Changes
  - Hold Current
  - Vcc Generation
  - Cascode setup and layout considerations
  - Protection Features
    - OVP
    - OTP



Typical Input Schematic Figure 1.

### Dimmer compatibility

The input filter plays an important role in dimmer compatibility. There are 2 main types of phase control dimmers: leading edge modulated and trailing edge modulated. Here is an example of the line current in a leading edge modulated dimmer:



Line Current for a Leading Edge Dimmer Figure 2.

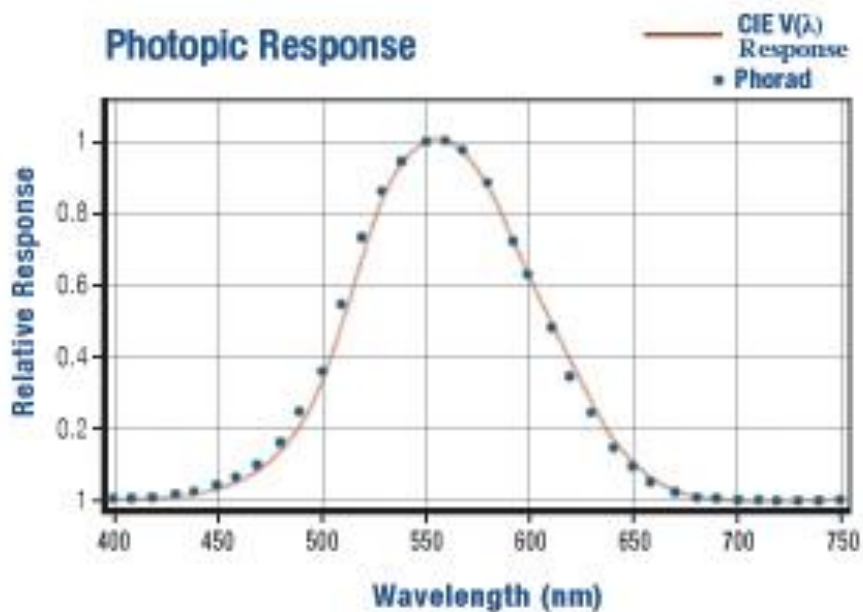
Notice that the line current is delayed from the zero crossing. In this case, dimmer turn on modulates the leading edge of the current to control the bulb. Trailing edge dimmer current turns off partly though the line cycle. Both techniques are equally effective at dimming the bulb. However, the implementation for each technique is quite different. Leading edge dimmers are much more common because their designs are much older and lower cost because the main switch is a TRIAC or SCR. TRIACs and SCRs can only be turned off when the current through the device drops below the holding current. This occurs naturally at the zero crossing after the device has been turned on. Trailing edge dimmers use MOSFETs to control the current. MOSFETs can be turned on or off regardless of the current through the device which makes them able to turn off partly through the line cycle. The MOSFETs and their associated control are more expensive and complicated than the TRIAC/SCR controlled dimmers. Not only have TRIAC/SCR dimmers existed longer than MOSFET dimmers but they are lower cost and still dominated the dimmer market. While this is great for the consumer, TRIAC dimmers present a host of complex issues for the driver designer.

Incandescent bulbs have some non-linearities that make them well suited to TRIAC dimmers. In particular:

1. Positive temperature coefficient
2. Light output that drops off rather sharply with applied voltage.

The positive temperature coefficient comes from the tungsten filament. As the tungsten cools, its resistance goes down. This makes the current almost constant over the dimming range providing hold current for the TRIAC.

Light output from a tungsten filament drops rapidly as the filament cools. Typical filament temperatures are 2,500K which puts them in the warm spectrum of light (more red). As the filament is dimmed, the power in the filament drops but also the color temperature further shifts into the red region. Incandescent bulbs are good examples of nearly perfect black body radiators. The human eye is less sensitive to red light so the luminous output from the filament drops because of lower power and color temperature shift. Light output is measured in lumens which is photopically adjusted for the response of the human eye. The human eye is most sensitive to green light at 560nm.



Human Eye Response Figure 3.

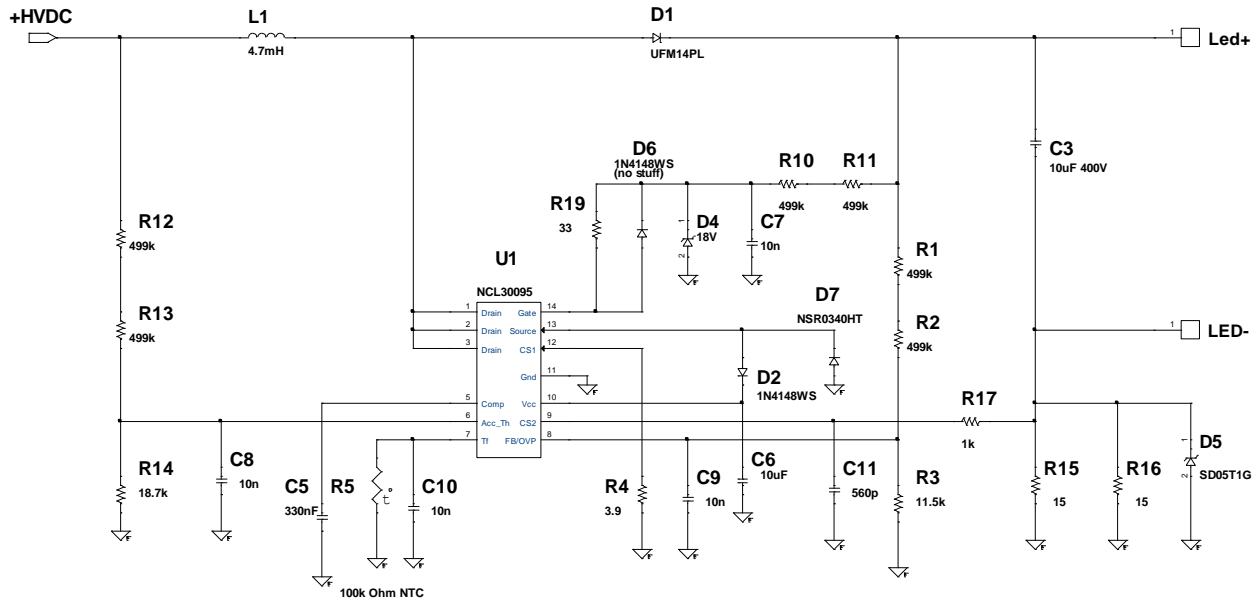
This explanation serves to help understand why TRIAC dimmers are so well suited to work with incandescent bulbs. No light driver (LED or otherwise) behaves like an incandescent bulb. The single biggest challenge for any type of electronic light source driver is maintaining sufficient hold current so that TRIAC does not stop conducting from current starvation. A typical 60W incandescent bulb will produce 800 lumens. An equivalent LED light source consumes only 8W to produce the same light output. Reduced input current is the chief cause of TRIAC dimmer problems. The driver must draw continuous

current of a high enough magnitude over the line cycle to keep the TRIAC conducting. The EMI filter design is a critical part of this.

In figure 1, L1, C4, C6, and Rdamp form the EMI filter of the driver. When the TRIAC begins conducting, it applies a step function of voltage to the EMI filter. The reactive elements of the EMI filter will ring at their natural frequency if not well damped. C4 and Rdamp form the damping network which dampens out ringback current and keeps the TRIAC current above the hold current threshold. The ratio of C4/C6 is critical to maintaining optimum filter damping. This ratio is between 2:1 and 4:1. A ratio below 2:1 is nearly impossible to completely dampen which results in compatibility problems with some dimmers. A ratio greater than 4:1 simply dissipates excessive power. In this architecture, the EMI filter design is agnostic to the driver design. Some designers have resorted to complex dampening circuits that contain active components to reduce dissipation or acoustic noise. If you're willing to bear the cost of the added complexity, there are advantages to be gained.

### **Overview of NCL30095/NCL30167 features**

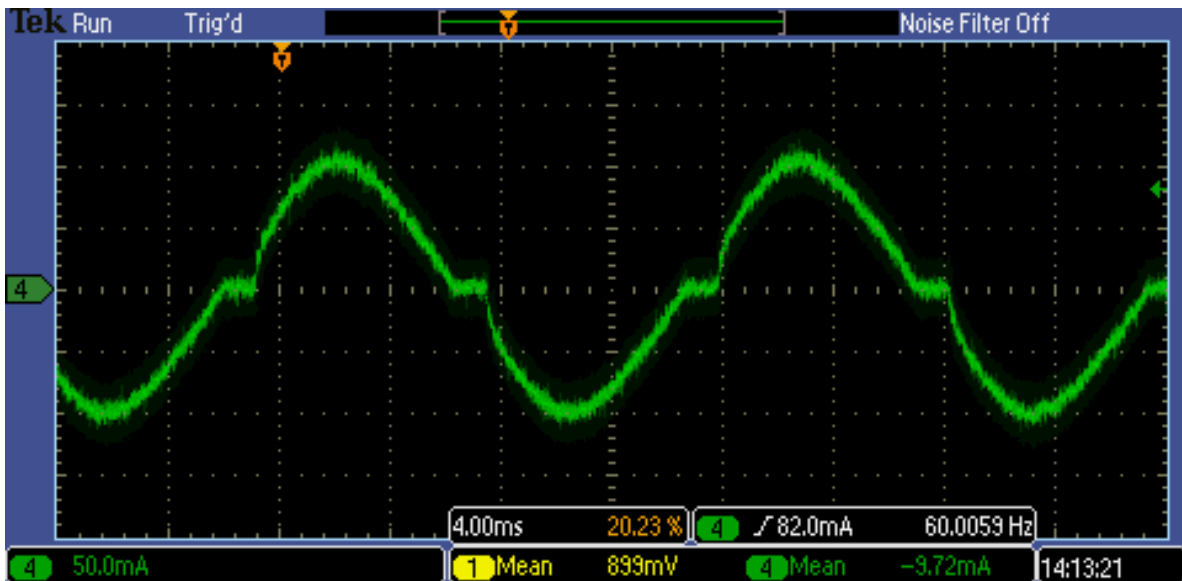
The NCL30095/NCL30167 are constant current output boost regulators. Boost converters make input current control very easy especially in low power CrM designs. Peak current is easily measured and controlled. The instantaneous average current is simply  $\frac{1}{2}$  of the peak current. The output voltage is set by the LED array on the output. The LED voltage must be greater than the peak of the line voltage (as with any boost converter) in order to control the LED current. The NCL30095/NCL300167 have closed loop control of the LED current, overvoltage protection, thermal foldback, and hold current management.



Main Schematic Figure 5.

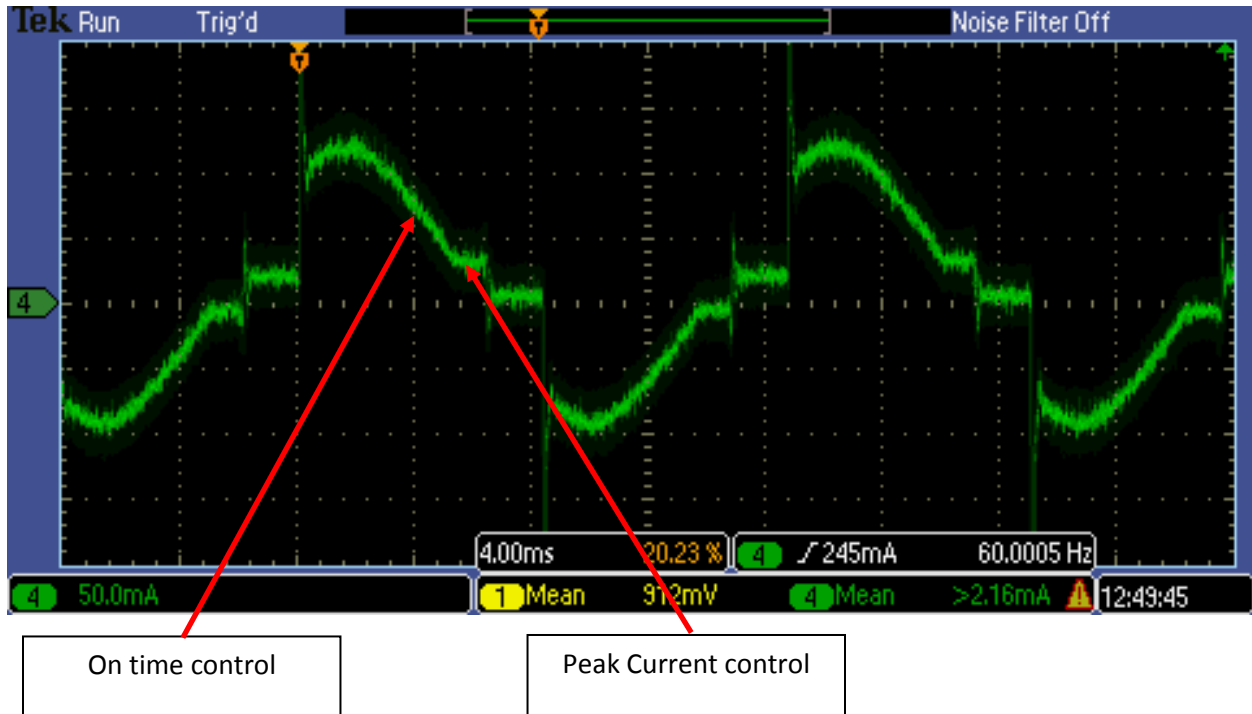
### Mode Changes

NCL30095/NCL30167 operate in different modes depending on the detection of a phase-cut dimmer. The operating mode is on-time control and peak current control. When no dimmer is detected, the control operates in on time control exclusively.



No Dimmer Operation Figure 4.

The power factor is greater than 0.95 and the TDH is less than 20%. No hold current management is invoked because no dimmer is present (or detected). Some distortion is seen at the zero crossings which is typical for CrM based on time controllers. Here the control is in on time control only. Once a dimmer is detected the control is both on time control and peak current control.



Typical Input Current during Dimming Figure 5.

The peak current mode establishes the minimum input current to provide holding current for the TRIAC. In this mode, the controller never allows the peak current to fall below 35% of the maximum peak current set by R4 on CS1. Even at minimum dim level, the minimum peak current is enforced. Decreasing the value of R4 increases the hold current. This also increases the maximum switch current which is  $\frac{1V}{R4}$ . As long as the boost inductor does not saturate, increasing the peak current does not affect regulation because of closed current loop.

### Current Regulation

R15 and R16 set the LED current. The parallel combination of R15 and R16 make up Rsense. The output current is calculated as follows:

$$\text{Led Current} = \frac{0.25V}{R_{\text{sense}}}$$



D5 limits the peak current (by clamping the peak voltage) on R15 and R16 which occurs from inrush current at initial application of input voltage. This is a one-time event since the boost voltage quickly exceeds the peak of the line so no further inrush current is seen. R17 is necessary to limit current in or out of CS2 pin preventing damage to the controller. D5 must have adequate surge capability to handle the inrush current.

## **ZCD**

The current through R15 and R16 is the output current since it's in series with the LEDs. The current in the LEDs is filtered by C3 so the LEDs see mostly a DC current. The current in R15 and R16 is exactly the same as the discharge current from the boost inductor L1. Consequently zero current detection is also done on the CS2 pin. When the decreasing voltage on CS4 reaches 40mV, the controller starts a new switch cycle. Even at 40mV, the current in L1 has not quite reached zero. C11 causes some time delay with R17 to allow for enough time for the current to truly reach zero thus allowing the drain voltage to swing down for ZVS. Some tuning of R17 and C11 will be necessary for each application.

## **Acc\_th**

The Acc\_th pin detects the presence of a dimmer if the sensed conduction angle is less than 160°. The Acc\_th pin has a comparator for sensing the input voltage. The threshold is 400mV rising and 350mV falling. The resistor divider R12, R13, and R14 have an influence on the detection angle because of the comparator threshold on Acc\_th. A lower voltage on Acc\_th makes the controller enter dimmer detection mode earlier which improves dimmer compatibility and accelerates the dim curve wrt phase angle.

The phase angle on the Acc\_th pin is mapped into the output current set point. It is common practice to allow the power stage to operate in open loop control when dimming. However that can lead to irregular output. The reference for the current control loop is established by the phase angle which keeps the LED current always in regulation.

## **OVP**

The voltage divider of R1, R2, and R3 set the over voltage threshold at the OVP pin. The threshold is 3V and it is non-latching.

## Thermal Protection

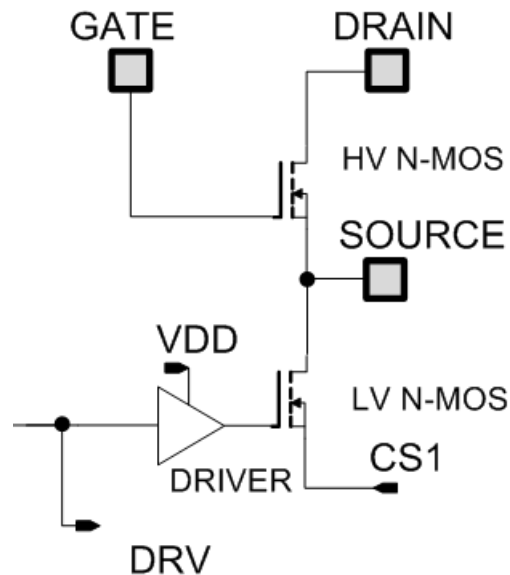
A single NTC (R5) sets the thermal foldback characteristic. Pin 7 sources 85  $\mu$ A and limits the voltage to 3V. As the NTC heats up, the resistance drops as does the voltage on Pin 7. Output current reduction begins when the voltage on pin 7 reaches 1V. Output current drops linearly to 10% when the voltage on pin 7 reaches 0.5V. Below 0.5V on pin 7, the output goes off. A small capacitor on pin 7 is recommended for noise immunity.

## Loop Compensation

The error amp is an OTA so the compensation network connects to the comp pin and ground. A single capacitor is enough for good PF and THD. More complex compensation networks will make small improvements in PF and THD. Compensation works like any PFC converter.

## Power Stage

The power stage uses a cascode arrangement of MOSFETs.



Cascoded MOSFETS Figure 6.

The chief advantage of the cascode is that the HV MOSFET provides  $V_{cc}$  power as a linear regulator. This results in:

1. Fast start up
2. Stable Vcc over the entire dimming range
3. Small Vcc capacitor
4. Single winding boost inductor – no aux winding needed
5. Only one HV MOSFET required

### **Basic Operation**

The gate of the HV MOSFET is held to a fixed voltage. In figure 5, this is done by R10, R11, D4, and C7. Selection of D4 is critical because it sets the startup voltage and limits Vcc in operation. Vcc\_on is 13V maximum and Vcc\_max is 20V. Vth of the HV MOSFET is 2-4V. So an 18V Zener assures that the Vcc at turn on will be 14V. Vcc will not exceed the Zener voltage in operation. The range of Zener voltages that will meet the startup and operating requirements is limited so 18V is a good target value.

The selection value for C7 is rather wide. In general, C7 needs to be large enough to have a low ripple voltage in operation since the gate charges and discharges through C7. Large values of C7 delay the startup. Typical values for C7 are 10nF - 1 $\mu$ F.

### **Clamping the LV MOSFET**

The lower MOSFET will not have a drain voltage greater than Vcc. So the LV MOSFET is much smaller than the HV MOSFET even though both MOSFETs have about the same Rdson. The drain of the LV MOSFET needs to be clamped with a Schottky diode (D7) to prevent conduction of the body diode. Body diode conduction is not ordinarily any concern for MOSFETs in a standalone application. In this case, the LV MOSFET is part of the control circuit die. Body diode conduction will draw substrate current on the die and disrupt control. This is usually noted by an irregularity in the dimming curve. A conventional PN diode will not work because its VI characteristics are similar to the body diode.

### **Vcc Capacitor Size**

The Vcc capacitor is recharged whenever the HV MOSFET switches off. However in deep phase cut dimming, recharge pulses may not occur over a large portion of the half line cycle because there is no

available power from the dimmer. So the Vcc capacitor must hold up Vcc over a full half line cycle. This sets the minimum capacitor size of C6. 4.7 $\mu$ F is the smallest value that will work. 10 $\mu$ F is the recommended minimum value since it provides good design margin and is still available in a SMD package.

### **Layout Considerations and HF Noise Issues**

While cascode drives have significant advantages, there are also challenges related to them. In particular, they are prone to HF oscillations and sensitive to layout. This is caused by the extremely high small signal gain. Oscillations of 200MHz – 400MHz have been seen from the cascode drive. In the best case, the oscillations disrupt operation or show as radiated EMI. In the worst case, the circuit will fail catastrophically. Oscillation is particularly evident at startup. A good scope with high bandwidth is needed to see the oscillation which is most easily seen on the gate pin 14.

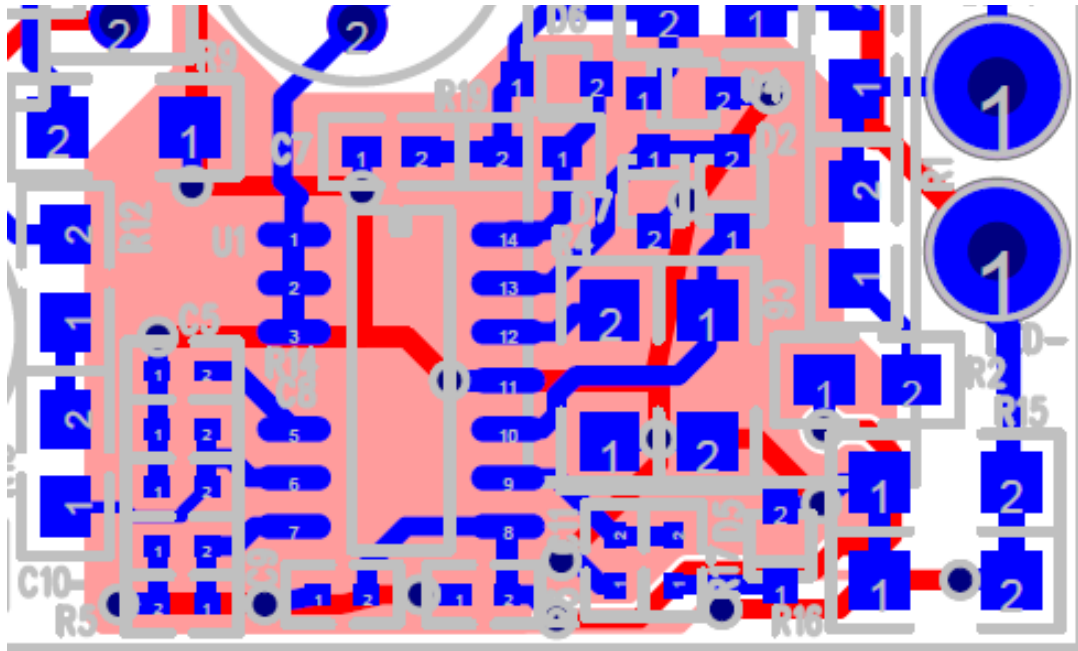
Care should be taken to minimize the trace lengths on the gate (pin 14), Source (pin 13), and CS1 (pin 12). A ground plane under the controller is recommended to minimize impedance back to pin 11 (ground). The gate circuit is especially critical to have a low impedance ground path back to the controller.

Here are some ways to dampen out the oscillations:

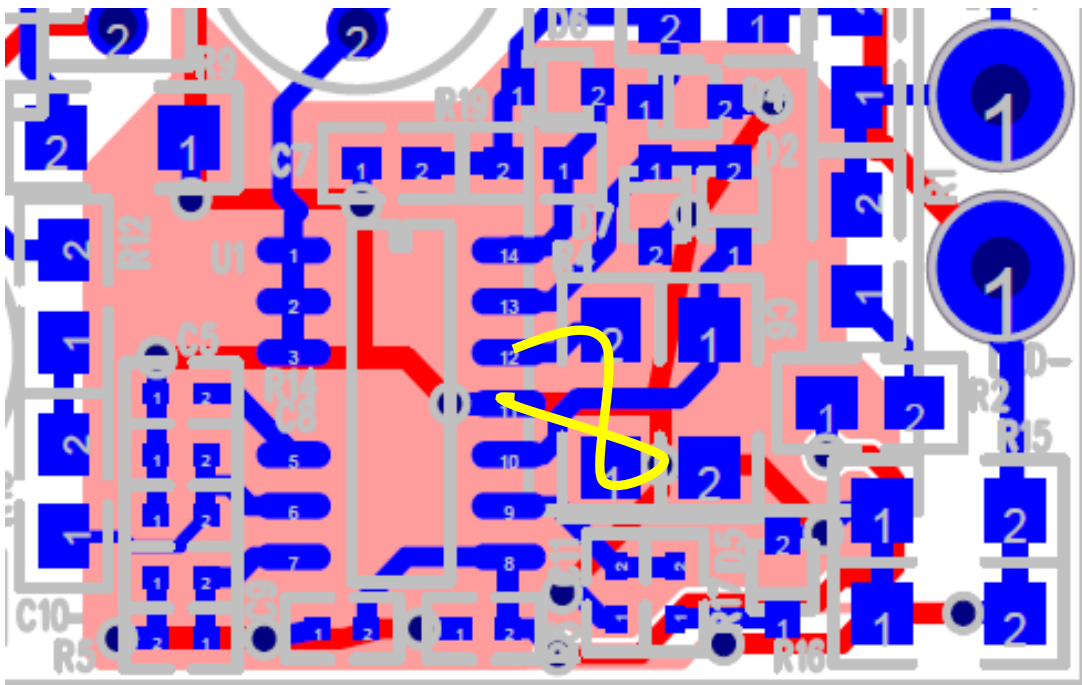
1. Gate resistor (R19) – a speed up diode can be placed in parallel with the resistor to speed turn off
2. Ferrite bead on the gate
3. RC snubber on the source

### **Examples of Good Layout Practice**

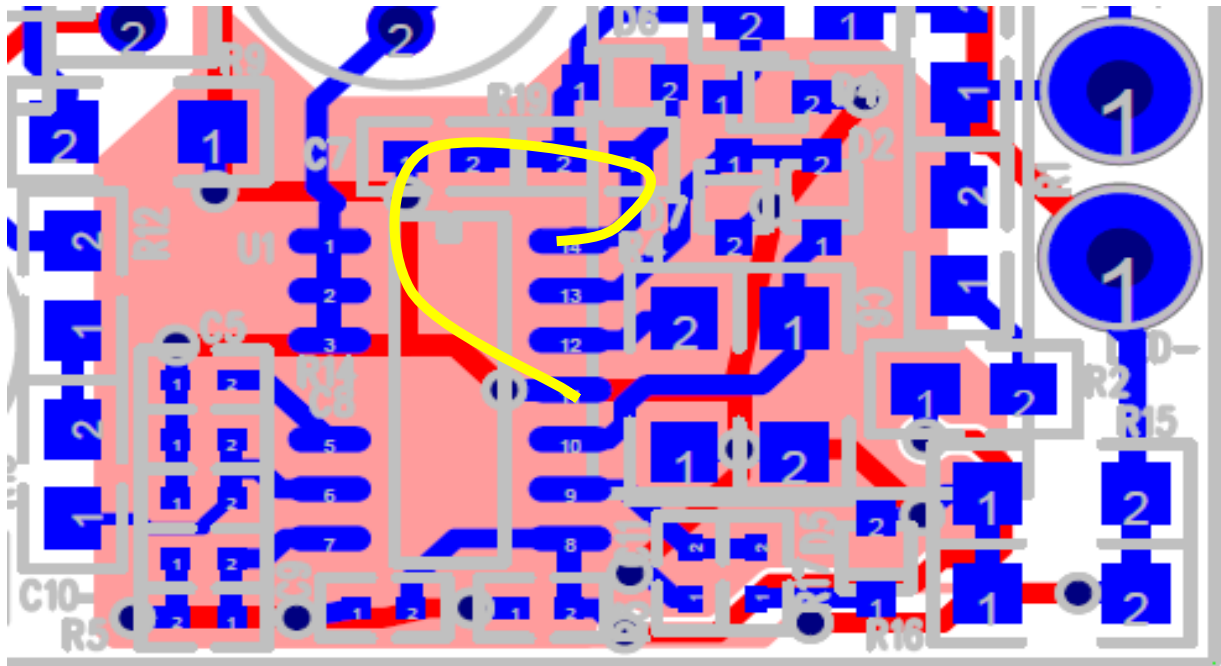
Let's examine some good layout practices for the cascode drives in general and NCL30095 in particular.



One of the first things to notice is the ground plane under the control circuit (colored in pink). The controller ground pin is pin 11. It is immediately connected to the ground plane through a via.



Notice the tight current loop formed by the current sense resistor R4. Pin 11 and Pin 12 are adjacent to make this a naturally tight current loop.




Here the loop for the gate of the HV FET is show in yellow. The gate resistor (R19) is right next to pin 14 which is the gate of the HV FET. The gate capacitor (C7) is directed connector to R19 and the ground plane.

Here are some general layout rules to keep in mind.

1. Placement is critical – high  $dv/dt$  and  $di/dt$  loops need to be kept short. A well placed layout will route easily.
2. Don't cross power and signal grounds – power and signal returns should be connected at one point usually at a sense point or power semiconductor.
3. Keep high voltage away from signal level circuits – high voltage dividers usually have multiple SMD resistors which can be separated if needed.
4. Input signal traces should be kept short to avoid noise sensitivity.

#### Ground Planes

Ground planes can be your best friend or your worst enemy if done wrong. Ground planes make a nice way to connect to a circuit common. Don't use the ground plane for signal and power currents. This definitely cause circuit problems. So pouring a ground plane over the entire board is bad idea for power boards. Its common practice for digital boards but digital boards have much lower currents. Under the control circuit is a good use for the ground plane on a power board. Ground planes makes good layouts better but won't make bad layouts good.

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