Selecting Camera Switches for Next-generation Imaging Applications

Providing high-quality camera and display functionality – increasingly with more than one camera and sometimes with more than one display – is important in applications ranging from surveillance systems and gaming devices, to mobile phones and tablets. And, as users demand higher levels of performance and reliability from ever-more integrated designs, delivering camera-enabled systems presents a growing number of challenges for today’s designers.

Among these challenges are deciding on the most effective methods for routing high volumes of data, protecting and isolating high-frequency signals to ensure data integrity, and maximizing power efficiency. One way to address these challenges is to use analog ‘camera’ switches. By choosing the right combination of switches designers can simplify the handling of multiple camera interfaces, ensure high-integrity data communications, reduce the impact of EMI, protect against ESD, minimize power consumption, and even improve the options for board layout.

Interface Handling

Today’s portable, camera-enabled applications typically integrate an application processor and video/imaging coprocessors, alongside technologies such as baseband processors for handling wireless communications and one or more displays. There are two primary approaches to connecting peripherals such as displays and cameras with application processors or coprocessors: the wide, parallel interfaces favoured by older designs, and the increasingly prevalent serial-oriented interface based on standards developed by the MIPI® (Mobile Industry Processor Interface) Alliance.

Whether based on parallel legacy interconnects or a MIPI standard, integrating multiple cameras and displays can potentially cause problems when it comes to signal integrity. With a parallel interface, the simplest approach is to simply connect the two peripherals to the same set of signals. In the case of a camera, the data flows to the processor, and in the case of a display, it flows from the processor. Such one-way flow can allow the bussed-signal connection to function even without a bus-contention management scheme.

However, two peripherals connected on the same set of conductors causes problems for either the camera or display. There is inherently a different distance between the processor and each of the peripherals resulting in significant potential for signal reflections. One way to improve the parallel interconnect design case is via the use of an analog switch, with a typical design switching the signals that travel the furthest distance.

Newer designs based on MIPI interfaces have a similar problem. While MIPI interconnects do afford a better opportunity to support multiple cameras and displays, they were originally conceived as point-to-point links. As most processors and coprocessors include only a single MIPI port for each peripheral type, multiplexing is essential. And for this, choice of switch is critical.
In Figure 1, for example, the two MIPI camera modules offer four data interfaces and two clock signals. In this case, a triple-pole double-throw (TPDT) device such as the ON Semiconductor FSA642 three-port, high-speed differential switch can fully multiplex access to a peripheral ensuring that only one link is active at any time. The switch accommodates the D-PHY standard, has a typical (~3 dB) bandwidth of 1.0 GHz and, with a quiescent current consumption of less than 1 μA, minimizes power consumption.

Figure 2. Dual High-/Low-resolution Camera

More complex designs may need to accommodate multiple data lanes and/or multiple high-resolution and low-resolution cameras as shown in Figure 2. Here we see connectivity for dual high/low resolution cameras with the FSA641 single-pole double throw (SPDT) 2:1 MIPI switch – which has the same power and bandwidth specifications as the FSA642 – providing the requisite multiplexing.

Figure 3. Dual 4-data Lane Camera/Display

Figure 3 illustrates a 4-data lane camera/display architecture with multiplexing provided by the ON Semiconductor FSA644 1.5 Gbps MIPI D-PHY switch, while Table 1 and Figure 4 summarize the MIPI switch architecture options offered by the highlighted devices.

Table 1. FSA64x SWITCH OPTIONS

<table>
<thead>
<tr>
<th></th>
<th>Rate</th>
<th>2-lane (mm)</th>
<th>4-lane (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSA641</td>
<td>700–800 Mbps</td>
<td>3 × 3</td>
<td>&gt; 18</td>
</tr>
<tr>
<td>FSA642</td>
<td>700–800 Mbps</td>
<td>2.5 × 3.4</td>
<td>&gt; 18</td>
</tr>
<tr>
<td>FSA644</td>
<td>&gt; 1.2 Gbps</td>
<td>2.5 × 3.4</td>
<td>5.76</td>
</tr>
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</table>
Data Integrity – The Need for Isolation

Higher frequencies of modern portable devices such as cell phones means there is a need to manage parasitics for optimal signal integrity. And as cameras within these phones move to higher resolutions, parasitic components can easily deteriorate signals and generate unwanted EMI. That’s where high-speed isolation switches come in.

Take, for example, the FSA1208 low-power, 8-port, high-speed switch illustrated in Figure 5. This part is configured as a single-pole, single-throw switch (SPST) and is designed to isolate the high-speed bus from parasitic components in dual camera applications. With a bandwidth in excess of 400 MHz and high ESD rating of 7.5 kV, the FSA1208 offers an optimal way to isolate capacitance and maintain signal integrity for high-speed data paths.

When isolating the unused parallel interface, the FSA1208 reduces the radiated EMI of the path, improving RF desense. The traditional parallel solution can deteriorate the signal due to the unwanted “stub”, resulting in image degradation of the camera module. Another approach is to use multiple analog switches, which complicates design and adds to the overall bill of material (BOM) costs. In contrast, the FSA1208 offers robust isolation and ease of design at a lower cost.

The FSA1208 features an extremely low on capacitance ($C_{ON}$) of 6 pF. The wide bandwidth (> 400 MHz) contributes to signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference. Furthermore, special circuitry on pins A and B allows the switch to withstand an over-voltage condition. The device is also designed to minimize current...
consumption even when the control voltage applied to the OE pin is lower than the supply voltage (VCC). This feature is especially valuable for mobile applications, such as cell phones, allowing direct interface with the general–purpose I/Os of the baseband processor.

Other applications include port isolation and switching in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

### Design Flexibility

One challenge for designers of small form factor portable, camera–enabled applications is the need to deliver high performance while minimizing component count and board space. By choosing the right analog switch, engineers can address these challenges and improve overall design flexibility in high component density designs.

Take, for example, switches such in the ON Semiconductor µSerDes™ family shown in Table 2.

### Table 2. ON SEMICONDUCTOR µSerDes FAMILY

<table>
<thead>
<tr>
<th>Product</th>
<th>FIN210AC</th>
<th>FIN212AC</th>
<th>FIN224C</th>
<th>FIN224AC</th>
<th>FIN324C</th>
<th>FIN424C</th>
<th>FIN425C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data &amp; Control Bits</td>
<td>10</td>
<td>12</td>
<td>24</td>
<td>22</td>
<td>24</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Max Frequency</td>
<td>48 MHz</td>
<td>40 MHz</td>
<td>20 MHz</td>
<td>26 MHz</td>
<td>15 MHz</td>
<td>10 MHz</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Interface</td>
<td>Micro RGB YUV</td>
<td>Micro RGB YUV</td>
<td>Micro RGB</td>
<td>Micro RGB</td>
<td>Micro RGB SPI</td>
<td>Micro RGB</td>
<td>Micro RGB</td>
</tr>
<tr>
<td>Core Voltage (VDDA/S)</td>
<td>2.8 to 3.6 V</td>
<td>2.8 to 3.6 V</td>
<td>2.5 to 3.3 V</td>
<td>2.5 to 3.3 V</td>
<td>2.5 to 3.0 V</td>
<td>2.5 to 3.0 V</td>
<td>2.5 to 3.0 V</td>
</tr>
<tr>
<td>I/O Voltage (VDDP)</td>
<td>1.65 to 3.6 V</td>
<td>1.65 to 3.6 V</td>
<td>1.65 to 3.6 V</td>
<td>1.65 to 3.6 V</td>
<td>1.6V to 3.0 V</td>
<td>1.6 V to VDDA/S</td>
<td>1.6 V to VDDA/S</td>
</tr>
<tr>
<td>ESD</td>
<td>15 kV</td>
<td>14 kV</td>
<td>15 kV</td>
<td>15 kV</td>
<td>15 kV</td>
<td>15 kV</td>
<td>15 kV</td>
</tr>
</tbody>
</table>

Designed to support high–volume data flows between points such as cameras, displays and controllers, these low–cost, ultra–low EMI devices reduce the number of signals needed across the interface media by converting parallel data paths to serialized differential pairs. As a result, the cost and complexity associated with implementing and managing parallel interface connections is diminished – not least because this approach frees the designer to place the image processor anywhere on the board.

The FIN212AC, which is a member of the µSerDes family, is a low–power serializer/deserializer optimized for use in cell phone displays and camera paths. The device reduces a 12–bit data path to four wires and allows an additional master clock signal to be passed in the opposite direction of data flow. It also provides requisite levels of isolation to ensure data integrity. Based on proprietary, ultra–low–power, low–EMI technology, the switch offers microcontroller, RGB and YUV interfaces and can operate with multiple frequencies up to 40 Hz.
Figure 6 shows two of these devices being used in a mobile phone application. It is worth noting that the μSerDes switches have been designed so that a 180–degree rotation of either device results in a straightforward alignment of the serial clock and data lines. This arrangement, which is shown in Figure 7, is intended to make the layout of the differential trace routes as clean as possible.

**Best Practice Design**

Getting the optimum performance from the chosen analog camera switch technology requires engineers to carefully consider a number of issues. For the MIPI switches described earlier, key considerations will include the specific architecture of implementation, the number of data lanes, the clock rate, switch insertion loss and the scattering (S–Parameter) characteristics of the switch.

In the case of the μSerDes devices, because information is transmitted at a high serial rate, care must be taken when implementing the cabling. In particular, all differential serial wires should be the same length and no noisy signals should be run over or near the wires.

However, the main consideration with differential pairs should be electrical balance. This means that any discontinuity (from vias, pads, stubs, layer transitions or crosstalk) introduced to one side of the differential pair should be introduced equally to the other side. And while differential traces may be tightly or loosely coupled depending on the application, priority should be given to the matching of lengths between the positive and negative pairs over the trace–to–trace configuration.

**Additional Information and Support**

ON Semiconductor can offer engineers a wide variety of information and support for its comprehensive family of camera switch technologies including data sheets, application notes, Spice models and evaluation boards.