TND6050/D

Raising the Efficiency of Power-Factor Correction, from Standby to Full Load

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TECHNICAL NOTE

Digital power-factor control seeks to enhance efficiency by synthesising waveforms according to prevailing load conditions, but the latest linear architectures can offer a simpler solution.

Growing Demand for Power-Factor Correction

Uncorrected reactive power in the power lines of distribution networks and consumer power lines adds undesirable harmonics and reduces efficiency. It can also present a safety risk by allowing excessive currents to flow in ground conductors that are not designed to handle high levels of current.

Given the current focus on reducing carbon emissions and integrating renewable energy sources into electricity generation strategy, there are intense regulatory efforts to improve power quality and energy efficiency of the power distribution network and consumer devices. International standards such as IEC/EN61000−3−2 governing maximum permissible harmonic currents, and Energy Star 80 Plus, effectively require power supplies designed to be connected to the AC mains to implement Power-Factor Correction (PFC). Energy Star 80 Plus recognition, for power supplies achieving efficiency over 80%, stipulates a minimum power factor of 0.9. PFC is also needed to improve the efficiency and harmonic performance of electronic lighting ballasts.

PFC can be implemented with either a passive or an active circuit. While passive circuits contain a combination of reactive components and a rectifier, and operate at the AC line frequency, active power factor correction regulates the input current harmonics using a high-frequency switching converter. High-frequency operation allows the circuit elements to be physically small and lightweight, and helps improve efficiency compared to a passive circuit. With proper control of an active PFC stage, almost any complex load can be made to appear as a linear resistance, which significantly reduces the harmonic current content.

Typical PFC Controller Operation

Generally, active PFC is implemented by inserting a boost (step-up) converter as a pre-converter between the rectifier bridge and bulk capacitor of the power supply, as shown in Figure 1.

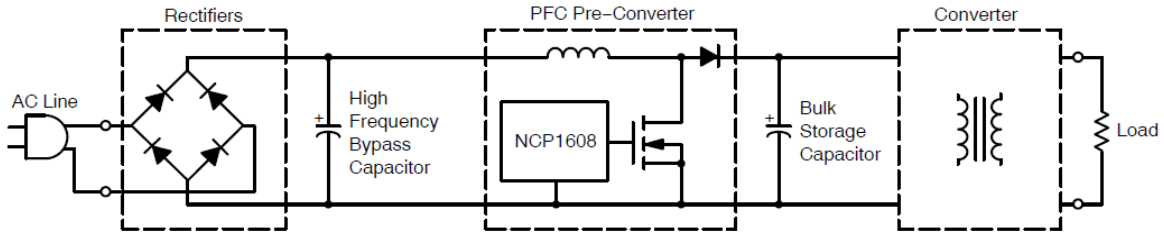

Figure 1. Active PFC Using Boost Pre-converter

For medium-power applications, typically below 350 W, the preferred control method is to operate the boost PFC converter in Critical Conduction Mode (CrM). CrM occurs at the boundary between Discontinuous-Conduction Mode (DCM) and Continuous-Conduction Mode (CCM). In CrM, the driver on time begins when the boost inductor current reaches zero. CrM operation is an ideal choice for medium power PFC boost stages because it combines the reduced peak currents of CCM operation with the zero current switching of DCM operation. The waveforms illustrated in Figure 2 show the boost PFC operating in CrM.

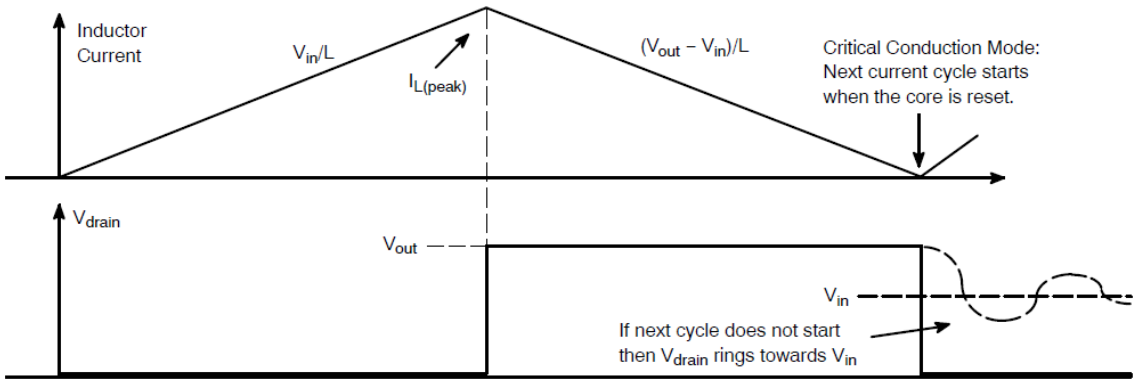

Figure 2. PFC Boost Converter Operating in CrM

High power factor in CrM operation is achieved when the on time of the switch is constant during an AC cycle. The on time is constant, but the off time varies and is dependent on the instantaneous line voltage. The constant on time causes the peak inductor current ($I_{L(peak)}$) to scale with the AC line voltage.

A PFC control IC operating in CrM is able to achieve near-unity power factor, with the aid of additional on-chip circuitry. Although conventional CRM controllers are able to achieve high energy efficiency at nominal load, efficiency is reduced when the power supply is operating at light loads, such as when the appliance is in a standby mode. Another potential drawback is that the controller may enter a burst mode at very light loads, resulting in audible noise.

Digital PFC controllers have been developed, which are able to overcome such limitations and so improve efficiency over the entire load range. This is becoming important as modern ecodesign regulations increasingly call for engineers to pay more careful attention to efficiency at several points across the load range such as 10%, 25%, 50% and 75% of full load.

In a digital PFC controller, sensed analog voltages are converted into the digital domain. Average current-mode control is implemented by calculating the required duty cycle in every switching cycle, based on the sensed values and reference levels, by applying signal processing algorithms. The calculated results are used to generate a pulse-width modulated waveform that operates the boost converter power switch. Vendors of digital PFC controllers claim increased efficiency and high power factor across the full load range, in particular at lighter loads that have challenged linear controllers using traditional CrM.

Increasing Light-Load Efficiency

A new technique implemented in the latest generation of analog controllers enables designers to achieve greater light-load efficiency than traditional CrM controllers, without making the changes in design approach needed to adopt digital PFC. This new operating mode, called Current-Controlled Frequency Foldback (CCFF), is implemented in the ON Semiconductor NCP1611 and NCP1612. These controllers also implement enhanced features that improve fault handling and transient response and provide extra flexibility for designers by supporting different biasing scenarios.

The controller operates at high efficiency, as a conventional analog PFC IC in CrM, under high-current conditions up to the nominal load. At current levels below a programmable threshold, however, the operating frequency is reduced as the controller enters a controlled-frequency discontinuous operation. This happens near the line zero crossing at heavy load and across the entire sine wave at light load. Under such conditions a timer delays the start of the next cycle by inserting dead time until sufficient time has elapsed for a ramp to rise from a sensed voltage representative of the input current up to an internally generated precision 2.5 V “ramp threshold”. This results in longer dead time for a lower input current. Figure 3 shows the voltage across the boost MOSFET under varying load conditions, illustrating the principle of CCFF.

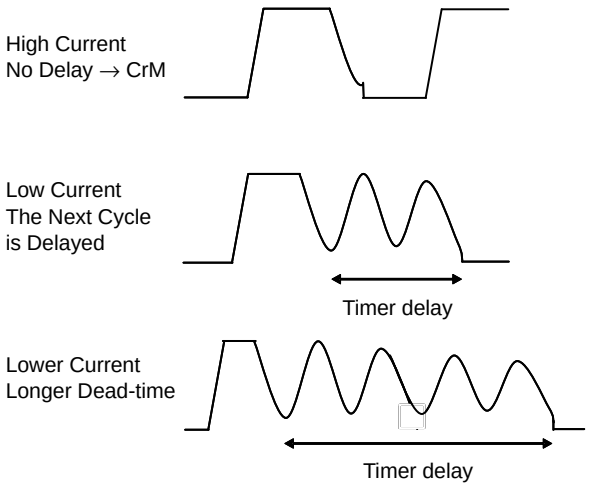

Figure 3. CCFF with Dead Time Controlled by Timer

The timer controls the dead time, rather than the switching period and off time. The frequency is linearly reduced down to a minimum of around 20 kHz when the current is zero. In this way, the controller is able to maximize efficiency at both nominal and light load. In particular, stand-by losses are

reduced to a minimum. A further reduction in losses is achieved by delaying the point at which the MOSFET turns on until the drain-source voltage is at its valley. Valley switching also minimizes generation of electromagnetic interference (EMI). A further advantage is that the system does not stall between valleys. Since the dead time is not affected by variations of the current-cycle duration, valley turn-on happens without hesitation.

An additional advantage of clamping the lower frequency of the CCFF controller above 20 kHz is to keep operation outside the audible frequency range, thereby ensuring quiet operation.

Similar to conventional analog controllers, the NCP1611 and NCP1612 with CCFF integrate circuitry to maintain near-unity power factor even when the switching frequency is reduced. In addition, skipping cycles near the line zero crossing when the current is very low enables the PFC to achieve optimal efficiency at very light loads. This avoids circuit operation when the power transfer is particularly inefficient. Figure 4 compares the efficiency of a PFC controller using CCFF at light loads with that of a conventional CrM controller. Figures 5 and 6 compare power factor and harmonic distortion performance.

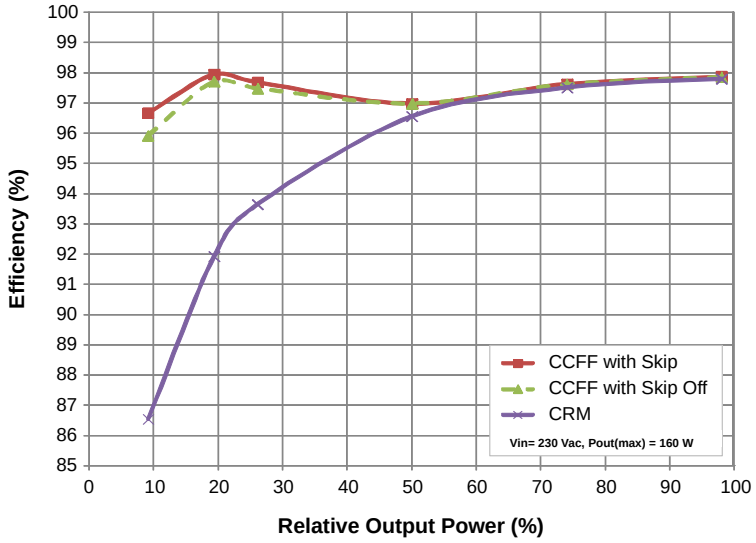

Figure 4. CCFF Eliminates the Loss in Efficiency Seen with Conventional CrM PFC at Light Load

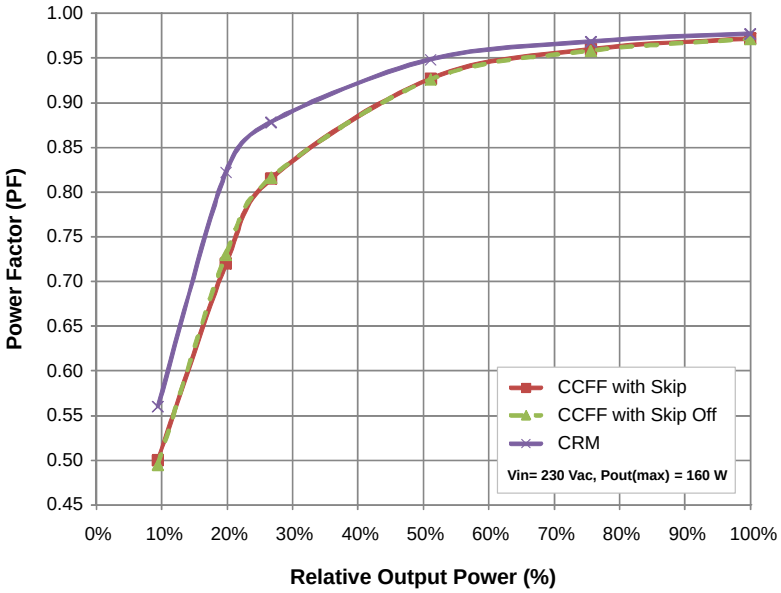

Figure 5. Power Factor over Load Range for CCFF and Conventional CrM PFC

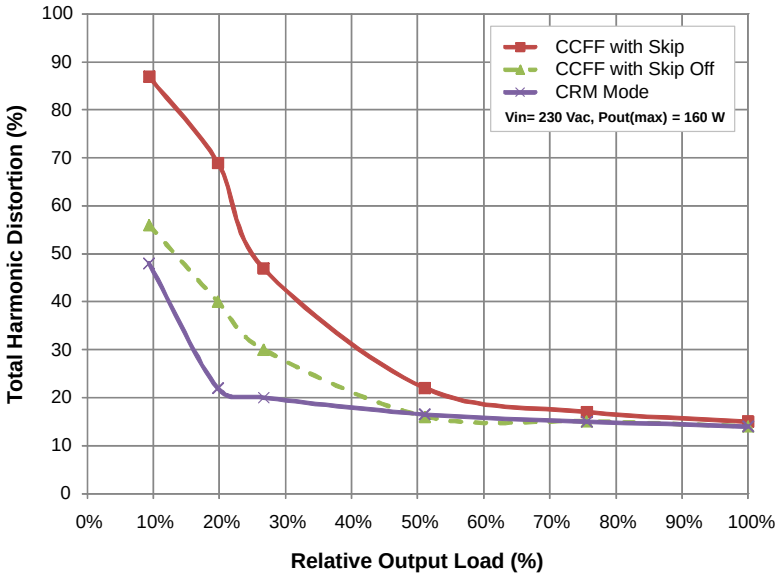

Figure 6. Total Harmonic Distortion for CCFF and CrM PFC

Further Improvements in Analog Controllers

In a conventional PFC control circuit, the typically low bandwidth of the feedback loop can allow voltage overshoot or undershoot in the event of abrupt variations in the load. Digital PFC control, of course, is not subject to such limitation. However, newer analog PFC controllers such as the NCP1611 implement over-voltage protection to prevent excessive overshoot and also integrate an innovative Dynamic Response Enhancement (DRE) function to contain undershoots. This circuitry monitors the voltage at the controller's feedback pin, and effectively provides a temporary increase in loop gain by connecting a 200 μA current source to speed up charging of the compensation network, if the feedback voltage falls below 95.5% of its nominal value. This function is enabled only after the PFC stage has started up to allow normal soft-start operation to occur.

The controller's soft over-voltage protection (soft OVP) function handles overshoots by linearly decaying the power delivery to zero if the output voltage exceeds 105% of its desired level. If the output continues to rise, power delivery is immediately interrupted the when the output voltage reaches 107% of the desired level. Figure 7 shows how these modes work together to regulate the output voltage.

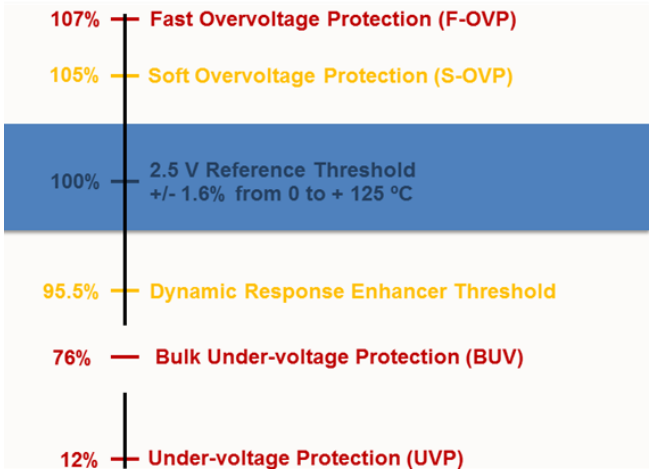

Figure 7. The Controller Implements a Number of Mechanisms to Maintain Load Regulation

Other integrated protection features in the latest-generation analog PFC controllers include two-level current limiting with the ability to turn off the power switch or enter a reduced duty-cycle mode if the bypass or the boost diode is shorted, as well as under-voltage protection, brown-out detection and thermal shutdown. By integrating these essential features on-chip, devices such as the NCP1611 help designers reduce the component count, and

therefore the size and cost, of analog PFC capable of sustaining high energy efficiency and output-voltage regulation across varying load conditions.

Conclusion

Active PFC is becoming necessary across a growing range of applications, as the benefits it provides for the environment, end users and product manufacturers become increasingly attractive. Demands for better performance across the entire load range can be addressed by using digital PFC control ICs. However, designers may prefer to continue using established analog control techniques to meet tight cost and time-to-market constraints. The latest PFC controllers featuring Current-Controlled Frequency Foldback (CCFF) and Dynamic Response Enhancement (DRE) allow designers to continue using proven techniques, benefiting from significant improvements in energy efficiency and regulation from light-load standby operation up to full load.

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