Agenda

- EPA efficiency requirements
- Reference design goals
- Topology selection
- PFC stage design
- LLC stage design
- SR design
- Standby management and handshaking
- Reference design performance
- Conclusions
- Future work
Energy Efficiency: Regulatory Agencies Targets

- **Standby (no load) Power Reduction**
  - ~25% of total energy passing through power supplies is in standby mode\(^{[13]}\)
  - Concerted effort by worldwide regulatory agencies

- **Active Mode Efficiency Improvement**
  - ~75% of total energy passing through power supplies is in active mode\(^{[13]}\)

- **Power Factor Correction (or Harmonic Reduction)**
  - Applicable with IEC61000-3-2\(^{[11]}\) (Europe, Japan)
  - Some efficiency specifications also require >0.9 PF.
  - Example: computers (ENERGY STAR\(^{®}\) rev. 4\(^{[12]}\))
Update on Energy Efficiency Regulations

Computing
• Desktops:
  • ENERGY STAR® 5.0 effective on Jul. 1, 2009
  • 80 PLUS & Climate Savers Computing Initiative
  • Tiered efficiency levels
• Laptops (More information at ENERGY STAR® 2.0 for External Power Supplies)
  • Efficiency: ≥ 87%
  • Standby (no load) power: ≤ 500 mW
  • PF ≥ 0.9

Solid State Lighting Luminaires
• ENERGY STAR® 1.1 effective on Feb. 1, 2009
  • Off-state power: 0
  • Minimum efficacy (Lumen/Watt) requirements by applications (downlights, outdoor lights, etc…)
    • PF ≥ 0.9 for Commercial
    • ≥ 0.7 for Residential
• ENERGY STAR® 1.2 effective in 2H2009
• ENERGY STAR® additional requirements for LED bulbs
  • PF ≥ 0.7
  • High system efficacy → high efficiency power supply

Set-Top Boxes (STB)
• ENERGY STAR® 2.0 effective on Jan 1, 2009
• Europe Code of Conduct version 7 effective Jan 1, 2009
  • Standard is based on maximum allowable TEC (Total Energy Consumption in kWh/year) or allowance
  • Base Allowance depends on the type of STB (Cable, Satellite, etc…)
  • Additional functionalities allowance (DVR, etc…)
  • Annual Energy Allowance (kWh/year) = Base Functionality Allowance + Additional Functionalities Allowance

For exhaustive and up-to-date information on agencies and regulations, check the PSMA energy efficiency data base at: www.psma.com
## Efficiency Targets for Single-output Computing Power Supplies (Servers, Blades, All-in-1)

<table>
<thead>
<tr>
<th>Levels</th>
<th>Specification</th>
<th>20% of rated output power</th>
<th>50% of rated output power</th>
<th>100% of rated output power</th>
<th>Effective Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>80 PLUS Bronze</td>
<td>Single-Output, Non-Redundant, PFC 0.9 at 50%</td>
<td>81%</td>
<td>85%</td>
<td>81%</td>
<td>Start June 2007</td>
</tr>
<tr>
<td>80 PLUS Silver</td>
<td>Single-Output, Non-Redundant, PFC 0.9 at 50%</td>
<td>85%</td>
<td>89%</td>
<td>85%</td>
<td>Start June 2008</td>
</tr>
<tr>
<td>80 PLUS Gold</td>
<td>Single-Output, Non-Redundant, PFC 0.9 at 50%</td>
<td>88%</td>
<td>92%</td>
<td>88%</td>
<td>Start June 2010</td>
</tr>
<tr>
<td>80 PLUS Platinum</td>
<td>Single-Output, Non-Redundant, PFC 0.9 at 50%</td>
<td>90%</td>
<td>94%</td>
<td>91%</td>
<td>Target</td>
</tr>
</tbody>
</table>

**Sources:**
- 80 PLUS®: [http://www.80plus.org/](http://www.80plus.org/)
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Reference Design Goals

- Must meet highest EPA eff. requirements (80+ silver or gold)
- Must fit into All-in-1 PC (Apple iMAC – 0.23 dm^3)
- Input voltage range 90-265 Vac
- Single output – 12 V divided into two terminals:
  => Standby terminal: delivers power all the time
     - 50 mA in off mode
     - 100 mA in sleep mode
     - 5 A maximum in active mode
  => Power terminal: delivers power in active mode (15 A max.)
- Total maximum output power 216 W
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**PFC Stage Selection**

- Input power for this application is > 75 W => need a PFC
- ON Semiconductor offers solutions for three modes:

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Main Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous Conduction Mode (CCM)</td>
<td>Always hard-switching Inductor value is largest Minimized rms current e.g.: NCP1654</td>
</tr>
<tr>
<td>Critical conduction Mode (CrM)</td>
<td>Large rms current Switching frequency is not fixed e.g.: NCP1606</td>
</tr>
<tr>
<td>Frequency Clamped Critical Conduction Mode (FCCrM)</td>
<td>Large rms current Frequency is limited Reduced coil inductance e.g.: NCP1605</td>
</tr>
</tbody>
</table>
PFC Stage Selection - FCCrM

Efficiency of a 300 W, wide mains PFC has been measured:

- Efficiency at 100 Vrms

- NCP1605 (FCCrM)
- NCP1654 (CCM)
- NCP1606 (CrM)

Frequency Clamped CrM seems the most efficient solution while keeping reasonable cost.
PFC Stage Selection – Controller

Some features useful in our application:

- Frequency Clamped Critical Conduction Mode
- Lossless High Voltage Current Source for Startup
- Soft Skip Cycle for Low Power Standby Mode
- Fast Line / Load Transient Compensation
- Signal to Indicate that the PFC is Ready “pfcOK”
- VCC range: from 10 V to 20 V
- Output Under and Overvoltage Protection
- Brown–Out Detection

NCP1605 integrates all needed features for all-in-one power supply and thus reduces overall cost
Power Stage Selection

- Increasing power & Power Density
- Forward
- Flyback
- Half-bridge LLC
- Active clamp forward

ON Semiconductor®
Power Stage Selection – LLC Benefits

- Series type of resonant converter that allows operation over relatively wide input voltage and output load ranges

- Limited number of components: resonant tank can be partially or fully integrated into main transformer

- Zero Voltage Switching (ZVS) condition for the primary switches under all load conditions

- Zero Current Switching (ZCS) for secondary rectifier under all load conditions

- Simple synchronous rectification (SR) implementation

Cost effective, highly efficient and EMI friendly solution
Power Stage Selection – Controller

**NCP1397**

**Features:**
- High-frequency operation from 50 kHz up to 500 kHz
- 600 V high-voltage floating driver
- Adjustable minimum switching frequency (3% accuracy)
- Adjustable deadtime from 100 ns to 2 us
- Startup sequence via an externally adjustable soft-start
- Brown-out protection combined with latch input
- Timer-based auto-recovery and immediate latched OCP
- Disable input for ON/OFF control (skip mode)
- Low startup current of 300 µA
- 1 A / 0.5 A peak current sink / source drive capability
- Common collector or emitter optocoupler connections

**Benefits for all-in-1 application:**
- No driver transformer needed => size restrictions
- Simple skip mode implementation => needed for standby
- Simple OCP implementation => cost impact

**NCP1397 is cost effective and reliable solution for LLC power stage**
Synchronous Rectification can significantly improve efficiency above certain output power.
Power Stage Selection – SR Controller

Some features useful in our application:

- Operates in CCM and DCM Applications
- True Secondary ZCD with Adjustable Threshold
- Automatic Parasitic Inductance Compensation
- 50 ns Turn off Delay from CS to Driver
- Interface to External Signal for CCM Mode
- Trigger Input to enter Standby Mode
- Adjustable Min Ton Independent of Vcc Level
- Adjustable Min Toff Independent of Vcc Level
- 5 A / 2.5 A Peak Current Drive Capability
- Voltage range up to 28 V
- Gate drive clamp of either 12 V or 5 V
- Low startup and standby current consumption
- Maximum Frequency of Operation up to 500 kHz

NCP4303 is high performance driver for any SR system
Secondary SR Turn On/Off

- Usage of SR boosts efficiency above certain power only
- Operation of SR for low output currents is inefficient

SR needs to be turned off based on the output current information
OTP for Secondary Rectifiers

• Max output current is 18 A. In case of fan or secondary rectification system fail serious damage can occur to data or SMPS itself.

SMPS needs to be protected against over temperature and provide a signal to PC for fan speed control and to shut down prior the SMPS would fail.
Standby Management

- According to All-in-1 spec the power terminal has to be turned off during standby mode by an external switch.

NFET provides low $R_{ds\,on}$ compare to PFET.
Complete Block Diagram

- FCCrM maximize eff. of front stage, reduces PFC coil size
- ZVS maximizes efficiency, LLC topology minimizes dimensions
- SR improves eff. under medium and high loads
- Disconnects pwr. output during STBY
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### NCP1605 Design Worksheet

#### NCP1605 Excel Spreadsheet

J. Trench / January 2007

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>350V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>48V</td>
</tr>
<tr>
<td>Input current</td>
<td>40A</td>
</tr>
<tr>
<td>Output current</td>
<td>10A</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>10uF</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>4.7uF</td>
</tr>
<tr>
<td>Maximum input power</td>
<td>250W</td>
</tr>
<tr>
<td>Minimum output power</td>
<td>2W</td>
</tr>
</tbody>
</table>

#### Bulk Capacitor and Coil specification

- **Q bulk** (µF): 180
- **Q inductor**: 200 uH

#### Conduction Losses

- **Input Bridge**: 1.2
- **Device**: 1.25

#### Oscillator Capacitor

- **Capacitor**: 100pF

#### On-time Adjust Circuitry

- **RF1/2**: 6.5

#### Feed-back and OVP arrangements

- **Rfb**: 1kΩ
- **Rovp1**: 1kΩ
- **Comp**: 1kΩ

#### Input Voltage Sensing

- **Rin**: 33Ω
- **Vin**: 15V

#### Current sense Network

- **Rsense**: 1Ω
- **Resense**: 1Ω

#### Generic NCP1605 Application Schematic

- **EMI Filter**: Illustration of EMI filter design

---

200 uH PFC inductor keeps low operating frequency => EMI impact
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Resonant Inductance Location?

**External inductance**
- **Benefits:**
  - Greater design flexibility
  - Lower radiated EMI emission
  - Transformer winding utilization
- **Drawbacks:**
  - Worse windings cooling
  - Primary to secondary insulation is more complex to achieve

**Internal leakage inductance**
- **Benefits:**
  - Primary to secondary insulation is easy to achieve
  - Better cooling for windings
  - One component only
- **Drawbacks:**
  - Less design flexibility
  - EMI radiation
  - Eddy currents in SMPS metal cover due to stray flux
  - Pure winding window utilization

External resonant coil provides more benefits for high power density designs
LLC Resonant Tank Parameters

Selected solution: Standard transformer + external resonant inductance

Transformer: Primary inductance $L_m = 430\, \mu\text{H}$
Leakage inductance $L_{lk} = 55\, \mu\text{H}$
Turn ratio prim. to sec. $n = 17.5$
Turn ratio prim. to aux. $n_{aux} = 11.6$

Resonant coil: $L_s = 30\, \mu\text{H}$

Resonant capacitor: $C_s = 2 \times 12\, \text{nF}$
LLC Resonant Tank Model

- This design uses transformer leakage and external coil as resonant inductance
- T model can be used

\[
k = \sqrt{1 - \frac{L_{lk}}{L_m}}
\]

\[
L_{e1} = L_{e2} = (1 - k) \cdot L_m
\]

\[
L_{me} = k \cdot L_m
\]

T model reflects the fact that Lm also participates on resonance => transformer gain impact
LLC Stage Gain Characteristic

Selected resonant tank provides narrow operating frequency range

- \( f_{op} = 87 \text{ kHz} @ V_{bulk}=350 \text{ Vdc} \)
- \( f_{op} = 103 \text{ kHz} @ V_{bulk}=385 \text{ Vdc} \)
- \( f_{op} = 124 \text{ kHz} @ V_{bulk}=420 \text{ Vdc} \)
NCP1397 simplifies LLC stage design by implementing dual OCP and skip mode
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SR Design

SR MOSFET losses:
- Conduction losses
  \[ P_{cond} = \left( I_{out} \cdot \frac{\pi}{4} \right)^2 \cdot R_{ds\_on} \]
  \[ \Rightarrow \text{Rds\_on selection} \]
- Gate drive losses
  \[ P_{drv} = Q_g \cdot F_{sw} \cdot Vcc \]
  \[ \Rightarrow \text{gate charge selection} \]
- Body diode losses
  \[ P_{body} = \frac{I_{out}}{2} \cdot V_f + \left( I_{out} \cdot \frac{\pi}{4} \right)^2 \cdot R_{dyn} \]
  \[ \Rightarrow \text{Affected by diode Vf, dynamic resistance and parasitic inductance, external Shottky to be used} \]

SR controllers consumption and gate drive losses in standby would hamper standby efficiency
⇒ It is critical to turn off whole SR system in standby mode
SR – Package Parasitic Inductance

- TO220 package is mostly used due to cost and also simple soldering process

- Parasitic inductances $L_{\text{drain}}$ and $L_{\text{source}}$ create voltage drop that is proportional to the secondary current $I_{\text{sec}(t)}$ derivative.
- The $V_{\text{ds}}$ voltage reaches zero level prior secondary current
- SR controller detects zero voltage in the time the secondary current has still significant level => efficiency degradation
- Higher frequency or $dI_{\text{sec}(t)}/dt$ is, higher efficiency drop will be
SR Design – Package Parasitic Inductance

- This issue becomes really serious when very low $R_{ds\_on}$ MOSFET is used.

SR controller with $V_{th\_zcd} = 0$ mV

SR controller with $V_{th\_zcd} = -5$ mV

SR controller with 0 mV ZCD threshold provides longer conduction period for SR MOSFET.
NCP4303 Parasitic Inductance Compensation

$L_{\text{comp}}$ can be done on PCB or using ferrite bead

SR MOSFET conduction period is maximized when NCP4303 implemented with compensation Inductance

Note: Parasitic inductance compensation not used in this PCB version

Note: Patent pending
SR Design – MOSFET Selection

- SR MOSFET works under ZVS conditions
  => Gate charge is given by Ciss capacitance (Cgs+Cgd) and gate voltage

<table>
<thead>
<tr>
<th>MOSFET type</th>
<th>Qg @ 5 V [nC]</th>
<th>Qg @ 12 V [nC]</th>
<th>Rds_on @ 5V [mΩ]</th>
<th>Rds_on @ 12V [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPP015N04N</td>
<td>101</td>
<td>245</td>
<td>1.9</td>
<td>1.2</td>
</tr>
<tr>
<td>FDP047AN</td>
<td>39</td>
<td>96</td>
<td>5.8</td>
<td>4</td>
</tr>
<tr>
<td>IRFB3206</td>
<td>55</td>
<td>133</td>
<td>3.3</td>
<td>2.3</td>
</tr>
</tbody>
</table>
SR Design – Gate Voltage Clamp Selection

NCP4303 with 12 V gate voltage clamp to be used
SR Final Schematic with SR Turn On/Off

- **Schottky** Improves efficiency under light loads
- **NCP4303 with min. ton and min. toff adjust resistors**
- **SR on/off comparator**
- **Secondary current sensing and amplifier**

Simple and cost effective SR implementation

[Image of schematic diagram with annotations]

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OTP

Either PFC or LLC can be latched-off in case of overtemperature
Power Terminal On/Off

N MOSFET provides low $R_{ds_{\text{on}}}$
Primary Biasing

- HV startup is needed for All-in-1 application

NCP1605 simplifies primary biasing
X2 Capacitor Discharge Circuitry

- It is mandatory to discharge X2 cap after application unplugged from mains
- X2 discharge resistor increases standby consumption

Charge pump helps to decrease standby input power by removing X2 cap. discharge resistor
Total Board Schematic

Full All-in-1 solution from ON semiconductor
Reference Design Photo – Top Side

- PFC stage
- Secondary capacitor
- Output connector
- SR MOSFETs and STBY switch on cooler
- EMI filter
- LLC stage
- Resonant inductor
- Transformer
- Output connector
Reference Design Photo – Bottom Side

- NCP1397B LLC cnt.
- NCP1605 PFC cnt.
- NCS1002 regulator
- LM324 amplifier
- 2 x NCP4303 SR cnt.
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SMPS Efficiency Charts

Reference design meets 80+ silver specification
SMPS Efficiency Charts, Comparison With Original Solution Without SR

230 V (ON reference design)
230 V (Original SMPS)
110 V (ON reference design)
110 V (Original SMPS)
Light Load Efficiency

![Graph showing Light Load Efficiency with AC voltage range from 90 to 265 V and consumption range from 0 to 2200 mW, comparing No load and 50 mA load scenarios.]
Detail Losses Distribution

- **Vin=110 Vac**
- **Vin=230 Vac**

<table>
<thead>
<tr>
<th>Component</th>
<th>Pd [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output switch</td>
<td>0.5</td>
</tr>
<tr>
<td>LLC MOSFETs</td>
<td>0.3</td>
</tr>
<tr>
<td>Resonant coil</td>
<td>1.0</td>
</tr>
<tr>
<td>PFC coil</td>
<td>2.5</td>
</tr>
<tr>
<td>Bridge rect.</td>
<td>4.0</td>
</tr>
<tr>
<td>Transformer</td>
<td>5.5</td>
</tr>
<tr>
<td>PFC sw. &amp; diode</td>
<td>6.0</td>
</tr>
<tr>
<td>SR rectifier</td>
<td>7.5</td>
</tr>
</tbody>
</table>
Future Work

• Implement parasitic inductance compensation in SR stage and thus further boost the efficiency.
• Use different SR MOSFET(s) and gate clamp voltage to reduce driving losses.
• Further optimization of the PFC stage efficiency
• Boost efficiency to meet 80+ gold specification 😊
Conclusion

• High efficient 80+ silver reference design from ON Semiconductor is now available!!
• FCCrM PFC stage driven by NCP1605 provides excellent efficiency results and minimizes PFC inductor size. PFC OK signal and skip mode featured in this controller simplifies design of All-in-1 PC SMPS
• LLC power stage driven by NCP1397 provides high efficiency, skip mode capability and cheap OCP implementation
• Synchronous Rectifier driven by NCP4303 maximize the SR MOSFET conduction time – thus maximize efficiency. Voltage clamp on the driver reduces driving losses
• ON Semiconductor provides full support on this reference design and mentioned ICs
For More Information

• View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

• View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies