Compensating a PFC Stage
Agenda

• Introduction

• Deriving a small-signal model
  – General method
  – Practical example: NCP1605-driven PFC stages

• Compensating the loop
  – Type-2 compensation
  – Influence of the line and power level
  – Computing the compensation
  – Practical example

• Conclusion
The load power demand is matched in average only

A low frequency ripple is inherent to the PFC function
PFC Stages are Slow Systems...

- The output ripple must be filtered to avoid current distortion.

- In practice, the loop frequency is selected in the range of 20 Hz, which is very low.

- Even if the bandwidth is low, the loop must be compensated!
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A Simple Representation

• We will consider the PFC stage as a system delivering a power under an input rms voltage and a control signal.

\[ V_{in(rms)} \quad \text{PFC stage} \quad P_{out} \]

\[ V_{\text{control}} \]

• Details of the power processing are ignored:
  • Operation mode (CrM, CCM, Voltage or Current mode…)
  • 100% efficiency, only the average power contribution of the sinusoidal signals is considered.
Let’s represent the PFC stage as a current source delivering the power to the bulk capacitor and the load:

\[ I_D = \frac{P_{\text{in(avg)}}}{V_{\text{out}}} \]

- \( P_{\text{in(avg)}} \) depends on \( V_{\text{control}} \) (always), on \( V_{\text{in(rms)}} \) (in the absence of feedforward) and sometimes on \( V_{\text{out}} \).
- 3 possible sources of perturbations: \( V_{\text{control}} \), \( V_{\text{out}} \) and \( V_{\text{in(rms)}} \).
NCP1605

- Frequency Clamped Critical Conduction Mode (FCCrM)
- Key features for a master PFC:
  - High voltage current source, Soft-Skip™ during standby mode
  - “pfcOK” signal, dynamic response enhancer
  - Bunch of protections for rugged PFC stages
- Markets: high power AC adapters, LCD TVs
NCP1605 – Follower Boost

• Voltage mode operation: the circuit adjusts the power level by modulating the MOSFET conduction time.

• The charge current of the timing capacitor is proportional to the FB square and hence to \((V_{out})^2\):

\[
I_{charge} = I_t \cdot \left( \frac{V_{out}}{V_{out,nom}} \right)^2
\]

where:

- \(V_{out,nom}\) is the \(V_{out}\) regulation voltage
- \(I_t\) is a 370-\(\mu\)A current source

• The on-time is inversely proportional to \((V_{out})^2\) allowing the Follower boost function:

\[
t_{on} = \frac{C_t \cdot V_{ton}}{I_t} \cdot \left( \frac{V_{out,nom}}{V_{out}} \right)^2
\]
NCP1605 - Power Expression

- The control signal is $V_F$ offset down and divided by 3 to form $V_{REGUL}$ used in the PWM section.

- Hence due to the follower boost function, the power is inversely dependent on $(V_{out})^2$:

$$P_{in(avg)} = \frac{C_t \cdot V_{in(rms)}^2}{2 \cdot L \cdot I_t} \cdot \left(\frac{V_{out,nom}}{V_{out}}\right)^2 \cdot \frac{(V_{control} - V_F)}{3}$$
NCP1605 - Large Signal Model

Let’s represent the PFC stage as a current source delivering the power to the bulk capacitor and the load:

\[ I_D = \frac{P_{in(avg)}}{V_{out}} \]

\[ I_D = \left( \frac{C_t \cdot V_{out,nom}^2}{6 \cdot L \cdot I_t} \right) \cdot \left( \frac{V_{in(rms)}^2 \cdot (V_{control} - V_F)}{V_{out}^3} \right) \]

- **Constants**
- **Time varying terms**

3 sources of perturbations: \( V_{CONTROL} \), \( V_{out} \) and \( V_{in(rms)} \).
Small Signal Model

• A large signal model is nonlinear because $I_D$ is formed of the multiplication and division of $V_{control}$, $V_{in,rms}$ and $V_{out}$.

• This model needs to be linearized to assess the AC contribution of each variable.

• The model is perturbed and linearized around a quiescent operating point (DC point).
Considering Variations Around the DC Value…

- Let’s omit the perturbations of the line magnitude (assumed constant)
- Let’s consider small variations around the DC values for \( V_{\text{out}} \) and \( V_{\text{control}} \):

\[
\dot{i}_D = \frac{\partial I_D}{\partial V_{\text{control}}} \cdot \dot{V}_{\text{control}} + \frac{\partial I_D}{\partial V_{\text{out}}} \cdot \dot{V}_{\text{out}}
\]

- We then obtain:
Deriving a Small Signal Model…

- The DC portion can be eliminated
- The partial derivatives are to be computed at the DC point that is for:
  - $V_{\text{control}}$ that is the control signal DC value for the considered working point
  - $V_{\text{out,nom}}$ that is the nominal (DC) output voltage
- Replacing the derivations by their expression, we obtain:

\[
I_1 = \frac{\partial I_D}{\partial V_{\text{out}}} \cdot \hat{V}_{\text{out}} \\
I_2 = \frac{\partial I_D}{\partial V_{\text{control}}} \cdot \hat{V}_{\text{control}}
\]

$I_1$ computed for $V_{\text{control}}$ DC point

$I_2$ computed for $V_{\text{out}}$ DC point that is $V_{\text{out,nom}}$
Contribution of the $V_{out}$ Perturbations

• Depending on the controller scheme

\[ I_D = \frac{P_{in,\text{avg}}}{V_{out}} = \frac{f(V_{in,\text{rms}}, V_{control})}{(V_{out})^{n+1}} \quad \text{where } n = 0, 1 \text{ or } 2 \]

• $n=0$ for NCP1607
• $n=1$ for NCP1654 (predictive CCM PFC for which $P_{in,\text{avg}} \propto \frac{V_{control} \cdot V_{in,\text{rms}}}{V_{out}}$)
• $n=2$ for NCP1605 (follower boost – see slide 10)

• At the DC point

\[ V_{out} = V_{out,\text{nom}} \quad \text{and} \quad \frac{P_{in,\text{avg}}}{(V_{out,\text{nom}})^2} = \frac{1}{R_{LOAD}} \]

• Finally:

\[ I_1 = \frac{\partial I_D}{\partial V_{out}} \cdot \hat{V}_{out} = - \frac{(n+1) \cdot f(V_{in,\text{rms}}, V_{control})}{(V_{out})^{n+2}} \bigg|_{V_{out} = V_{out,\text{nom}}} \cdot \hat{V}_{out} = - \frac{(n+1) \cdot P_{in,\text{avg}}}{(V_{out,\text{nom}})^2} \cdot \hat{V}_{out} = - \frac{(n+1)}{R_{LOAD}} \cdot \hat{V}_{out} \]
• Hence, the small signal model can be simplified as follows:

\[ I_2 = \left( \frac{\partial I_D}{\partial V_{control}} \right) \cdot \hat{V}_{control} \]

\[ \frac{R_{LOAD}}{n + 1} \]

\[ \frac{R_{LOAD}}{n + 2} \]

the model can be further simplified
Finally…

- The small signal model is:

\[ I_2 = \frac{\partial I_D}{\partial V_{\text{control}}} \cdot \hat{V}_{\text{control}} \]

where: \[ I_D = \frac{P_{\text{in,avg}}}{V_{\text{out}}} \]

- The transfer function is:

\[
\frac{\hat{V}_{\text{out}}}{\hat{V}_{\text{control}}} = \frac{R_{\text{LOAD}}}{n+2} \cdot \left( \frac{\partial I_D}{\partial V_{\text{control}}} \right) \cdot \frac{1 + s \cdot r_C \cdot C_{\text{bulk}}}{1 + s \left( \frac{R_{\text{LOAD}} \cdot C_{\text{bulk}}}{n+2} \right)}
\]
NCP1605 Example

• The large signal model instructed that:

\[ I_D = \frac{P_{in(\text{avg})}}{V_{out}} = \left( \frac{C_t \cdot V_{out,\text{nom}}^2}{6 \cdot L \cdot I_t} \right) \cdot \left( \frac{V_{\text{in(rms)}}^2 \cdot (V_{\text{control}} - V_F)}{V_{out}^3} \right) \]

• Hence:

\[ n = 2 \]

\[ \frac{\partial I_D}{\partial V_{\text{control}}} = \frac{C_t \cdot (V_{\text{in(rms)}})^2}{6 \cdot L \cdot I_t \cdot V_{out,\text{nom}}} \]
Finally:

\[ I_2 = \frac{C_t \cdot \left(V_{in\,(rms)}\right)^2}{6 \cdot L \cdot I_t \cdot V_{out,nom}} \cdot \hat{V}_{CONTROL} \]

The transfer function is:

\[
\frac{\hat{V}_{out}}{\hat{V}_{CONTROL}} = \frac{R_{LOAD} \cdot C_t \cdot \left(V_{in\,(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}} \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD} \cdot C_{bulk}}{4}\right)}
\]
Power Stage Characteristic – Bode Plots

Asymptotic representation

Gain (dB)

Phase (°)

Frequency (Hz)

\[ f_p = \frac{2}{\pi \cdot R_{LOAD} \cdot C_{bulk}} \]

\[ f_z = \frac{1}{2\pi \cdot r_C \cdot C_{bulk}} \]
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Compensation Phase Boost

• The zero brought by the bulk capacitor ESR is too high to bring some phase margin. It is ignored.

• The PFC open loop inherently causes a -360° phase shift:
  – Power stage pole ➔ -90°
  – Error amplifier inversion ➔ -180°
  – Compensation origin pole ➔ -90°

• The compensation must then provide some phase boost

• A type-2 compensation is recommended
Type-2 Compensation

- The NCP1605 embeds a transconductance error amplifier (OTA)

  ![Circuit Diagram]

  - No direct influence of the $R_{fbU}$ impedance on the compensation
  - Only the feedback scale factor interferes

  $$f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$
  $$f_{p2} = \frac{1}{2\pi \cdot R_1 \cdot C_2}$$
  $$f_{p1} = \frac{1}{2\pi \cdot R_0 \cdot C_1}$$

  Pole at the origin

  $$R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$$

  - $V_{ref}$ is the reference voltage (generally 2.5 V in ON semi devices)
  - $G_{EA}$ is the OTA (200-μS transconductance gain for NCP1605, NCP1654 and NCP1631)
Type-2 Characteristic - Example

- $f_{p2}$ and $f_{z1}$ set the phase boost magnitude and location (frequency).
- The phase boost peaks at: $f_{pB} = \sqrt{f_{z1} \cdot f_{p2}}$ that is 27 Hz.
- The phase boost is:
  $$\tan^{-1}\left(\frac{f_{PB}}{f_z}\right) - \tan^{-1}\left(\frac{f_{PB}}{f_p}\right)$$
- The origin pole $f_{p1}$ adjusts the gain $G_c$ at the phase boost frequency.

**Graph:**
- Gain (dB) vs. frequency in hertz
- Phase (°) vs. frequency in hertz
- $f_{z1}$: compensation zero (6 Hz)
- $f_{p2}$: high frequency pole (90 Hz)
- $\sqrt{f_{z1} \cdot f_{p2}}$
Phase Boost at the Crossover Frequency

The lower $f_{z1}$ and/or the higher $f_{p2}$, the higher the phase boost (max. value: 90°)

Assuming the PFC power stage pole is well below the crossover frequency ($f_c$), the phase boost equates the phase margin ($\phi_m = \phi_B$)

Target a phase boost between 45° and 75°

$$\phi_B = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right)$$
Gain Considerations

- In the red trace, the distance between the zero and the pole frequencies is increased.
- Both characteristics generate the same attenuation at the crossover frequency.
- The lower the $f_{z1}$ frequency, the lower the gain in the low frequency region.
- The higher $f_{p2}$, the lower the $(2.f_{line})$ ripple rejection.
Type-2 Compensator - Summary

• The zero should not be placed at a too low frequency (not to penalize the low-frequency gain)
• The high frequency pole must be placed at a frequency low enough to attenuate the line ripple
• The phase boost (and phase margin) depends on the zero and high-frequency pole locations
• The origin pole is set to force the open loop gain to zero at the targeted crossover frequency
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Compensating for the Full Range?...

- The static gain depends on the load and if there is no feedforward, on the line magnitude:

\[
G_{\text{static(dB)}} = 20 \cdot \log \left( \frac{R_{\text{LOAD}} \cdot \left( \frac{\partial I_D}{\partial V_{\text{control}}} \right)}{n + 2} \right) = 20 \cdot \log \left( \frac{R_{\text{LOAD}} \cdot C_t \cdot (V_{\text{in(rms)}})^2}{24 \cdot L \cdot I_t \cdot V_{\text{out,nom}}} \right) \quad \text{(NCP1605)}
\]

- The power stage pole varies as a function of the load:

\[
f_{p0} = \frac{n + 2}{2\pi \cdot R_{\text{LOAD}} \cdot C_{\text{bulk}}} = \frac{2}{\pi \cdot R_{\text{LOAD}} \cdot C_{\text{bulk}}} \quad \text{(NCP1605)}
\]

- What is the worst case when closing the loop?
Load Influence on the Open Loop Plots

- Let’s increase $R_{LOAD}$ ($R_{LOAD2} = \alpha \cdot R_{LOAD1}$ with $\alpha > 1$)

Unchanged Gain and Phase at the targeted crossover frequency

$20 \cdot \log(\alpha)$

-20 dB/dec

Static gain

Gain (dB)

$\frac{f_{p0_2}}{\alpha} = \frac{f_{p0_1}}{\alpha}$

$f_c$

$\frac{1}{2\pi \cdot rC \cdot C_{bulk}}$

Asymptotic representation

$f_c$ and $\phi_m$ are not affected!
Line Influence on the Open Loop Plots

- No feedforward (e.g. NCP1607) and \(V_{in(rms)2} = \beta \cdot V_{in(rms)1}\) with \(\beta > 1\)

\[
\begin{align*}
40 \cdot \log(\beta) & \quad \text{Static gain} \\
-20 \text{ dB/dec} & \quad \text{Gain (dB)} \\
-0^\circ, -90^\circ & \quad \text{Phase (°)} \\
\end{align*}
\]

\[
\begin{align*}
f_{p0} &= \frac{n + 2}{2\pi \cdot R_{LOAD} \cdot C_{bulk}} \\
f_c &= \frac{1}{2\pi \cdot r_c \cdot C_{bulk}} \\
\end{align*}
\]

The loop crossover frequency is \(\beta^2\) increased.
Load and Line Considerations

• Compensate at full load
  – Same crossover frequency at lighter loads
  – The zero frequency is set optimally (not at a too low frequency)

• Compensate at high line
  – High line is the worst case as in the absence of feedforward, the static gain is proportional to \( (V_{\text{in(rms)}})^2 \)
  – This leads to:
    \[
    (f_c)_{HL} = \left( \frac{V_{\text{in(rms)}}}{V_{\text{in(rms)}}} \right)_{HL}^2 \cdot (f_c)_{LL}
    \]
    Where HL stands for Highest Line and LL for Lowest Line
  – In universal mains applications, the high-line crossover frequency is 9 times higher than the low-line one:
    \[
    (f_c)_{HL} = \left( \frac{265}{90} \right)^2 \cdot (f_c)_{LL} \approx 9 \cdot (f_c)_{LL}
    \]
Crossover Frequency Selection

• In the absence of feedforward, \((f_c)_{HL} \leq f_{line}\) is a good option

• With feedforward, \((f_c)_{HL} \leq \frac{f_{line}}{2}\) is rather selected for a better attenuation of the low frequency ripple

• Get sure that on the line range, the PFC boost pole remains lower than the crossover frequency at full load!

\[ f_{p0} \leq (f_c)_{LL} \]

• If not, increase \(C_{bulk}\)
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Compensation Techniques

• Several techniques exist:
  ▪ manual placement, “k factor” (Venable)…
    + Systematic
    - The PFC boost gain is to be computed at $f_c$
    - No flexibility in the zero and high pole locations $f_c = k \cdot f_{z1} = \frac{f_{p2}}{k}$
  ▪ Pole and zero cancellation:
    ✓ Place the compensation zero so that it cancels the power stage pole:
    ✓ Force the pole at the origin to cancel the PFC boost gain when $(f = f_c)$
    ✓ Adjust the phase margin with the high frequency pole
Pole and Zero Cancellation...

- The higher $f_{p2}$, the larger the phase margin.
- The lower $f_{p2}$, the better the rejection of the low frequency ripple.
- $\phi_m = 45^\circ$ if $f_{p2} = f_c$.
Poles and Zero Placement

- Design the compensation for full load, high line: 
  \[ R_{LOAD} = R_{LOAD(\text{min})} \]

- Place the origin pole to cancel \( K_0 \), the static gain at \( f_c \):
  \[ f_{p0} = \frac{f_c}{K_0} \quad \text{for} \quad R_{LOAD} = R_{LOAD(\text{min})} \]
  \[ \text{where: } \frac{\hat{V}_{out}}{V_{\text{CONTROL}}} = K_0 \cdot \frac{1 + s \cdot r_C \cdot C_{\text{bulk}}}{1 + s \cdot \left( \frac{R_{LOAD(\text{min})} \cdot C_{\text{bulk}}}{n + 2} \right)} \]

- Place the zero so that it cancels the PFC boost pole
  \[ (f_{z1} = f_{p0}) \quad \text{for} \quad R_{LOAD} = R_{LOAD(\text{min})} \]

- Place \( f_{p2} \) to obtain the targeted phase margin:
  \[ f_{p2} = \frac{f_c}{\tan(90^\circ - \phi_m)} \]
Example

- A wide mains, 150-W application driven by the NCP1605
- $V_{out,nom} = 390 \text{ V}$
- $(V_{in(rms)})_{LL} = 90 \text{ V}$
- $(V_{in(rms)})_{HL} = 265 \text{ V}$
- $L = 150 \mu\text{H}$
- $C_t = 4.7 \text{ nF}$
- $C_{bulk} = 100 \mu\text{F}$
- $r_C = 500 \text{ m}\Omega \text{ (ESR)}$
- $f_c = 50 \text{ Hz}$

and $\Phi_m = 60^\circ$

@ high line (265 V)

\[
\frac{n}{V_{out,nom}} = K_0 \cdot \frac{1+ s \cdot r_C \cdot C_{bulk}}{1+ s \cdot \left( \frac{R_{LOAD} \cdot C_{bulk}}{4} \right)} \quad \text{where: } K_0 = \frac{R_{LOAD} \cdot C_t \cdot (V_{in(rms)})^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}
\]

\[
R_{LOAD(min)} = \frac{(V_{out,nom})^2}{(P_{out})_{max}} = \frac{390^2}{150} = 1 \text{ k}\Omega
\]

\[
R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}} = \frac{390}{2.5 \cdot 200 \cdot 10^{-6}} = 780 \text{ k}\Omega \quad \text{(OTA)}
\]

\[
C_1 = \frac{K_{0(min)} \cdot C_t \cdot (V_{in(rms)})^2_{HL}}{2 \pi \cdot f_c \cdot R_0} = \frac{10^3 \cdot 4.7 \cdot 10^{-9} \cdot 265^2}{2 \pi \cdot 50 \cdot 780 \cdot 24 \cdot 150 \cdot 370 \cdot 390} \approx 2.59 \mu\text{F} \quad \Rightarrow \quad 2.2 \mu\text{F}
\]

\[
R_1 = \frac{R_{LOAD(min)} \cdot C_{bulk}}{(n+2) \cdot C_1} = \frac{10^3 \cdot 100 \cdot 10^{-6}}{(2+2) \cdot 2.2 \cdot 10^{-6}} \approx 11.36 \text{ k}\Omega \quad \Rightarrow \quad 12 \text{ k}\Omega
\]

\[
C_2 = \frac{\tan (90^\circ - \phi_m)}{2 \pi \cdot f_c \cdot R_1} = \frac{\tan (90^\circ - 60^\circ)}{2 \pi \cdot 50 \cdot 12 \cdot 10^3} \approx 153 \text{ nF} \quad \Rightarrow \quad 150 \text{ nF}
\]

\[
f_{p1} = \frac{1}{2 \pi \cdot R_0 \cdot C_1} = 93 \text{ mHz} \quad f_{z1} = \frac{1}{2 \pi \cdot R_1 \cdot C_1} = 6 \text{ Hz} \quad f_{z1} = \frac{1}{2 \pi \cdot R_1 \cdot C_2} = 88 \text{ Hz}
\]
Simulation Validation

• The simulation circuit is based on the large signal model:

  Large signal model of the NCP1605-driven PFC stage

  Generation and injection of the ac perturbation

  Feedback and regulation circuit (including type-2 compensation)
Open Loop Characteristic – Full Load

Vin(rms) = 90 V

Vin(rms) = 265 V

fc = 52 Hz @ Vin(rms) = 265 V
fc = 7 Hz @ Vin(rms) = 90 V

ϕm = 87°
ϕm = 62°
Open Loop Characteristic – Mid Load

Gain (dB)

Phase (°)

Vin(rms) = 90 V

Vin(rms) = 265 V

fc = 52 Hz @ Vin(rms) = 265 V

fc = 8 Hz @ Vin(rms) = 90 V

φm = 69°

φm = 58°
Experimental Results at Full Load

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings between 6.3 A and 7.7 A (+/-10%) with a 2 A/µs slope
- The high-line, larger bandwidth reduces the $V_{\text{bulk}}$ deviations and speeds-up the output voltage recovery
Experimental Results at Medium Load

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings between 3.1 A and 3.9 A (+/-10%) with a 2 A/µs slope

- The circuit still exhibits a first order response
Abrupt Load Changes

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings from 7.0 A to 3.5 A (2 A/µs slope)

The dynamic response enhancer speeds-up the loop reaction in case of a large undershoot. Implemented in NCP1605 (FCCrM), NCP1654 (CCM) and NCP1631 (Interleaved)

- The dynamic response enhancer reduces the undershoot at low line
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• General considerations were illustrated by the case of NCP1605-driven PFC stages
• A small signal model of PFC boosts can be easily derived
• The proposed method is independent of the operating mode
• A type-2 compensation is recommended
• If no feed-forward is implemented, the loop bandwidth and phase margin vary as a function of the line magnitude
• The crossover frequency does not vary as a function of the load
• A resistive load can be used for the computation even if the PFC stage feeds a power supply (negative impedance) – See back-up
For More Information

- View the extensive portfolio of power management products from ON Semiconductor at [www.onsemi.com](http://www.onsemi.com)

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at [www.onsemi.com/powersupplies](http://www.onsemi.com/powersupplies)