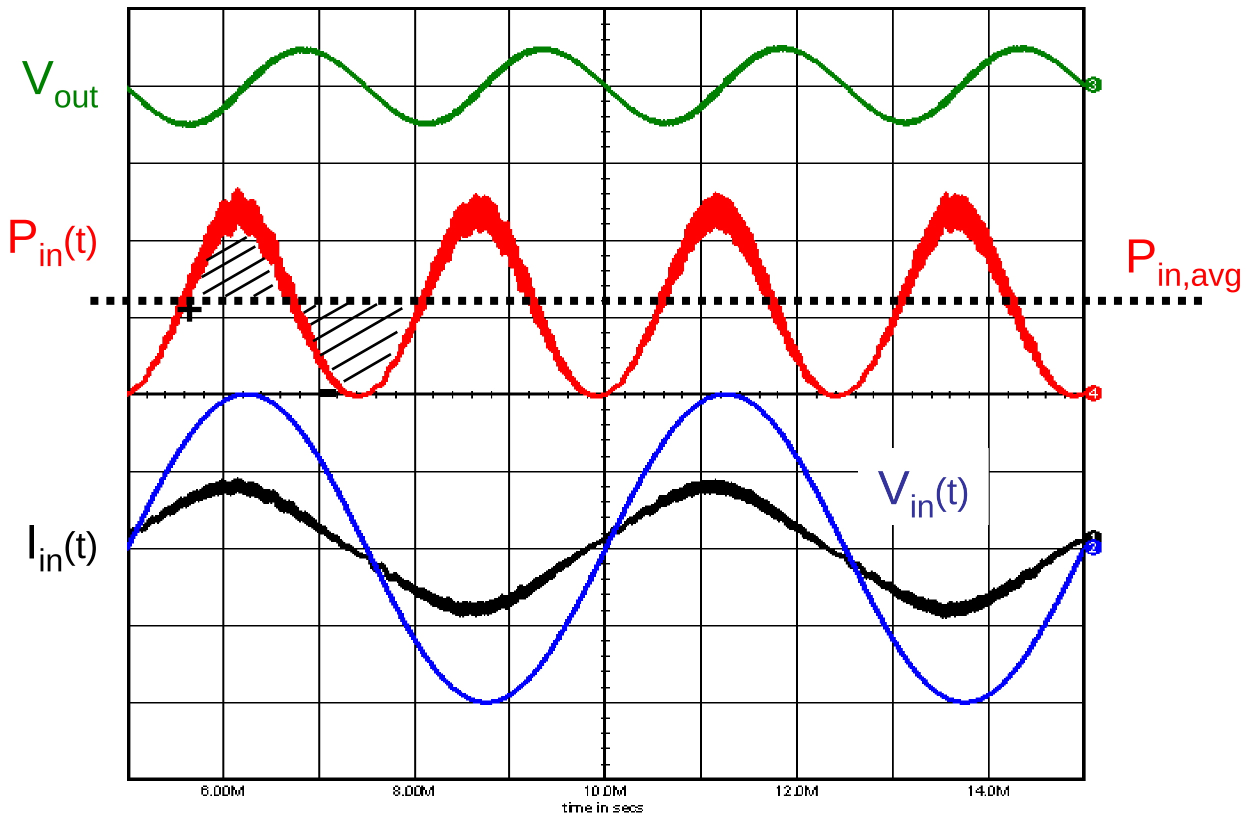
ON Semiconductor®

Compensating a PFC Stage

Agenda

- Introduction
- Deriving a small-signal model
  - General method
  - Practical example: NCP1605-driven PFC stages
- Compensating the loop
  - Type-2 compensation
  - Influence of the line and power level
  - Computing the compensation
  - Practical example
- Conclusion

Output Voltage Low Frequency Ripple



- ❑ The load power demand is matched in average only
- ❑ A **low frequency ripple** is inherent to the PFC function

PFC Stages are Slow Systems…

- ❑ The output ripple must be filtered to avoid current distortion.

- ❑ In practice, the loop frequency is selected in the range of 20 Hz, which is very low.

- ❑ Even if the bandwidth is low, the loop must be compensated!

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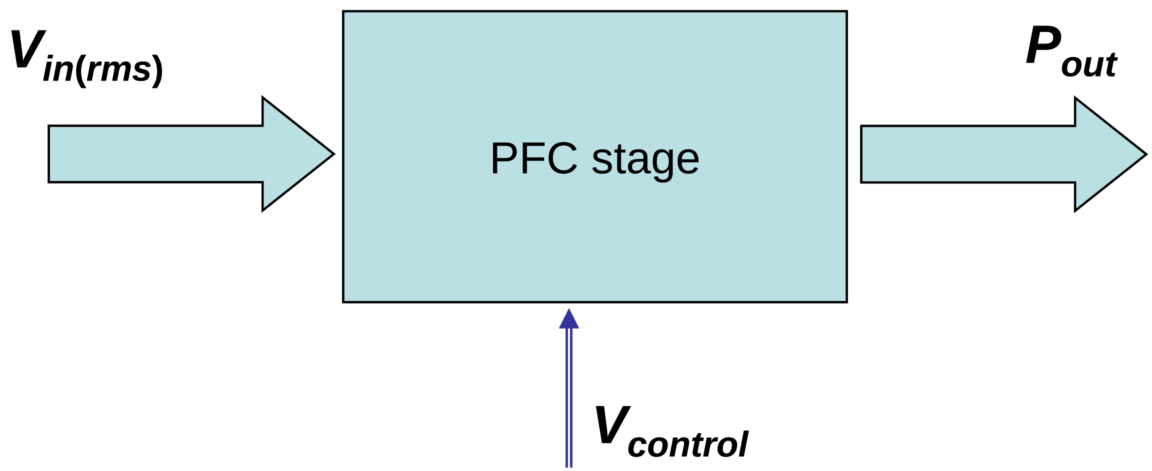
A Simple Representation

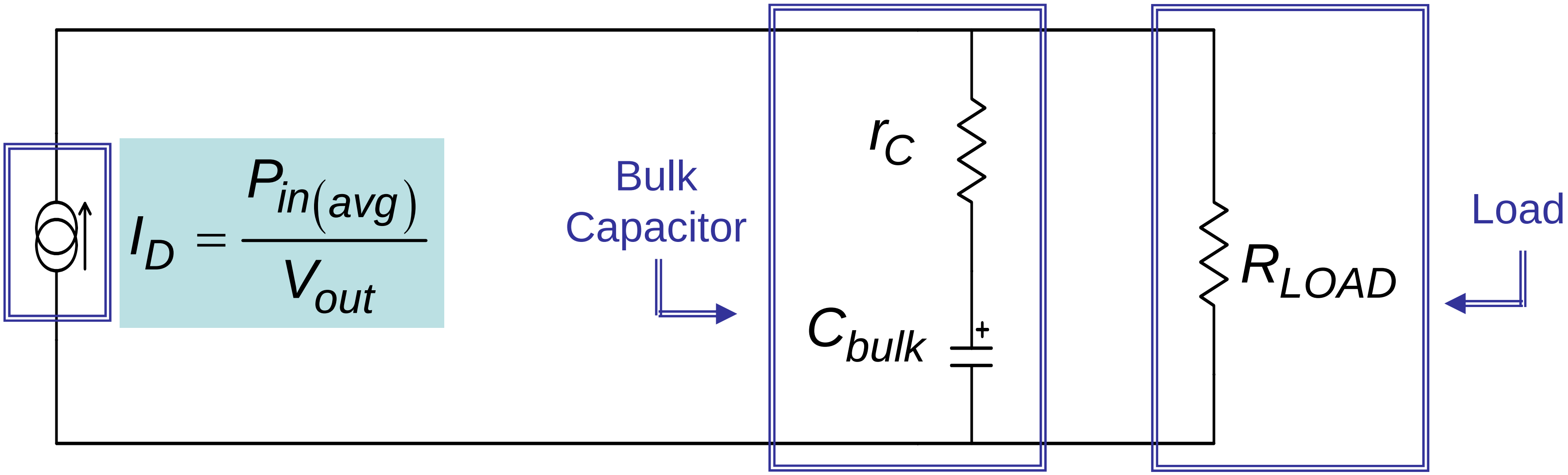
- We will consider the PFC stage as a system delivering a power under an input rms voltage and a control signal



- Details of the power processing are ignored:
  - Operation mode (CrM, CCM, Voltage or Current mode…)
  - 100% efficiency, only the average power contribution of the sinusoidal signals is considered

A Simple Large Signal Model

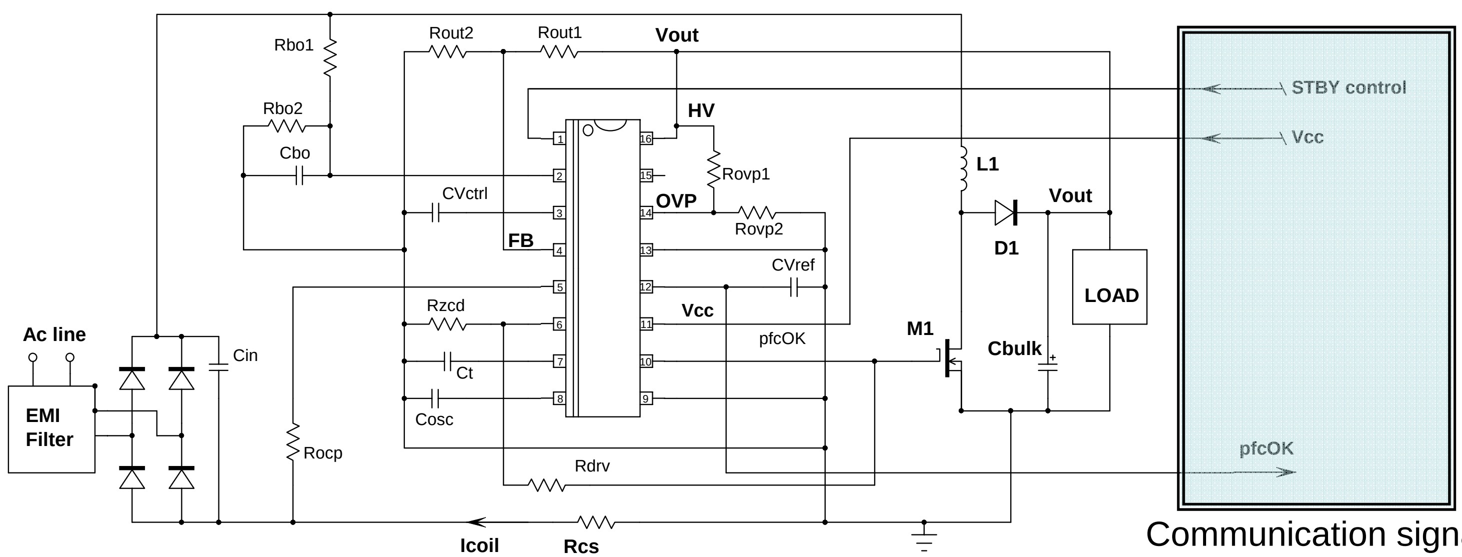
- Let's represent the PFC stage as a current source delivering the power to the bulk capacitor and the load:



- $P_{in(avg)}$ depends on $V_{control}$ (always), on $V_{in(rms)}$ (in the absence of feedforward) and sometimes on V_{out}
- 3 possible sources of perturbations: $V_{control}$, V_{out} and $V_{in(rms)}$.

NCP1605

- **Frequency Clamped Critical Conduction Mode (FCCrM)**
- Key features for a master PFC:
    - High voltage current source, Soft-Skip™ during standby mode
    - “pfcOK” signal, dynamic response enhancer
    - Bunch of protections for rugged PFC stages
- Markets: high power AC adapters, LCD TVs



Communication signals

NCP1605 – Follower Boost

- Voltage mode operation: the circuit adjusts the power level by modulating the MOSFET conduction time
- The charge current of the timing capacitor is proportional to the FB square and hence to $(\boldsymbol{V_{out}})^{\mathbf{2}}$:

$$I_{charge} = I_t \cdot \left(\frac{V_{out}}{V_{out,nom}} \right)^2$$

where :

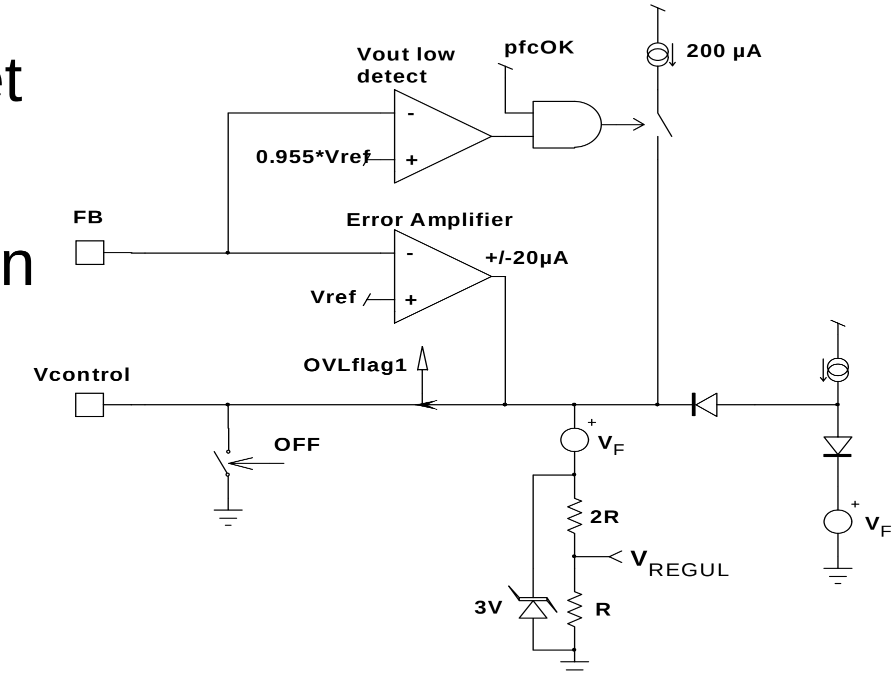
- $\boldsymbol{V_{out,nom}}$ is the V_{out} regulation voltage
- $\boldsymbol{I_t}$ is a 370-µA current source

- The on-time is inversely proportional to $(\boldsymbol{V_{out}})^{\mathbf{2}}$ allowing the Follower boost function:

$$t_{on} = \frac{C_t \cdot V_{ton}}{I_t} \cdot \left(\frac{V_{out,nom}}{V_{out}} \right)^2$$

NCP1605 - Power Expression

- The control signal is V_F offset down and divided by 3 to form V_{REGUL} used in the PWM section

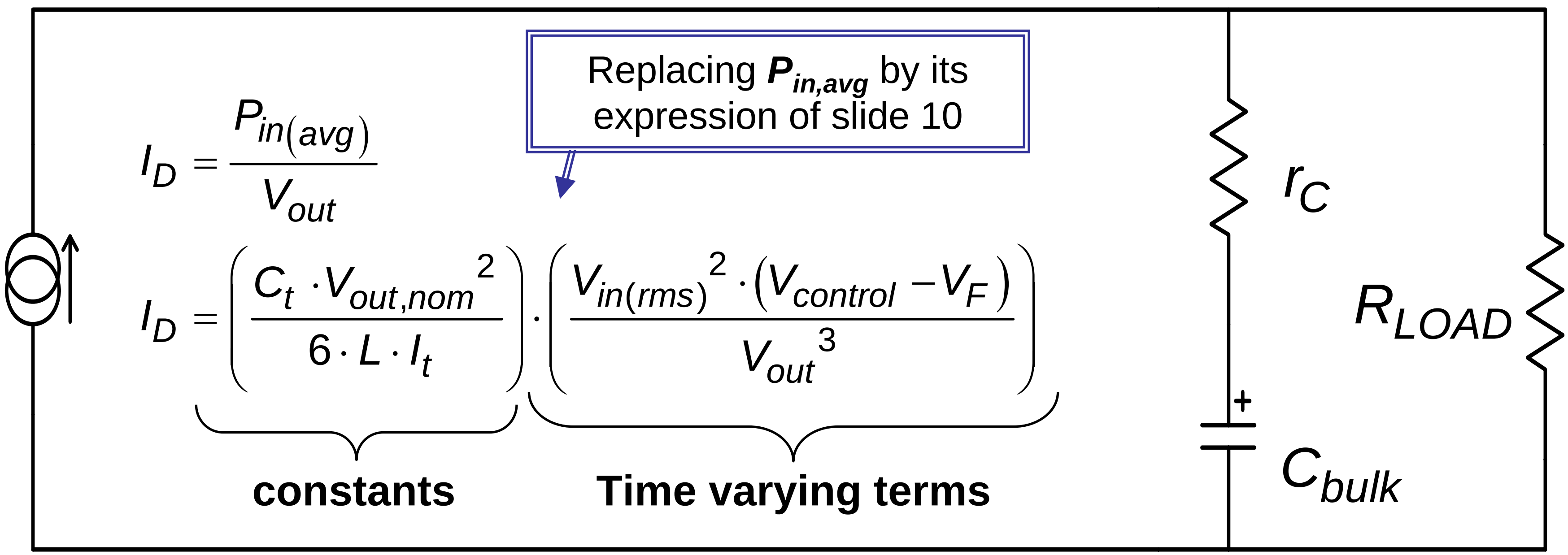


- Hence due to the follower boost function, the power is inversely dependent on $(\boldsymbol{V_{out}})^2$:

$$P_{in(avg)} = \frac{C_t \cdot V_{in(rms)}^2}{2 \cdot L \cdot I_t} \cdot \left(\frac{V_{out,nom}}{V_{out}}\right)^2 \cdot \frac{(V_{control} - V_F)}{3}$$

NCP1605 - Large Signal Model

- Let's represent the PFC stage as a current source delivering the power to the bulk capacitor and the load:



- 3 sources of perturbations: $V_{CONTROL}$, V_{out} and $V_{in(rms)}$.

Small Signal Model

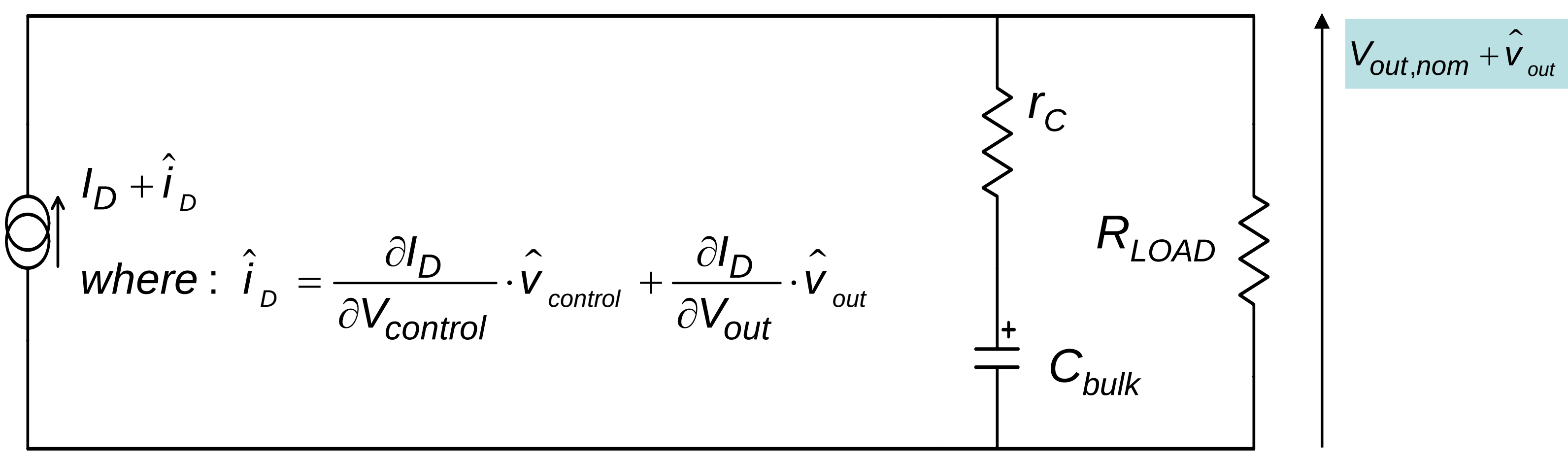
- A large signal model is nonlinear because I_D is formed of the multiplication and division of $V_{control}$, $V_{in,rms}$ and V_{out}.
- This model needs to be linearized to assess the AC contribution of each variable
- The model is perturbed and linearized around a quiescient operating point (DC point)

Considering Variations Around the DC Value…

- Let's omit the perturbations of the line magnitude (assumed constant)
- Let's consider small variations around the DC values for V_{out} and $V_{control}$:

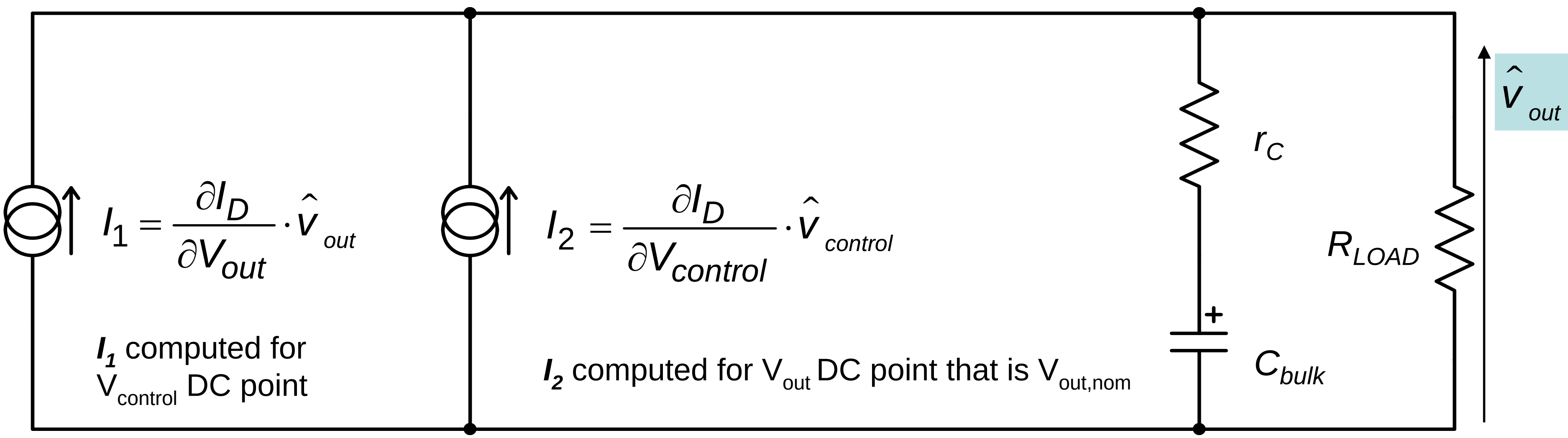
$$\hat{i}_D = \frac{\partial I_D}{\partial V_{control}} \cdot \hat{v}_{CONTROL} + \frac{\partial I_D}{\partial V_{out}} \cdot \hat{v}_{out}$$

- We then obtain:



Deriving a Small Signal Model…

- The DC portion can be eliminated
- The partial derivatives are to be computed at the DC point that is for:
  - $V_{control}$ that is the control signal DC value for the considered working point
  - $V_{out,nom}$ that is the nominal (DC) output voltage
- Replacing the derivations by their expression, we obtain:



Contribution of the V_{out} Perturbations

- Depending on the controller scheme

$$I_D = \frac{P_{in,avg}}{V_{out}} = \frac{f\left(V_{in(rms)}, V_{control}\right)}{\left(V_{out}\right)^{n+1}} \quad where\ n = 0{,}1\ or\ 2$$

  - n=0 for NCP1607
  - n=1 for NCP1654 (predictive CCM PFC for which $P_{in,avg} \propto \frac{V_{control} \cdot V_{in,rms}}{V_{out}}$)
  - n=2 for NCP1605 (follower boost – see slide 10)

- At the DC point

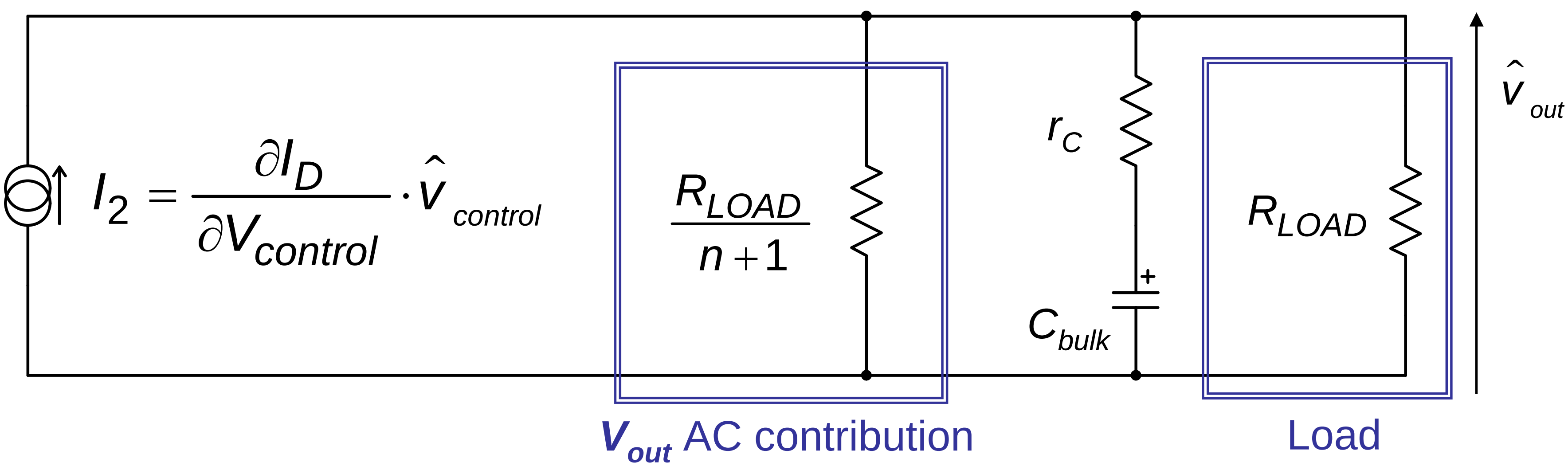
$$V_{out} = V_{out,nom} \quad and \quad \frac{P_{in(avg)}}{\left(V_{out,nom}\right)^2} = \frac{1}{R_{LOAD}}$$

- Finally:

$$I_1 = \frac{\partial I_D}{\partial V_{out}} \cdot \hat{v}_{out} = -\left.\frac{(n+1) \cdot f\left(V_{in(rms)}, V_{control}\right)}{\left(V_{out}\right)^{n+2}}\right|_{V_{out} = V_{out,nom}} \cdot \hat{v}_{out} = -\frac{(n+1) \cdot P_{in(avg)}}{\left(V_{out,nom}\right)^2} \cdot \hat{v}_{out} = -\frac{(n+1)}{R_{LOAD}} \cdot \hat{v}_{out}$$

2 Resistors…

- Hence, the small signal model can be simplified as follows:



- Noting that: $\frac{R_{LOAD}}{n+1} \parallel R_{LOAD} = \frac{R_{LOAD}}{n+2}$

the model can be further simplified

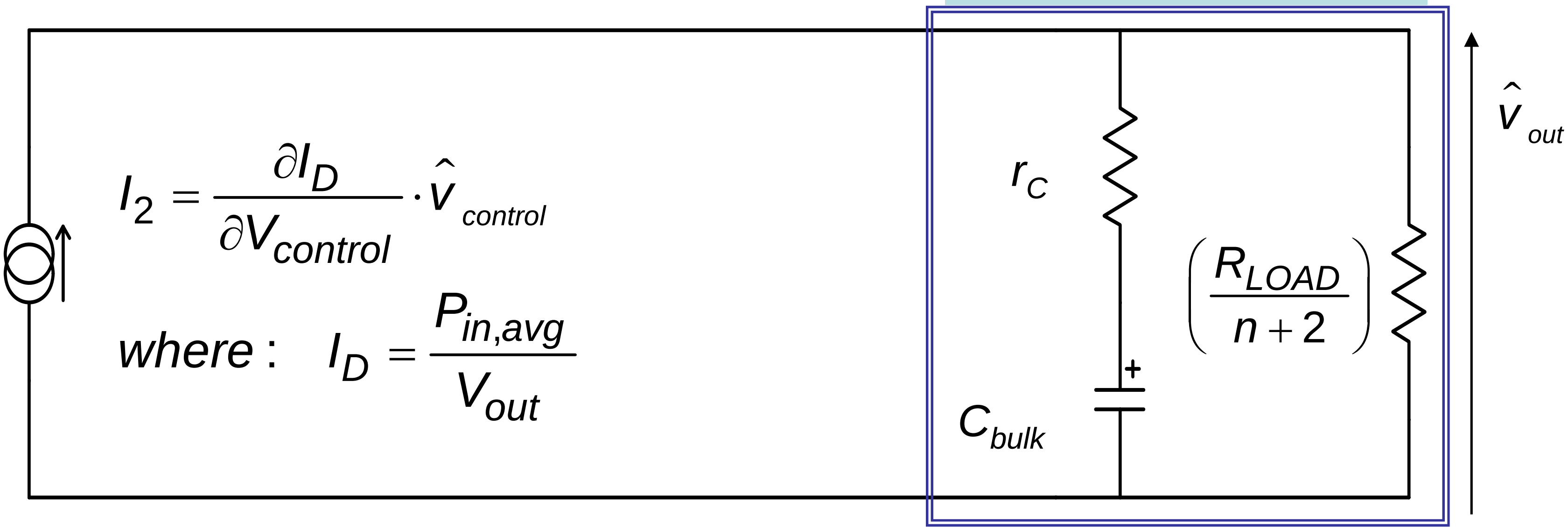
Finally…

❑ The small signal model is:

$$Z(s) = \frac{R_{LOAD}}{n+2} \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s\left(\frac{R_{LOAD} \cdot C_{bulk}}{n+2}\right)}$$

$$I_2 = \frac{\partial I_D}{\partial V_{control}} \cdot \hat{v}_{control}$$

$$\text{where}: \quad I_D = \frac{P_{in,avg}}{V_{out}}$$



❑ The transfer function is:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}} = \frac{R_{LOAD}}{n+2} \cdot \left(\frac{\partial I_D}{\partial V_{control}}\right) \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s\left(\frac{R_{LOAD} \cdot C_{bulk}}{n+2}\right)}$$

NCP1605 Example

- The large signal model instructed that:

$$I_D = \frac{P_{in(avg)}}{V_{out}} = \left(\frac{C_t \cdot V_{out,nom}^{\ \ 2}}{6 \cdot L \cdot I_t} \right) \cdot \left(\frac{V_{in(rms)}^{\ \ 2} \cdot (V_{control} - V_F)}{\boxed{V_{out}^{\ \ 3}}} \right)$$

$(V_{out})^{n+1}$ term

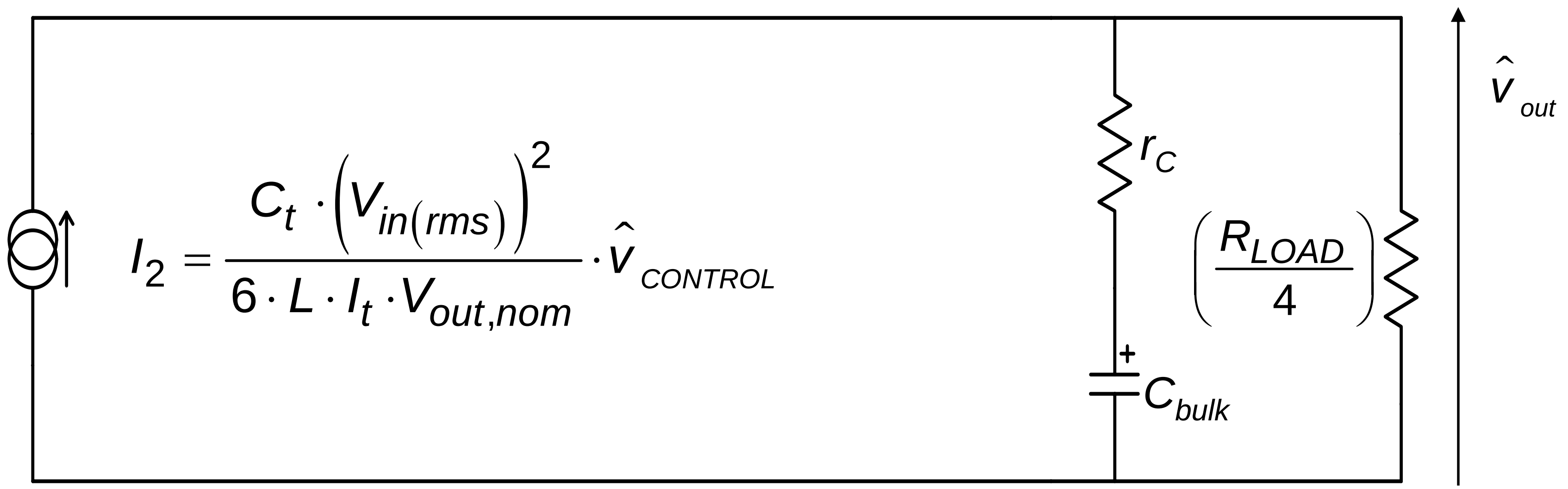
- Hence:

$$n = 2$$

$$\frac{\partial I_D}{\partial V_{control}} = \frac{C_t \cdot \left(V_{in(rms)} \right)^2}{6 \cdot L \cdot I_t \cdot V_{out,nom}}$$

NCP1605 - Small Signal Model

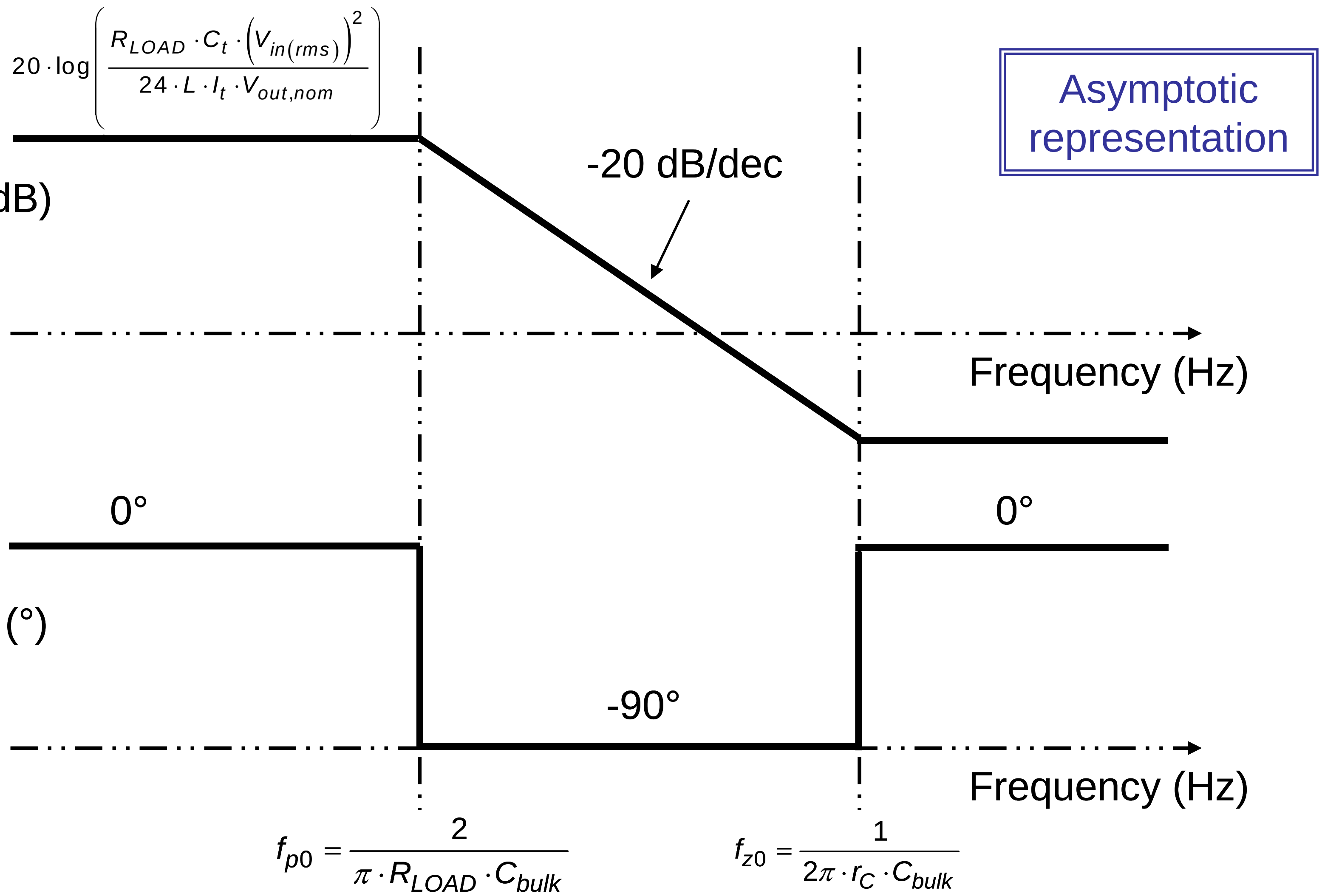
- Finally:



- The transfer function is:

$$\frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = \frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}} \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD} \cdot C_{bulk}}{4}\right)}$$

Power Stage Characteristic – Bode Plots



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Compensation Phase Boost

- The zero brought by the bulk capacitor ESR is too high to bring some phase margin. It is ignored.

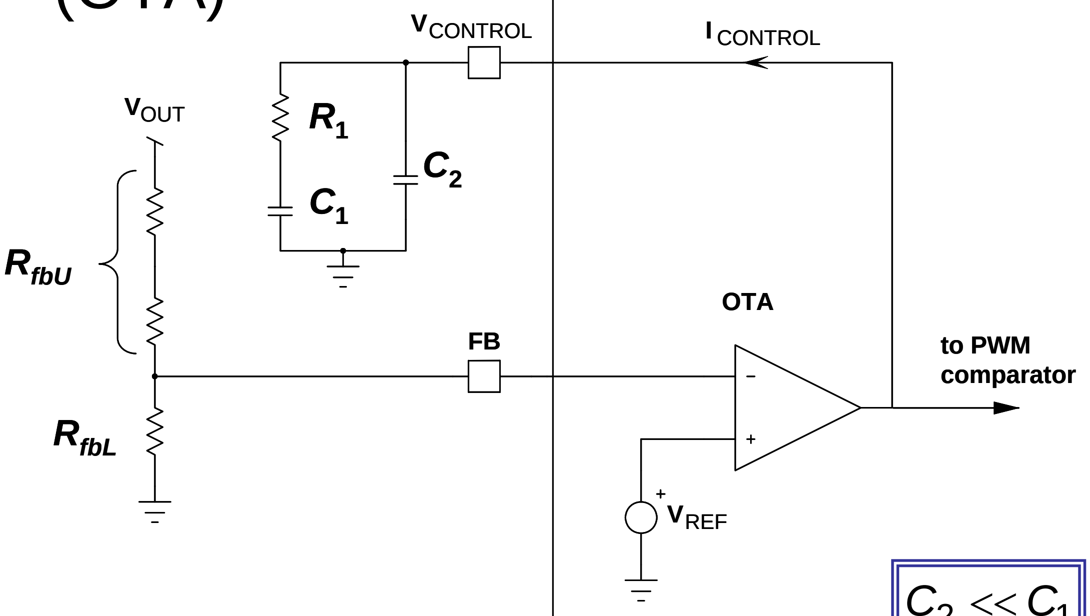
- The PFC open loop inherently causes a -360° phase shift:
  - Power stage pole ➔ -90°
  - Error amplifier inversion ➔ -180°
  - Compensation origin pole ➔ -90°

- The compensation must then provide some phase boost

- **A type-2 compensation is recommended**

Type-2 Compensation

- The NCP1605 embeds a transconductance error amplifier (OTA)



$$C_2 << C_1$$

$$f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$

$$f_{p2} = \frac{1}{2\pi \cdot R_1 \cdot C_2}$$

$$f_{p1} = \frac{1}{2\pi \cdot R_0 \cdot C_1}$$

pole at the origin

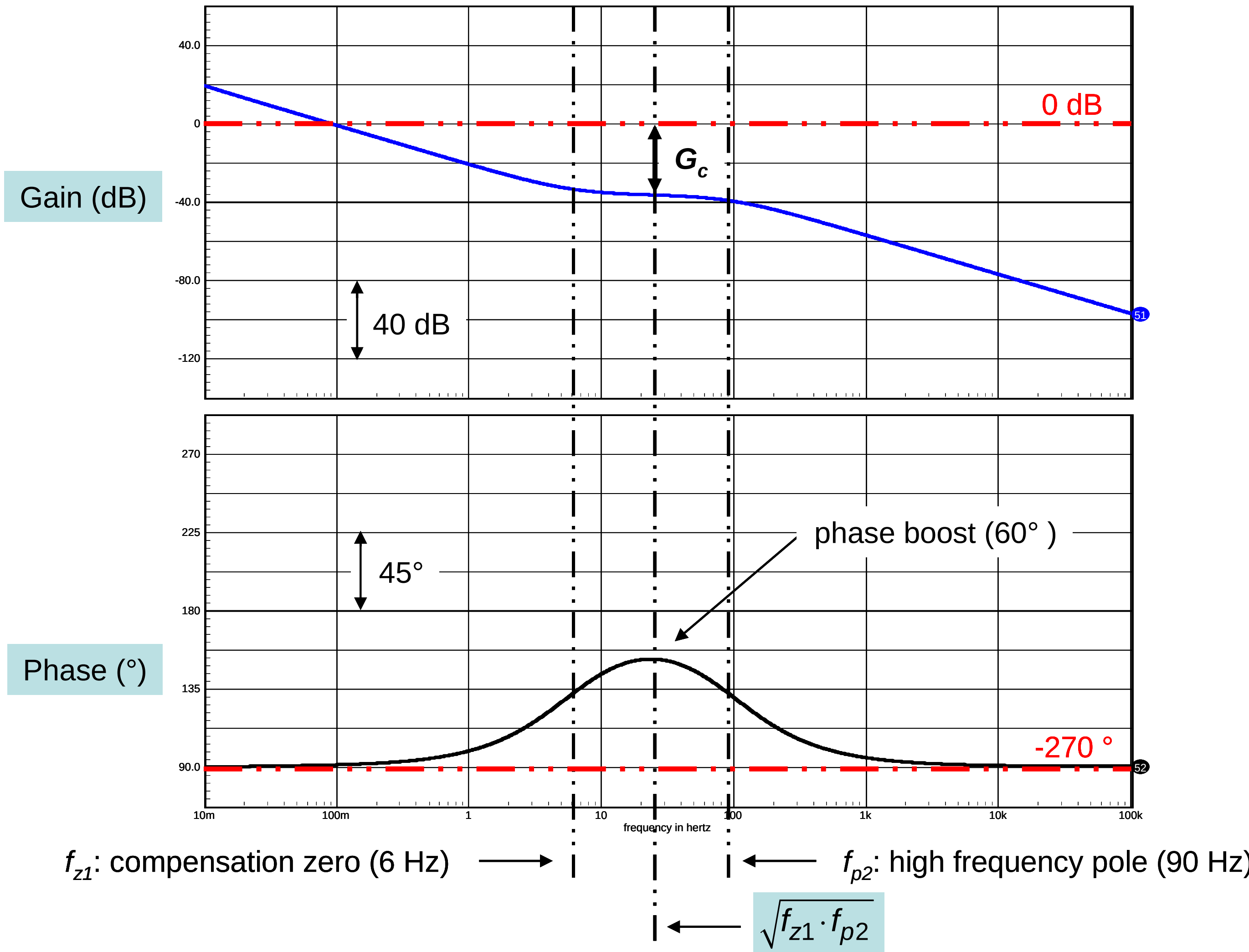
$$R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$$

- V_{ref} is the reference voltage (generally 2.5 V in ON semi devices)
- G_{EA} is the OTA (200-µS transconductance gain for NCP1605, NCP1654 and NCP1631)

  – No direct influence of the R_{fbU} impedance on the compensation

  – Only the feedback scale factor interferes

Type-2 Characteristic - Example

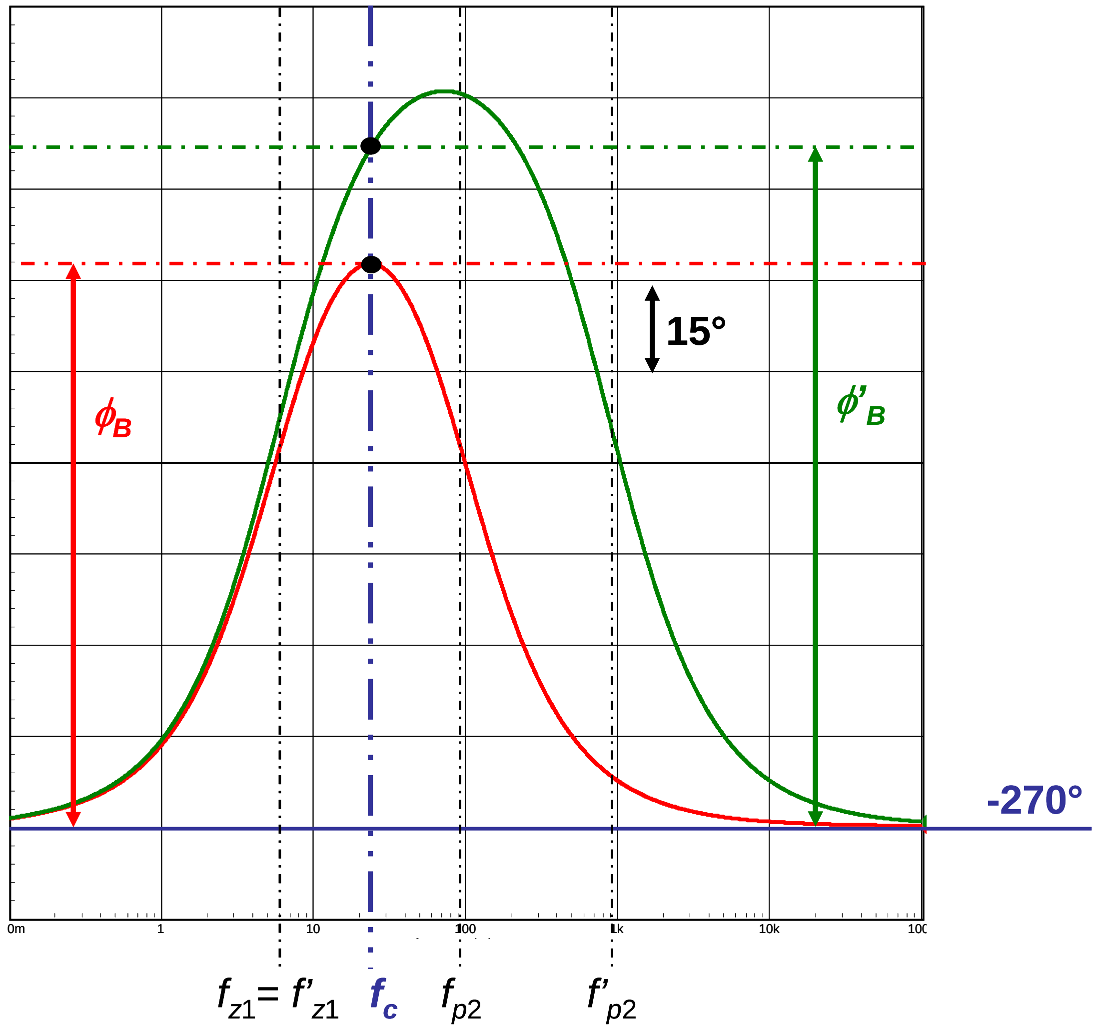


- ❑ f_{p2} and f_{z1} set the phase boost magnitude and location (frequency)
- ❑ The phase boost peaks at: $\left(f_{PhB} = \sqrt{f_{z1} \cdot f_{p2}}\right)$ that is 27 Hz
- ❑ The phase boost is:

$$\tan^{-1}\left(\frac{f_{phB}}{f_z}\right) - \tan^{-1}\left(\frac{f_{phB}}{f_p}\right)$$

- ❑ The origin pole f_{p1} adjusts the gain G_c at the phase boost frequency

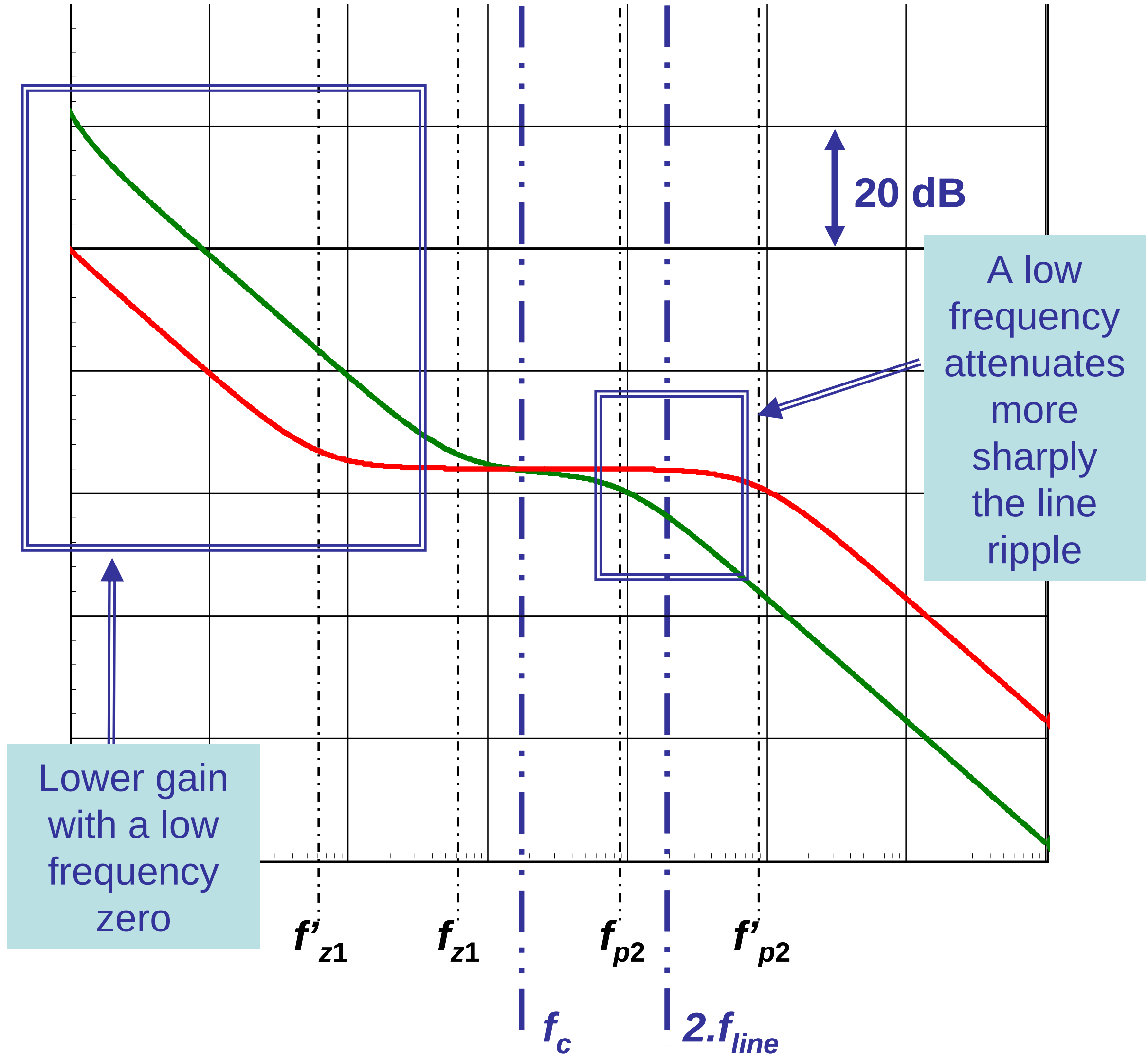
Phase Boost at the Crossover Frequency



$$\phi_B = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right)$$

- ❑ The lower $\boldsymbol{f_{z1}}$ and/or the higher $\boldsymbol{f_{p2}}$, the higher the phase boost (max. value: 90°)
- ❑ Assuming the PFC power stage pole is well below the crossover frequency ($\boldsymbol{f_c}$), the phase boost equates the phase margin ($\phi_m = \phi_B$)
- ❑ Target a phase boost between 45° and 75°

Gain Considerations



- In the red trace, the distance between the zero and the pole frequencies is increased
- Both characteristics generate the same attenuation at the crossover frequency
- The lower the f_{z1} frequency, the lower the gain in the low frequency region
- The higher f_{p2}, the lower the $(2.f_{line})$ ripple rejection

Type-2 Compensator - Summary

- The zero should not be placed at a too low frequency (not to penalize the low-frequency gain)
- The high frequency pole must be placed at a frequency low enough to attenuate the line ripple
- The phase boost (and phase margin) depends on the zero and high-frequency pole locations
- The origin pole is set to force the open loop gain to zero at the targeted crossover frequency

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Compensating for the Full Range?...

- The static gain depends on the load and if there is no feedforward, on the line magnitude

$$G_{static(dB)} = 20 \cdot \log\left(\frac{R_{LOAD}}{n+2} \cdot \left(\frac{\partial I_D}{\partial V_{control}}\right)\right) = 20 \cdot \log\left(\frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}\right) \qquad \text{(NCP1605)}$$

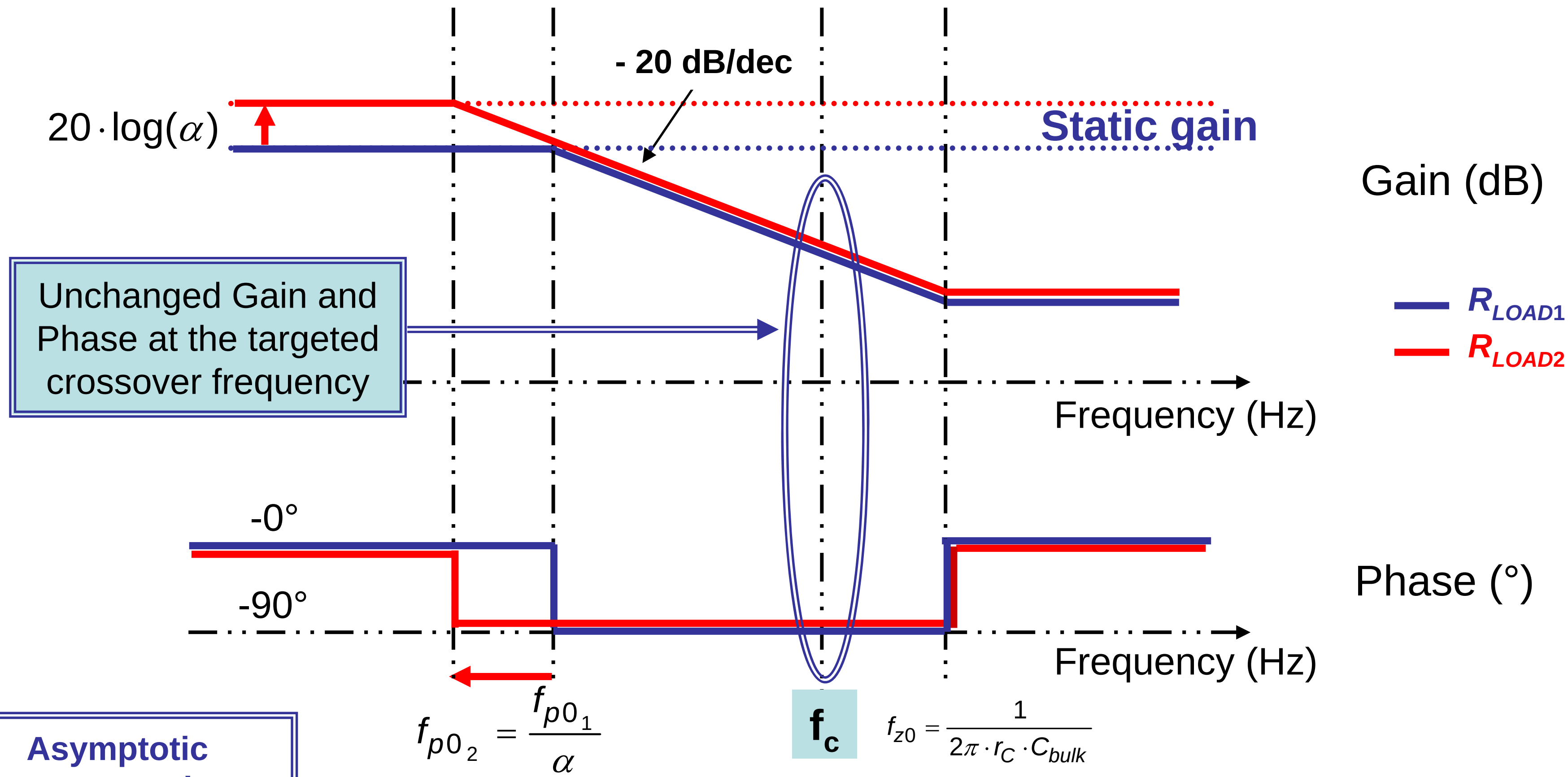
- The power stage pole varies as a function of the load:

$$f_{p0} = \frac{n+2}{2\pi \cdot R_{LOAD} \cdot C_{bulk}} = \frac{2}{\pi \cdot R_{LOAD} \cdot C_{bulk}} \qquad \text{(NCP1605)}$$

- What is the worst case when closing the loop?

Load Influence on the Open Loop Plots

- Let's increase R_{LOAD} $\left(R_{LOAD2} = \alpha \cdot R_{LOAD1} \quad with \quad \alpha > 1\right)$

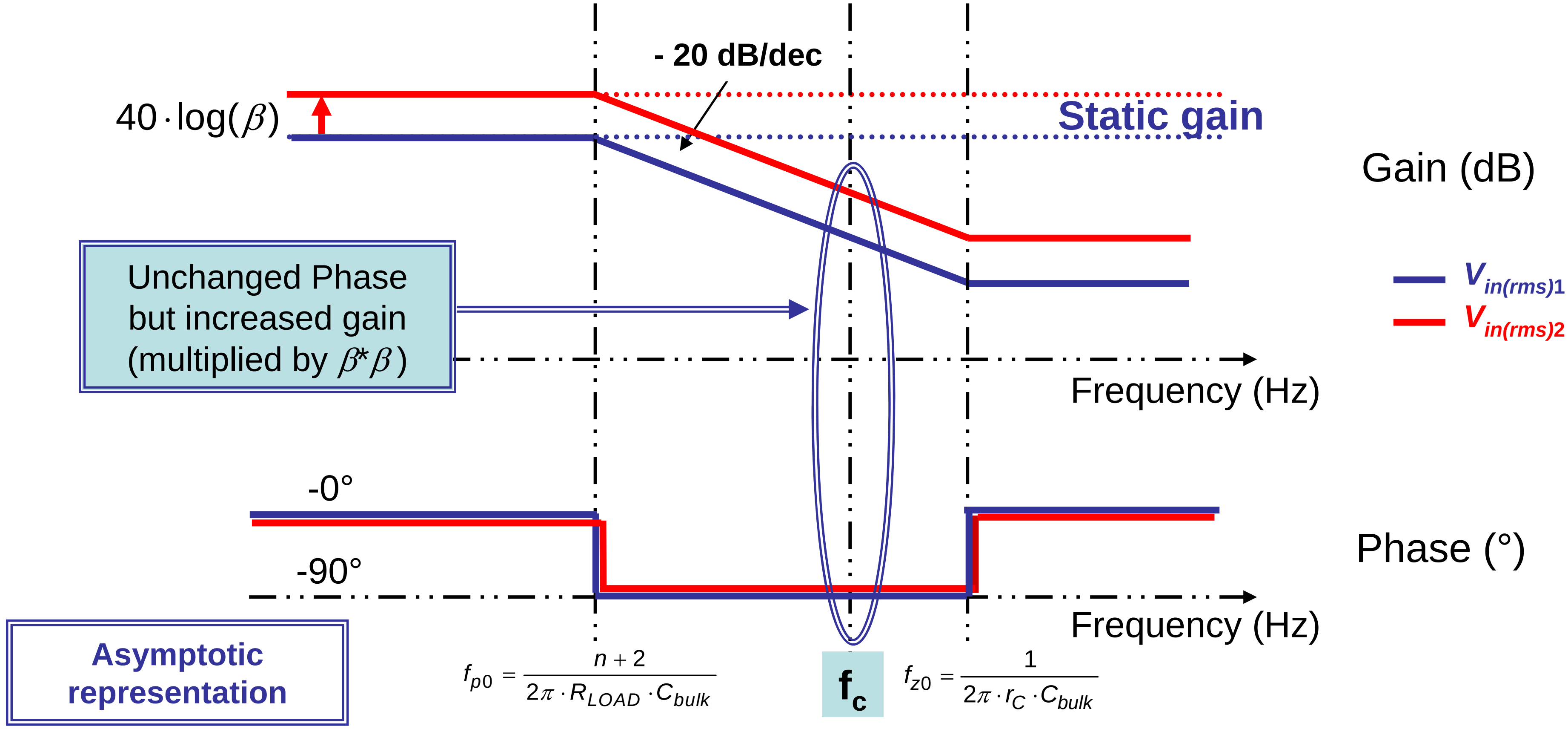


Asymptotic representation

f_c and ϕ_m are not affected!

Line Influence on the Open Loop Plots

- No feedforward (e.g. NCP1607) and $\left(V_{in(rms)2} = \beta \cdot V_{in(rms)1} \quad with \quad \beta > 1\right)$



The loop crossover frequency is β^2 increased

Load and Line Considerations

- Compensate at full load
  - Same crossover frequency at lighter loads
  - The zero frequency is set optimally (not at a too low frequency)

- Compensate at high line
  - High line is the worst case as in the absence of feedforward, the static gain is proportional to $\left(V_{in(rms)}\right)^2$
  - This leads to:

$$\left(f_c\right)_{HL} = \left(\frac{\left(V_{in(rms)}\right)_{HL}}{\left(V_{in(rms)}\right)_{LL}}\right)^2 \cdot \left(f_c\right)_{LL}$$

Where HL stands for Highest Line and LL for Lowest Line

  - In universal mains applications, the high-line crossover frequency is 9 times higher than the low-line one:

$$\left(f_c\right)_{HL} = \left(\frac{265}{90}\right)^2 \cdot \left(f_c\right)_{LL} \cong 9 \cdot \left(f_c\right)_{LL}$$

Crossover Frequency Selection

- In the absence of feedforward, $\left(f_c\right)_{HL} \le f_{line}$ is a good option
- With feedforward, $\left(f_c\right)_{HL} \le \frac{f_{line}}{2}$ is rather selected for a better attenuation of the low frequency ripple
- Get sure that on the line range, the PFC boost pole remains lower than the crossover frequency at full load!

$$f_{p0} \le \left(f_c\right)_{LL}$$

- If not, increase $\boldsymbol{C_{bulk}}$

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Compensation Techniques

- Several techniques exist:
  - manual placement, “k factor” (Venable)…

    \+ Systematic

    \- The PFC boost gain is to be computed at $\boldsymbol{f_c}$

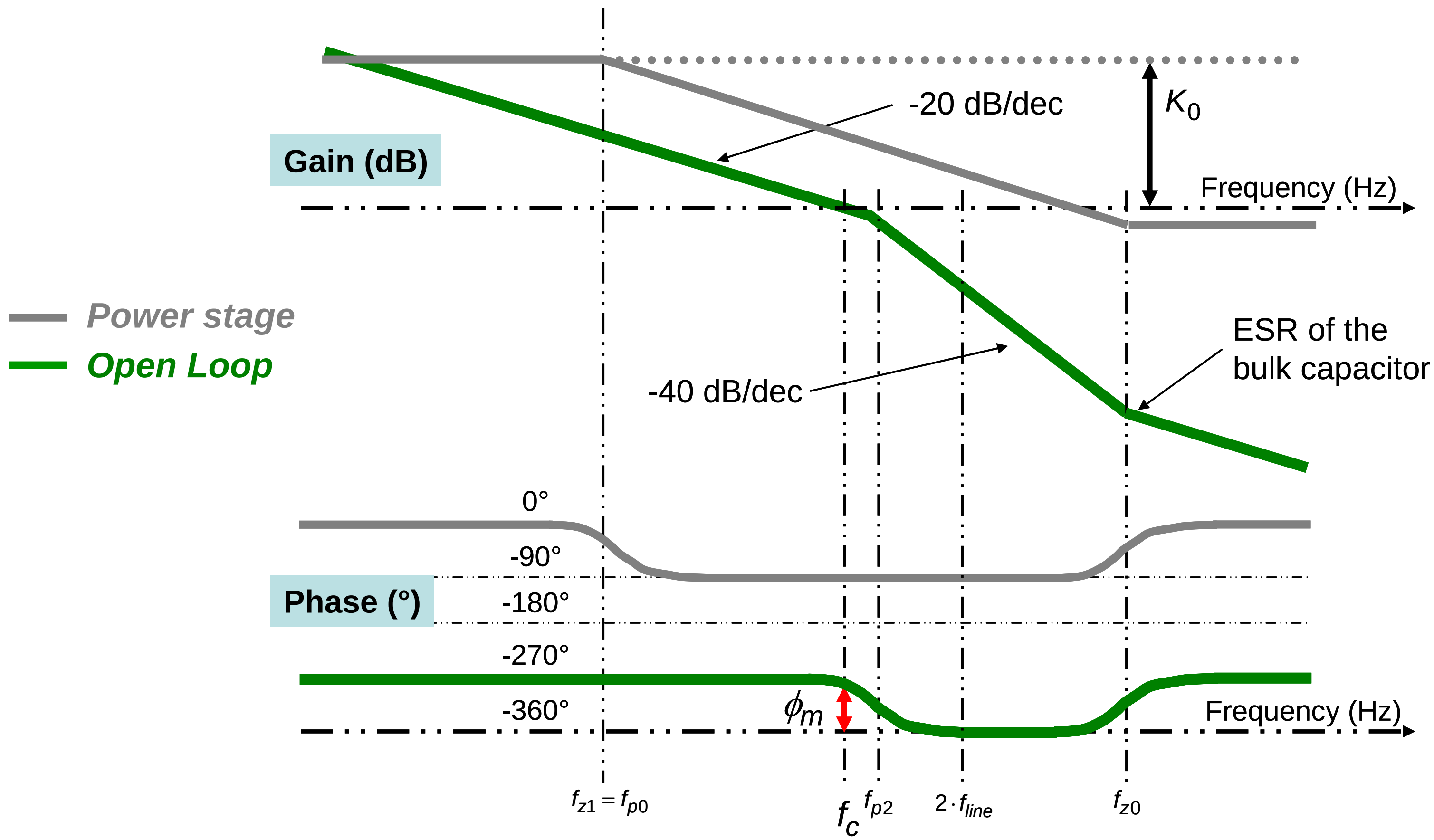
    \- No flexibility in the zero and high pole locations $f_c = k \cdot f_{z1} = \frac{f_{p2}}{k}$
  - Pole and zero cancellation:

    ✓ Place the compensation zero so that it cancels the power stage pole:

    ✓ Force the pole at the origin to cancel the PFC boost gain when ($f = f_c$)

    ✓ Adjust the phase margin with the high frequency pole

Pole and Zero Cancellation…



- The higher $\boldsymbol{f_{p2}}$, the larger the phase margin
- The lower $\boldsymbol{f_{p2}}$, the better the rejection of the low frequency ripple
- $\phi_m = 45°$ if $f_{p2} = f_c$.

Poles and Zero Placement

- Design the compensation for full load, high line: $R_{LOAD} = R_{LOAD(\min)}$

- Place the origin pole to cancel K_0, the static gain at f_c:

$$f_{p0} = \frac{f_c}{K_0} \quad for \quad R_{LOAD} = R_{LOAD(\min)}$$

$$where: \frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = K_0 \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD(\min)} \cdot C_{bulk}}{n+2} \right)}$$

- Place the zero so that it cancels the PFC boost pole

$$\left(f_{z1} = f_{p0} \right) \quad for \quad R_{LOAD} = R_{LOAD(\min)}$$

- Place $\boldsymbol{f_{p2}}$ to obtain the targeted phase margin: $f_{p2} = \frac{f_c}{\tan\left(90° - \phi_m\right)}$

Example

- A wide mains, 150-W application driven by the NCP1605
- $V_{out,nom}$ = 390 V
- $(V_{in(rms)})_{LL}$ = 90 V
- $(V_{in(rms)})_{HL}$ = 265 V
- L = 150 µH
- C_t = 4.7 nF
- C_{bulk} = 100 µF
- r_C = 500 mΩ (ESR)
- f_c = 50 Hz

and Φ_m = 60°

@ high line (265 V)

$$\frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = K_0 \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD} \cdot C_{bulk}}{4} \right)} \quad where: \quad K_0 = \frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)} \right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}$$

$$R_{LOAD(\min)} = \frac{\left(V_{out,nom} \right)^2}{\left(P_{out} \right)_{\max}} = \frac{390^2}{150} \cong 1\,k\Omega$$

$$R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}} = \frac{390}{2.5 \cdot 200 \cdot 10^{-6}} = 780\,k\Omega \quad (OTA)$$

$$C_1 = \frac{K_{0(\min)}}{2\pi \cdot f_c \cdot R_0} = \frac{R_{LOAD(\min)} \cdot C_t \cdot \left(V_{in(rms)} \right)_{HL}^2}{2\pi \cdot f_c \cdot R_0 \cdot 24 \cdot L \cdot I_t \cdot V_{out,nom}} = \frac{10^3 \cdot 4.7 \cdot 10^{-9} \cdot 265^2}{2\pi \cdot 50 \cdot 780k \cdot 24 \cdot 150\mu \cdot 370\mu \cdot 390} \cong 2.59\mu F \quad ==> \quad 2.2\,\mu F$$

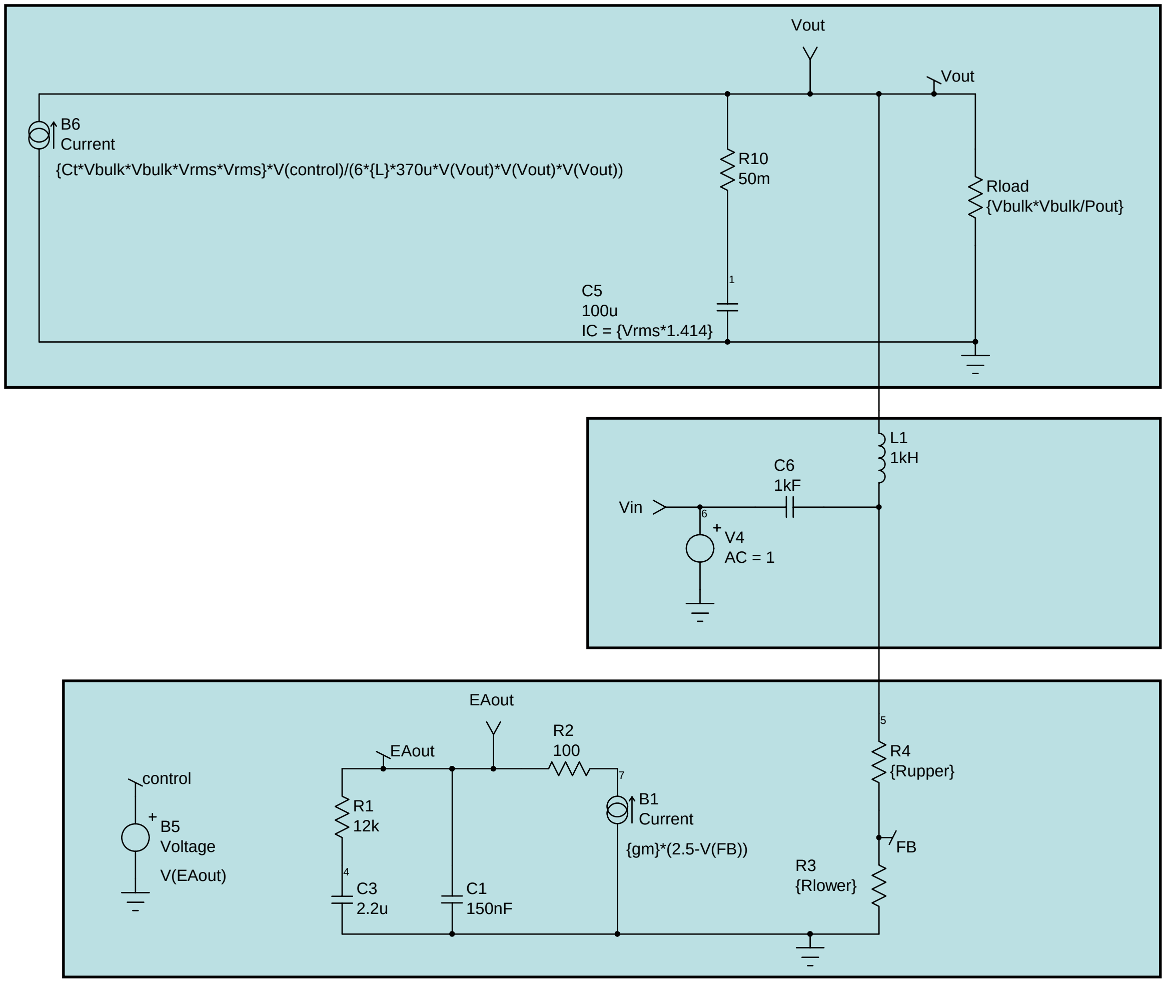
$$R_1 = \frac{R_{LOAD(\min)} \cdot C_{bulk}}{(n+2) \cdot C_1} = \frac{10^3 \cdot 100 \cdot 10^{-6}}{(2+2) \cdot 2.2 \cdot 10^{-6}} \cong 11.36\,k\Omega \quad ==> \quad 12\,k\Omega$$

$$C_2 = \frac{\tan\left(90° - \phi_m \right)}{2\pi \cdot f_c \cdot R_1} = \frac{\tan\left(90° - 60° \right)}{2\pi \cdot 50 \cdot 12 \cdot 10^3} \cong 153\,nF \quad ==> \quad 150\,nF$$

$$f_{p1} = \frac{1}{2\pi \cdot R_0 \cdot C_1} = 93\,mHz \qquad f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = 6\,Hz \qquad f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 88\,Hz$$

Simulation Validation

- The simulation circuit is based on the large signal model:

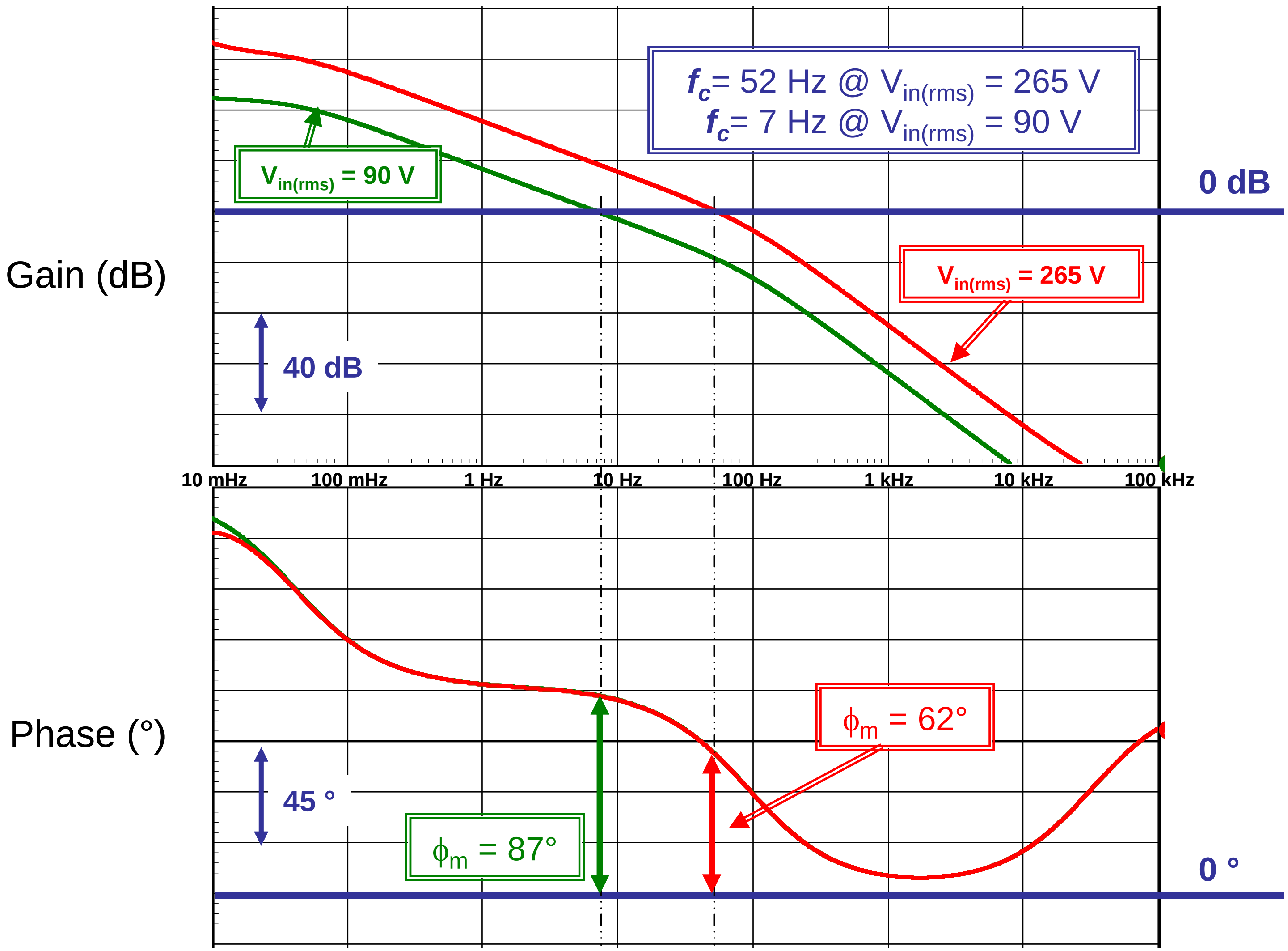


Large signal model of the NCP1605-driven PFC stage

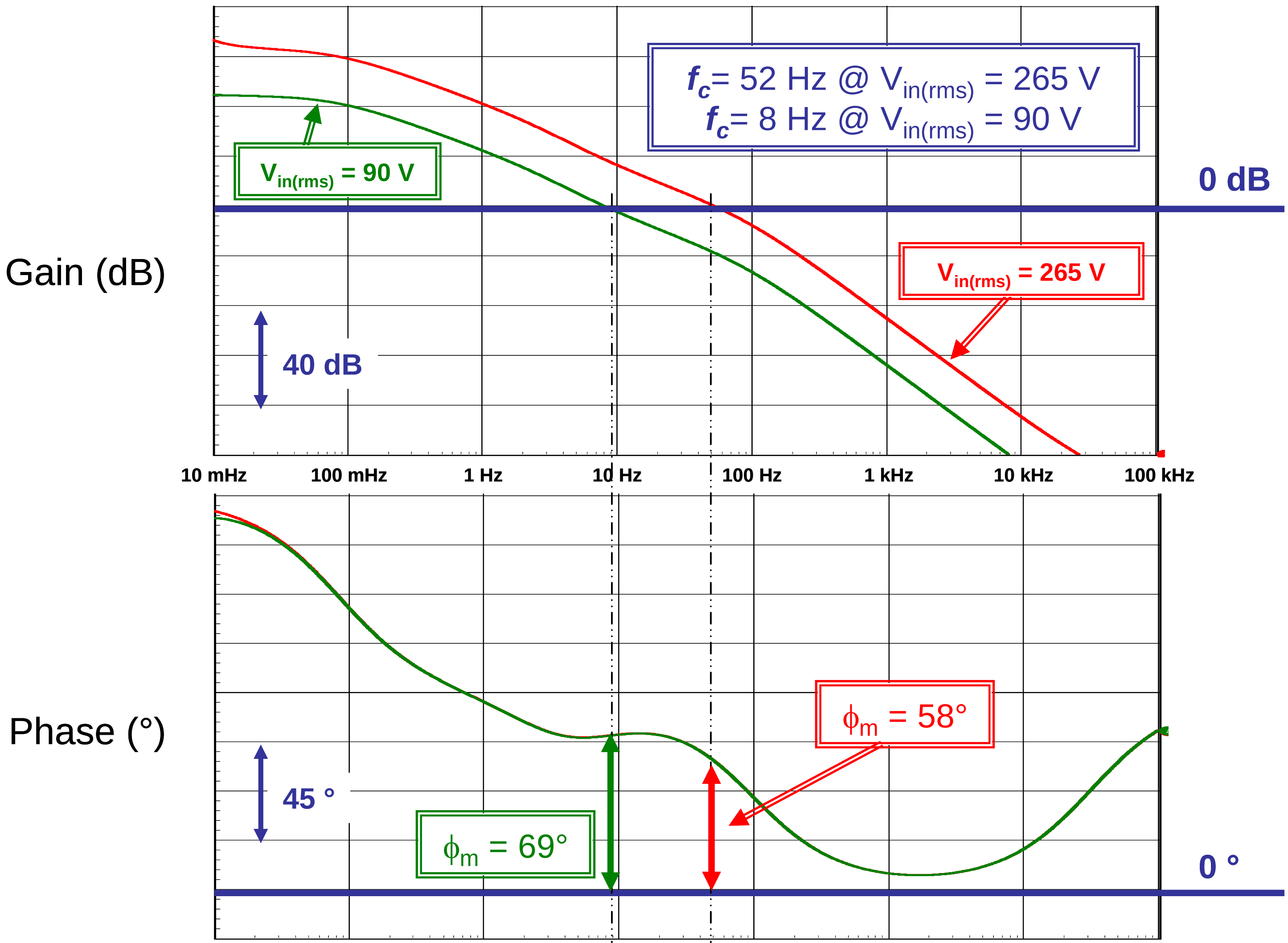
Generation and injection of the ac perturbation

Feedback and regulation circuit (including type-2 compensation)

Open Loop Characteristic – Full Load

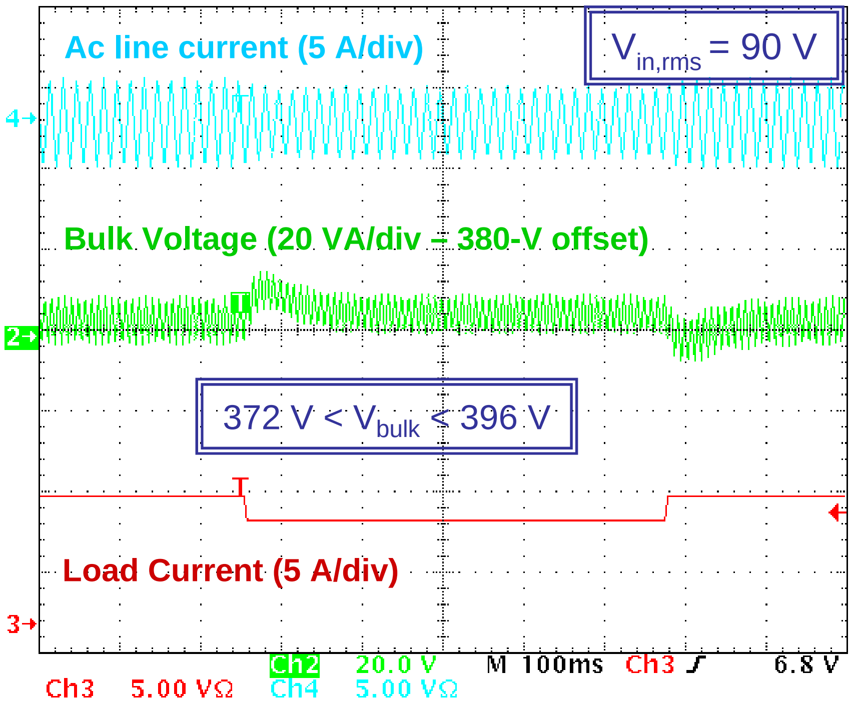


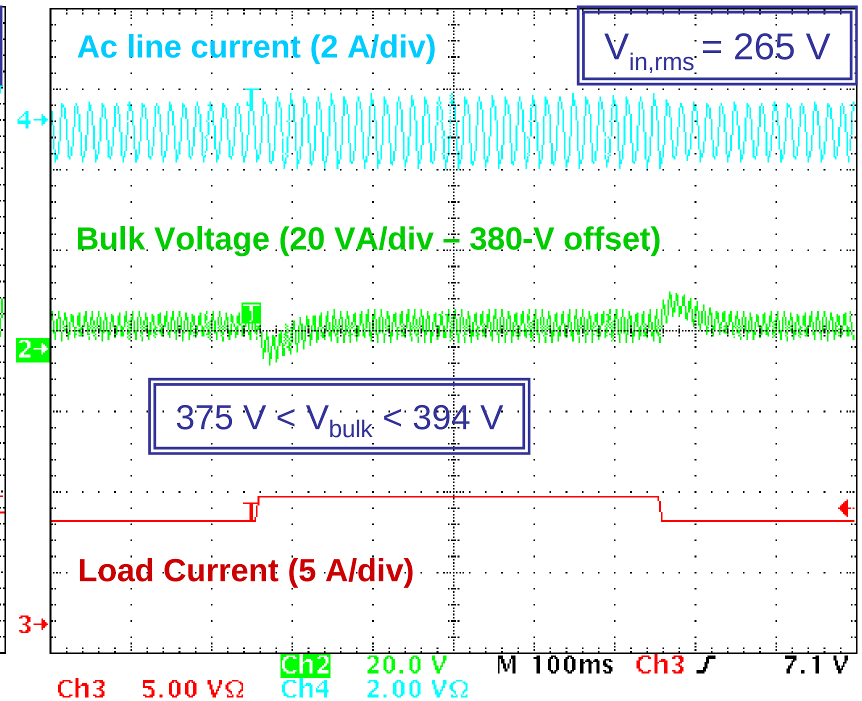
Open Loop Characteristic – Mid Load



Experimental Results at Full Load

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings between 6.3 A and 7.7 A (+/-10%) with a 2 A/µs slope

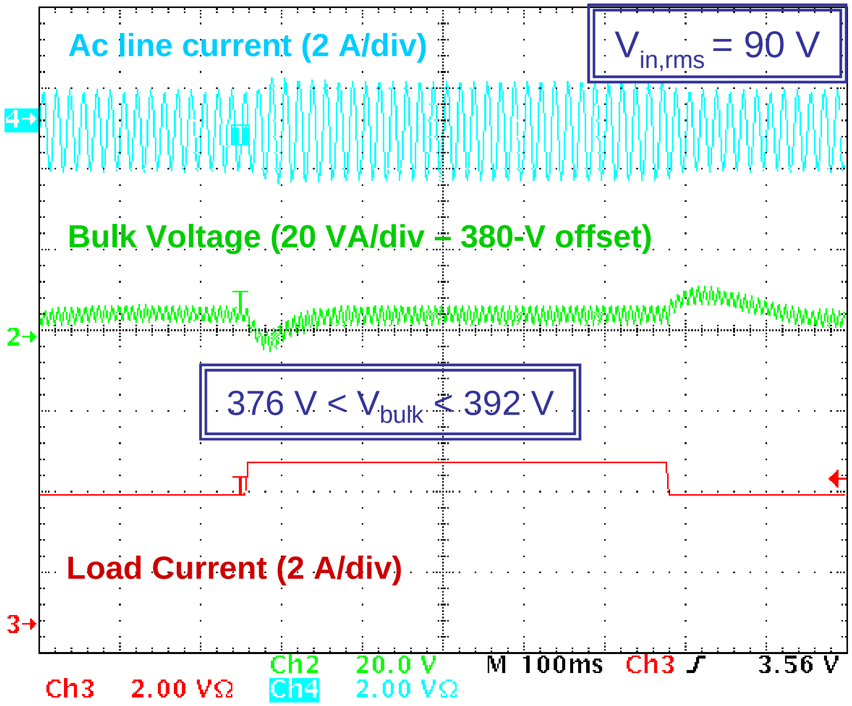


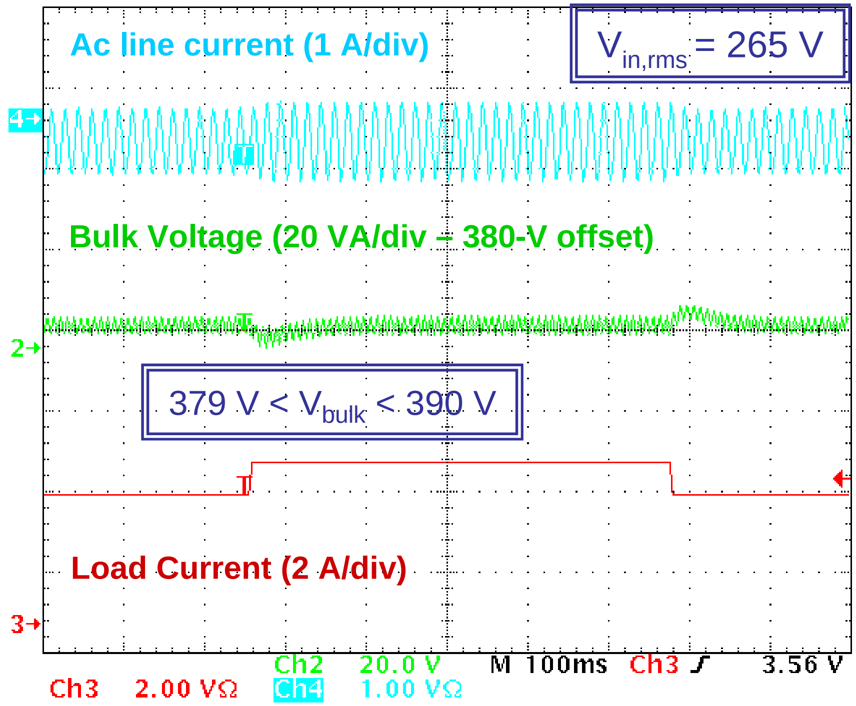


- The high-line, larger bandwidth reduces the V_{bulk} deviations and speeds-up the output voltage recovery

Experimental Results at Medium Load

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings between 3.1 A and 3.9 A (+/-10%) with a 2 A/µs slope

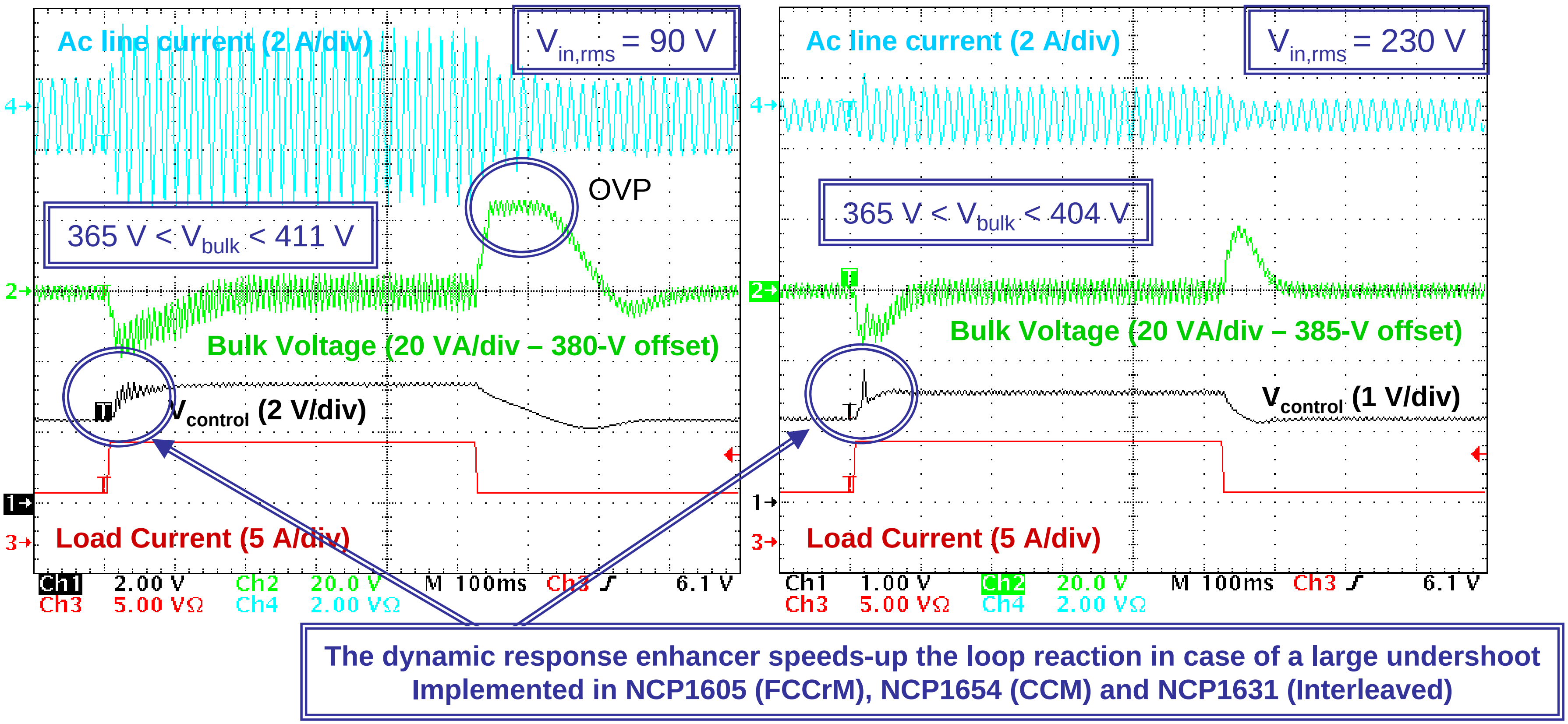




- The circuit still exhibits a first order response

Abrupt Load Changes

- A 19 V / 7 A loads the PFC stage
- The downstream converter swings from 7.0 A to 3.5 A (2 A/µs slope)



- The dynamic response enhancer reduces the undershoot at low line

Agenda

- Introduction
- Deriving a small-signal model
  - General method
  - Practical example: NCP1605-driven PFC stages
- Compensating the loop
  - Type-2 compensation
  - Influence of the line and power level
  - Computing the compensation
  - Practical example
- Conclusion

Conclusion

- General considerations were illustrated by the case of NCP1605-driven PFC stages
- A small signal model of PFC boosts can be easily derived
- The proposed method is independent of the operating mode
- A type-2 compensation is recommended
- If no feed-forward is implemented, the loop bandwidth and phase margin vary as a function of the line magnitude
- The crossover frequency does not vary as a function of the load
- A resistive load can be used for the computation even if the PFC stage feeds a power supply (negative impedance) – See back-up

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies