ON Semiconductor

Interleaved PFC
Agenda

- Introduction:
  - Basics of interleaving
  - Main benefits
- NCP1631: a novel controller for interleaved PFC
  - Out-of-phase management
  - The NCP1631 allows the use of smaller inductors
  - Main functions
- Experimental results and performance
  - General waveforms
  - Efficiency
- Conclusion
Interleaved PFC

- Two small PFC stages delivering $(P_{in(\text{avg})}/2)$ in lieu of a single big one

- If the two phases are out-of-phase, the resulting currents $(I_{L(\text{tot})})$ and $(I_{D(\text{tot})})$ exhibit a dramatically reduced ripple.
Interleaved Benefits

- More components but:
  - A 150 W PFC is easier to design than a 300 W one
  - Modular approach
  - Better heating distribution
  - Extended range for Critical Conduction Mode (CrM)
  - Smaller components

(help meet strict form factor needs – e.g., flat panels)
- **Two DCM PFCs look like a CCM PFC converter…**
  - Eases EMI filtering and reduces the output rms current
Input and Output Current

What is the ripple of the $I_{L(tot)}$ total input current?

What is the ripple of the $I_{D(tot)}$ total output current?
Input Current Ripple at Low Line

- When $V_{in}$ remains lower than $V_{out}/2$, the input current looks like that of a CCM, hysteretic PFC.
- $(I_{L(tot)})$ swings between two nearly sinusoidal envelopes.

![Diagram showing peak, averaged, and valley current at 90 Vrms, 320 W input (Vout = 390 V).]
Input Current Ripple at High Line

- When $V_{in}$ exceeds $(V_{out}/2)$, the valley current is constant!
- It equates $\left( \frac{V_{out}}{2 \cdot R_{in}} \right)$ where $R_{in}$ is the PFC input impedance

\[ P_{in(\text{avg})} \cdot V_{out} = \frac{V_{out}}{2 \cdot R_{in}} \]
Line Input Current

- For each branch, somewhere within the sinusoid:
  \[ I_L(t) = \frac{1}{2} \cdot 2 \cdot \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}} \]

- The sum of the two averaged, sinusoidal phases currents gives the total line current:
  \[ I_{in} = \frac{\langle I_{L(tot)} \rangle_{T_{sw}}}{2} = \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}} \]

- Assuming a perfect current balancing:
  \[ 2 \cdot \langle I_{L1} \rangle_{T_{sw}} = 2 \cdot \langle I_{L2} \rangle_{T_{sw}} = I_{in} \]

- The peak current in each branch is \( I_{in}(t) \)
Ac Component of the Refueling Current

- The refueling current (output diode(s) current) depends on the mode:

  - **Single phase CCM**
    - \( I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}} \)
    - \( I_{in} \):
  
  - **Single phase CrM**
    - \( \frac{2}{\sqrt{3}} \cdot I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}} \)
    - \( \frac{2}{\sqrt{3}} \): rms value over \( T_{sw} \)
  
  - **Interleaved CrM**
    - \( \sqrt{\frac{2}{3}} \cdot I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}} \)
    - \( \sqrt{\frac{2}{3}} \): rms value over \( T_{sw} \)
A Reduced Rms Current in the Bulk Capacitor

- Integration over the sinusoid leads to (resistive load):

<table>
<thead>
<tr>
<th></th>
<th>Single phase CCM PFC</th>
<th>Single phase CrM or FCCrM* PFC</th>
<th>Interleaved CrM or FCCrM* PFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode(s) rms current (I_D^{(\text{rms})})</td>
<td>[\sqrt{\frac{8\sqrt{2}}{3\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}}]</td>
<td>[\frac{2}{\sqrt{3}} \cdot \sqrt{\frac{8\sqrt{2}}{3\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}}]</td>
<td>[\sqrt{\frac{2}{3\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}}]</td>
</tr>
<tr>
<td>Capacitor rms current (I_C^{(\text{rms})})</td>
<td>[\sqrt{\frac{8\sqrt{2}}{3\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}} - \left(\frac{P_{\text{out}}}{V_{\text{out}}}\right)^2]</td>
<td>[\sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}} - \left(\frac{P_{\text{out}}}{V_{\text{out}}}\right)^2]</td>
<td>[\sqrt{\frac{16\sqrt{2}}{9\pi} \cdot \left(\frac{P_{\text{out}}}{\eta}\right)^2 \cdot V_{\text{in(rms)}} \cdot V_{\text{out}}} - \left(\frac{P_{\text{out}}}{V_{\text{out}}}\right)^2]</td>
</tr>
<tr>
<td>300 W, (V_{\text{out}}=390) V, (V_{\text{in(rms)}}=90) V</td>
<td>(I_D^{(\text{rms})} = 1.9) A (I_C^{(\text{rms})} = 1.7) A</td>
<td>(I_D^{(\text{rms})} = 2.2) A (I_C^{(\text{rms})} = 2.1) A</td>
<td>(I_D^{(\text{tot})^{(\text{rms})}} = 1.5) A (I_C^{(\text{rms})} = 1.3) A</td>
</tr>
</tbody>
</table>

- Interleaving dramatically reduces the rms currents
  
  ➔ reduced losses, lower heating, increased reliability

* Frequency Clamped CrM
Finally…

- Interleaved PFC combines:
  - The advantages of CrM operations
    - No need for low $t_{rr}$ diode
    - High efficiency
  - A reduced input current ripple and a minimized rms current in the bulk capacitor
  - A better distribution of heating
- More components but “small” ones
- Well adapted to slim form factor applications such as notebook adapters and LCD TVs
- Refer to application note AND8355 for more details
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NCP1631 Overview

- Interleaved, 2-phase PFC controller
- **Frequency Clamped Critical conduction Mode (FCCrM)** to optimize the efficiency over the load range.
- Substantial out-of-phase operation in all conditions including start-up, OCP or transient sequences.
- Feedforward for improved loop compensation
- Eased design of the downstream converter:
  - pfcOK, dynamic response enhancer, standby management
- High protection level:
  - Brown-out protection, accurate 1-pin current limitation, in-rush currents detection, separate pin for (programmable) OVP…
NCP1631 Overview

- Interleaved, 2-phase PFC controller

Zero voltage detection (branch1)

- Fixes the max. on-time
- Feed-forward

Zero voltage detection (branch2)

- Fixes the max. switching frequency

Adjusts the regulation loop bandwidth

Adjusts the Frequency Foldback characteristic

Brown-out detection with a 50-ms blanking delay to meet hold-up time requirements

Over and Under voltage protection (OVP, UVP)

Latch input: if $V_{\text{Latch}} > 2.5$ V, the controller shuts down

One CS pin to sense the total input current for Over-Current Protection and Inrush detection

High (5 V) when PFC is ready (steady state)

Over and Under voltage protection (OVP, UVP)
NCP1631 Typical Application

Synchronization of phases is completely internal

Indicates the downstream converter that the PFC is ready

1 current sense resistor
Interleaving: Master / Slave Approach…

- The master branch operates freely
- The slave follows with a 180° phase shift
- Main challenge: maintaining the CrM operation (no CCM, no dead-time)

![Diagram showing inductor unbalance and on-time shift]

Current mode: inductor unbalance  
Voltage mode: on-time shift

$L_2 < L_1$
Interleaving: Interactive-Phase Approach...

- Each phase properly operates in CrM
- The two branches interact to set the 180° phase shift
- Main challenge: to keep the proper phase shift

On-time perturbation for one phase

CrM operation is maintained but a perturbation of the on-time may degrade the 180° phase shift

We selected this approach
Interleaving Management

- The oscillator manages the out-of-phase operation
- It acts as the *interleaved clocks generator*

![Diagram of interleaving management with waveforms for CRM and DCM operations](image-url)
Current Balancing between the 2 Branches

- The NCP1631 operates in voltage mode
- Same on-time and hence switching period in the two branches
- An imbalance in the inductors:
  - Does not affect the switching period
  - “Only” causes a difference in the power amount conveyed by each branch

\[
\frac{I_{in(1)}}{I_{in(2)}} = \frac{L_2}{L_1}
\]

- The two branches remains synchronized
- CrM operation is kept (or FCCrM)
- No alteration of the 180 degree phase shift
Artificial Unbalancing

- In this test, the 150 µH inductor of branch 1 is replaced by a 300 µH coil !!!!
- Hence, more current is drawn by branch2 and MOSFET of branch2 is (normally) hotter
- The following plots show how the PFC stage behaves in these extreme conditions and full load
Still Operates in a Robust Manner…

120 Vrms, 0.8 A  
(PF = 0.997, THD = 6%)

230 Vrms, 0.8 A  
(PF = 0.980, THD = 11%)
Switching Frequency Variations in CrM

- The switching frequency varies versus the input power, the ac line amplitude and within the sinusoid
- $f_{sw}$ becomes high at light load, leading to large switching losses
- $f_{sw}$ should be limited
Limiting $f_{sw}$ to Optimize the Efficiency

- At the top of the sinusoid:
  \[
  f_{sw} = \frac{(V_{in,pk})^2}{4 \cdot L \cdot P_{in,avg}} \left(1 - \frac{V_{in,pk}}{V_{out}}\right)
  \]

- CrM operation requires large inductors to limit the switching losses at light load

- Can’t we clamp $f_{sw}$ not to over-dimension L?
  \rightarrow \text{Frequency Clamped Critical conduction Mode (FCCrM)}
Frequency Clamped Critical Conduction Mode

- At light load, the current cycle is short
- When shorter than the oscillator period, no new cycle until the oscillator period is elapsed ⇒ dead-times (DCM)
- On-times are increased to compensate the dead-times ⇒ **no PF degradation** (ON proprietary)
In FCCrM, the switching frequency is clamped:
- Fixed frequency in light load mode and near the line zero crossing
- Critical conduction mode (CrM) achieved at full load.

FCCrM optimizes the efficiency over the load range.
FCCrM reduces the range of frequencies to be filtered (EMI)
FCCrM allows the use of smaller inductors
  - No need for large inductances to limit the frequency range!
  - E.g., 150 µH (PQ2620) for a wide mains 300-W application

Frequency Foldback reduces the clamp frequency at light load to further improve the efficiency
NCP1631 Frequency Foldback

- The clamp frequency *linearly* decays when $P_{\text{in}}$ goes below a preset level ($P_{\text{LL}}$)

- $P_{\text{LL}}$ is programmed by the pin6 resistor

\[
\frac{(P_{\text{in}})_{FF}}{(P_{\text{in}})_{HL}} = \frac{R_{\text{pin6}} \cdot 105 \mu A}{1.66} \cong \frac{R_{\text{pin6}}}{15810}
\]

*(P_{\text{in}})_{HL}$ is the max. power deliverable by the PFC stage

Example: FF at 40% load and a 130 kHz nominal frequency

- Gradual decay of the clamp frequency
- *No discontinuity in the operation*
- A resistor across the oscillator capacitor sets a minimum clamp frequency (e.g., 20 kHz - see application note AND8407)

Pin 6 pins out a voltage proportional to the power. The $I_{\text{FF}}$ current is clamped to 105µA and used to charge and discharge the oscillator capacitor.
Light Load Operation

- Frequency is reduced at light load
  ➞ Heavy DCM operation to reduce the switching losses

- CrM at heavy load conditions

Input current (2 A / div)

Vaux1 (10 V/div)

Vaux2 (10 V/div)

Full load, 90 V
## No Load Consumption

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Line Voltage (V)</th>
<th>Input Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Frequency Foldback (pin6 grounded)</td>
<td>115</td>
<td>107</td>
</tr>
<tr>
<td>2 separate $V_{out}$ sensing networks for FB and OVP for a total 185-µA leakage on the $V_{out}$ rail</td>
<td>230</td>
<td>138</td>
</tr>
<tr>
<td>Frequency Foldback ($R_{FF} = 4.7 , k\Omega$)</td>
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<td>96</td>
</tr>
<tr>
<td>2 separate $V_{out}$ sensing networks for FB and OVP for a total 185-µA leakage on the $V_{out}$ rail (*)</td>
<td>230</td>
<td>134</td>
</tr>
<tr>
<td>Frequency Foldback ($R_{FF} = 4.7 , k\Omega$)</td>
<td>115</td>
<td>38</td>
</tr>
<tr>
<td>one $V_{out}$ sensing network for FB and OVP for a total 48-µA leakage on the $V_{out}$ rail</td>
<td>230</td>
<td>82</td>
</tr>
</tbody>
</table>

- Measured on the 300 W NCP1631 demoboard
- External $V_{cc}$, 3 * 680 kΩ resistors to discharge the X2 capacitors
- Frequency Foldback improves the efficiency in light load but also in no-load conditions

(*) Default demoboard configuration
NCP1631 Fault Management

- Brown-out
- Undervoltage protection
- Latch-off condition
- Die overtemperature
- Improper Vcc level for operation
- Too low current sourced by the Rt pin

In OFF mode, the major part of the circuit sleeps and consumption is minimized to < 500 µA
NCP1631 Over Current Protection

1) NCP1631 monitors a negative voltage, $V_{CS}$, proportional to the current drawn by both interleaved branches, $I_{in}$.

2) $I_{CS}$ current maintains 0 V on CS pin

$$-(R_{CS} \cdot I_{in}) + (R_{OCP} \cdot I_{CS}) = 0 \Rightarrow I_{CS} = \frac{R_{CS}}{R_{OCP}} \cdot I_{in}$$

3) If $I_{CS}$ exceeds 210uA, OCP is triggered

- Select $R_{CS}$ freely (optimally)
- $R_{OCP}$ sets the current limit
- Minimized losses in $R_{CS}$
NCP1631 Overcurrent Protection

When $I_{CS} > 210 \, \mu A$, the OCP switch closes and a current equal to $0.5*(I_{CS} - 210 \, \mu A)$ is injected into the negative input of the $V_{TON}$ processing opamp, the on-time sharply reduces proportionally to the magnitude of the over-current event.

- No discontinuity in the operation, out-of-phase operation is maintained
- No need for preventing OCP from tripping during a normal transient
- The current can be accurately limited
NCP1631 In-rush Current Detection

When plugged into the mains, the bulk capacitor is abruptly charged to the line voltage and the charge current (in-rush current) is huge. Drive turn-on during this time can damage the MOSFETs.

Disables output drive when signal is high ($I_{CS} > 14 \, \mu A$) (7% of $I_{LIMIT}$)

Circuitry to ground the In-rush protection once the circuit begins operation.
NCP1631 Over Voltage Protection

- Separate pins for FB and OVP (redundancy)
- The two functions share the same 2.5 V internal reference for an eased and accurate setting of the OVP level

Method 1: One feed-back network for OVP and FB

\[
\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}}
\]

Method 2: Two separate feed-back networks

\[
\frac{V_{out(ovp)}}{V_{out(nom)}} = \frac{R_{ovp1} + R_{ovp2}}{R_{out1} + R_{out2}} \cdot \frac{R_{out2}}{R_{ovp2}}
\]
Brown-out Protection with a 50 ms Blanking Time

- Mains interruptions shorter than 50 ms are ignored
- The blanking time helps meet hold-up time requirements
- The BO pin voltage serves for feedforward

For the blanking time, the BO pin voltage is maintained around the BO threshold not to delay the circuit restart when the line has recovered.

20-ms line interruption
NCP1631 PfcOK / REF5V Signal

- The pfcOK signal can be used to enable/disable the downstream converter.
- It is high (5 V) when the PFC stage is in normal operation and low otherwise.
- The pfcOK signal is low:
  - Any time the PFC is off because a major fault is detected (UVLO condition, thermal shutdown, UVP, Brown-out, Latch-off / shutdown, \( R_t \) pin open)
  - For the start-up phase of the PFC stage until the nominal bulk voltage is obtained
- The pfcOK pin can be used as a 5 V power source (5 mA capability)
A (simple but easy to use) Excel Spreadsheet (www.onsemi.com) computes the external components.
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NCP1631 Demoboard

Wide mains, 300 W, PFC pre-converter

NCP1631

MUR550
NCP1631 Demoboard Schematic

The circuit is latched off if $V_{cc}$ exceeds 17.5 V. Could be used for thermal protection

300 W, wide mains PFC pre-converter
As expected, the input current looks like a CCM one.
At high line, frequency foldback influences the ripple.
Zoom of the Precedent Plots

- These plots were obtained at the sinusoid top
- The current swings at twice the frequency of each phase
- At low and high line, the phase shift is substantially 180°
Refueling Sequences

- CrM at low line with valley switching
- Fixed frequency operation at high line (frequency clamp)
- Out-of-phase operation in both cases

![Graphs showing refueling sequences with different line voltages and measured parameters such as $I_{L(tot)}$, $V_{ZCD1}$, and $V_{ZCD2}$.]
Efficiency Measurements

- The output voltage is generally 390 V
- For a 300 W application, the output current is:
  - 770 mA at full load
  - 154 mA at 20% of the load
- Both currents are generally measured with the same tool
- If @ 20% of the load, the input power is 63 W
- 1-mA error in $I_{\text{out}}$ leads to
  - $I_{\text{out}} = 153 \text{ mA} \Rightarrow \text{Eff} = 100 \times 390 \times 0.153 / 63 = 94.7 \%$
  - $I_{\text{out}} = 155 \text{ mA} \Rightarrow \text{Eff} = 100 \times 390 \times 0.155 / 63 = 95.9 \%$
- A 1-mA error causes a 1.2% difference in the efficiency!
- Measurements @ 10% and 20% of the load need care!!!
Efficiency Measurements

- The efficiency does not only depend on the control mode.
- The inductor, the MOSFETs, diodes, EMI filter... play a role.
- For instance, if we compare the efficiency with a 200 µH PQ2625 inductor to that with a 150 µH PQ2620 one:

![Efficiency graph at 230 V](image)

Frequency Foldback limits the difference at light load.
In the 20% to 100% range, the efficiency remains:
- > 95.8% at low line
- > 97.0% at high line

Refer to NCP1631EVB/D at [www.onsemi.com](http://www.onsemi.com) for details.
Tweaking Frequency Foldback …

- A resistor can be added between the pfcOK (5 V) and frequency foldback pins.
- Doing so, the frequency clamp decays more sharply:

\[
V_{\text{REGUL}} = \frac{R_2 \cdot 5V}{R_1 + R_2}
\]

(V\_\text{REGUL} is proportional to the PFC power)
A resistor on the oscillator pin sets the minimum frequency
With $R_1$, the PFC stage operates at the minimum frequency (20 kHz) at 10% and 20% of the load
The tweak further improves the light load efficiency
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Conclusion

- Interleaved PFC allows use of smaller components, improves thermal performance, increases the CrM power range and reduces current ripple.

- The NCP1631 provides a single IC solution which incorporates all the features necessary for building a robust and compact 2-phase interleaved PFC stage with minimal external components.

- Its FCCrM and frequency foldback allows an efficient operation over the load range with small inductors.
For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies