Achieving High Power Density Designs in DC-DC Converters

Agenda

- Marketing / Product Requirement
- Design Decision Making
  - Translating Requirements to Specifications
  - Passive Losses
  - Active Losses
- Layout / Thermal PCB Guidelines
- Reference Designs

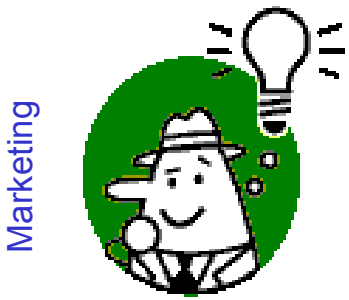
Marketing / Product Requirement

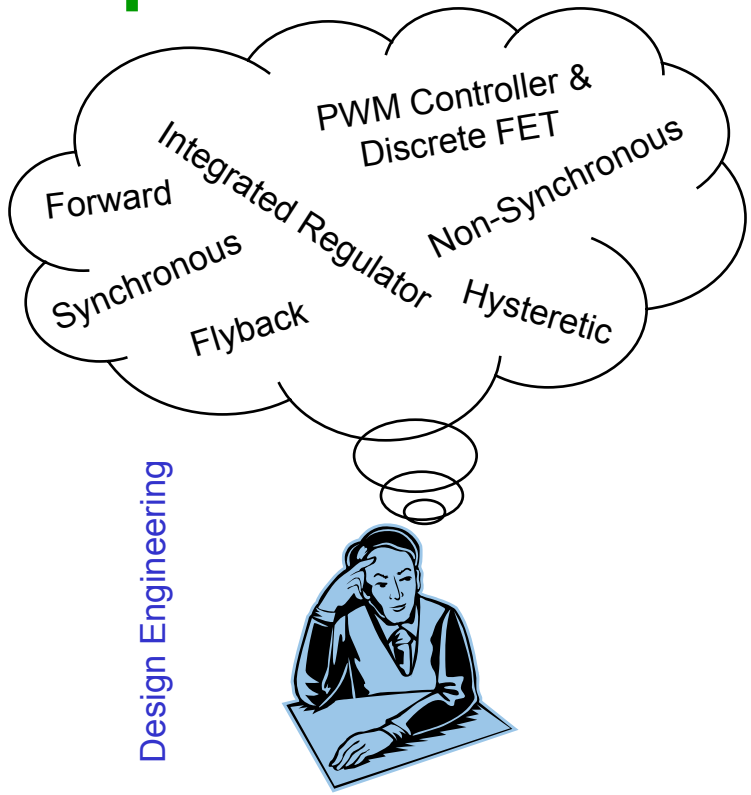
77 mm

Area Required For World's Greatest Idea

51 mm

Input: +12 V
Output: 3.3 V @ 10 A
Size: 77 x 51 mm
Height: 21 mm
Ripple: <30 mV
Thermal: <72 °C case
Transient: ~2.5 A/us
Cost: Low





Does this sound familiar?

Marketing has come up with a new product idea, but it requires more power and less space than the previous designs.

There are so many choices for a solution. Which one do you select?

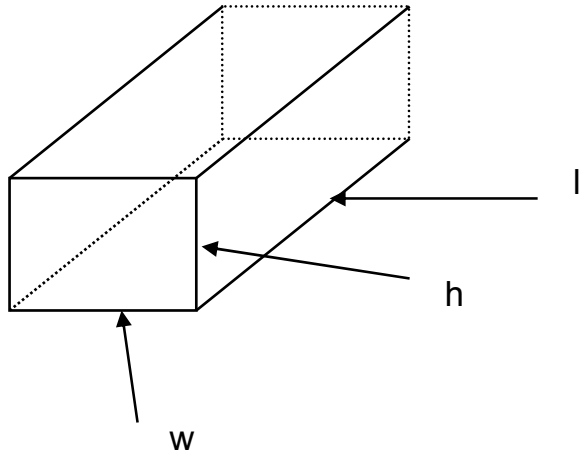
Reviewing potential options

In order to meet the high power density design requirement, you must first understand the efficiency losses in your system and make some design decisions.

Black box thermal analysis

$$\Delta T = T_{surf} - T_{amb}$$

In Kelvin or Celsius



Heat Convection can be calculated for a a 5 sided box

$$P_d^{conv} = 10^{-3} \times \left[4.6(l+w)h^{0.75} + 1.8(l \times w)^{0.75} \times (l+w)^{0.25}\right] \times \Delta T^{1.25}$$

The surface radiated heat transfer can be calculated using Boltzman's law

$$P_d^{rad} = 3.66 \times 10^{-11} \times f \times e \times A\left[T_{surf}{}^4 - T_{amb}{}^4\right]$$

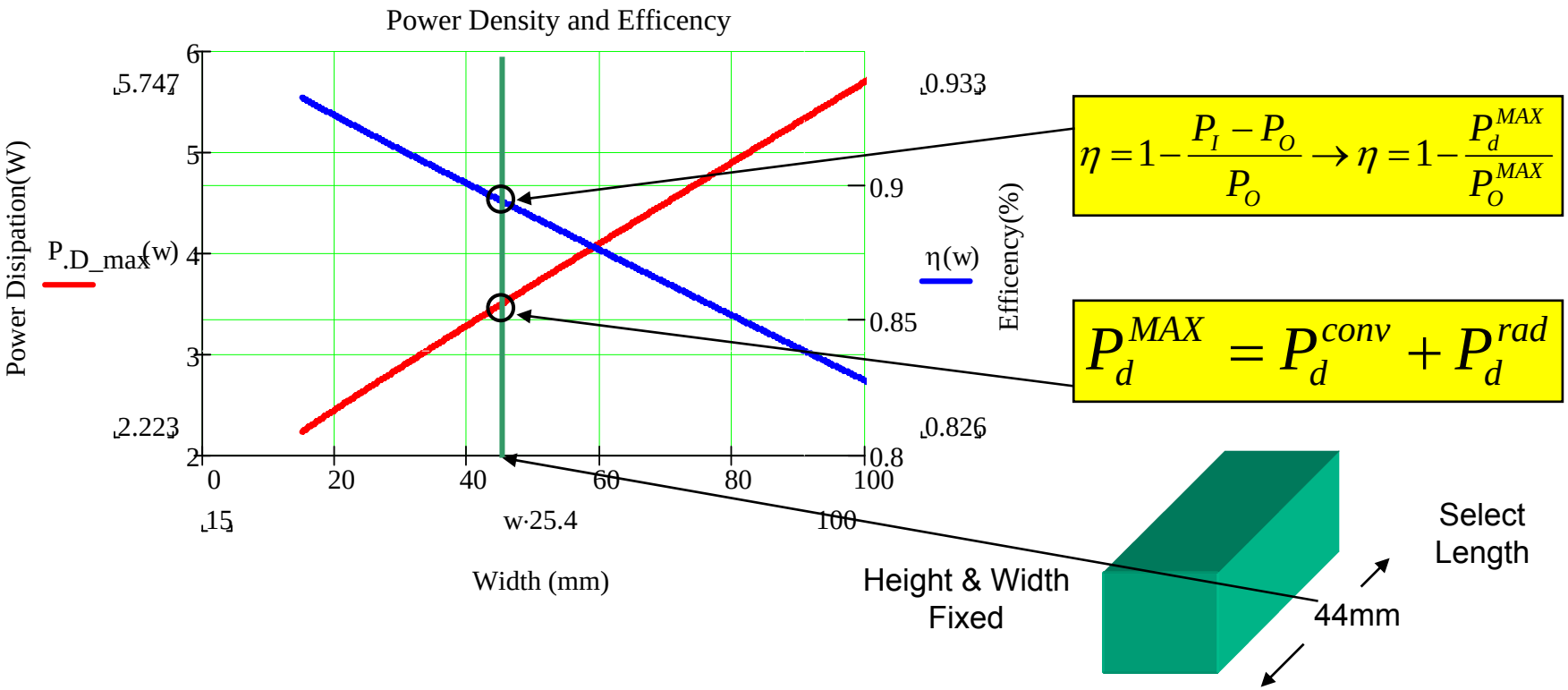
Surface area in square inches

Emissivity = .9

View factor = .5

General system thermal analysis

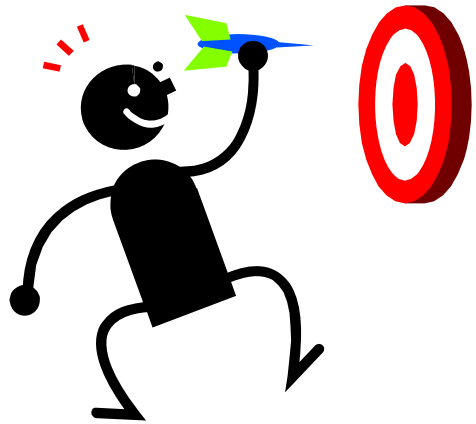
If the height and width are fixed at 20.5 mm and 77 mm respectively then the length can be selected from the graph.

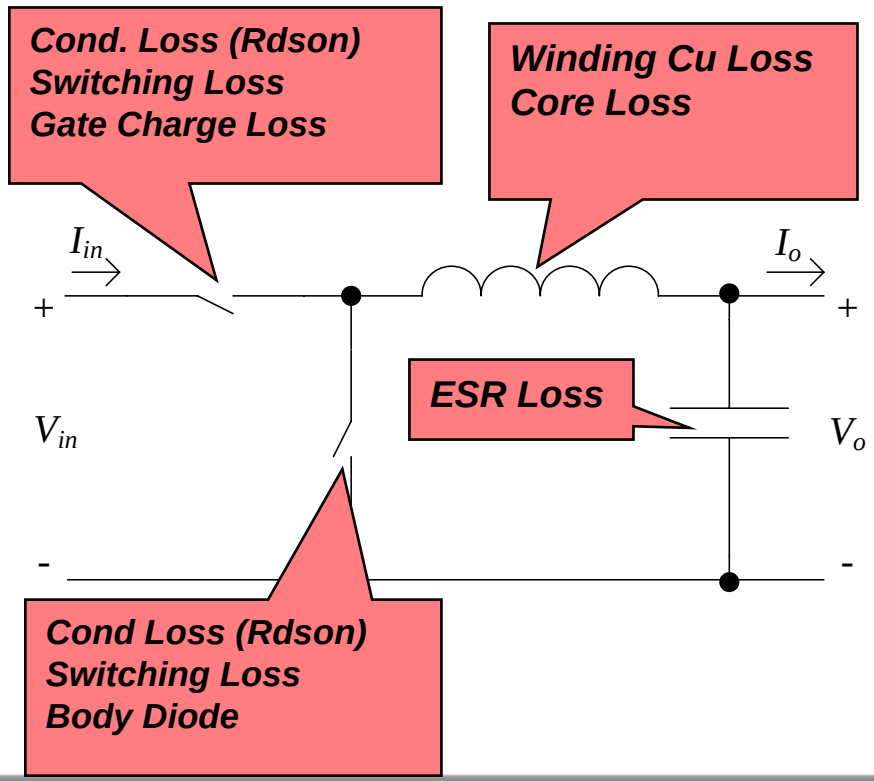


A length of 77 mm indicates that the system efficiency must be a minimum of of **88.7** %, allowing **3.72** W of dissipation.

Efficiency target

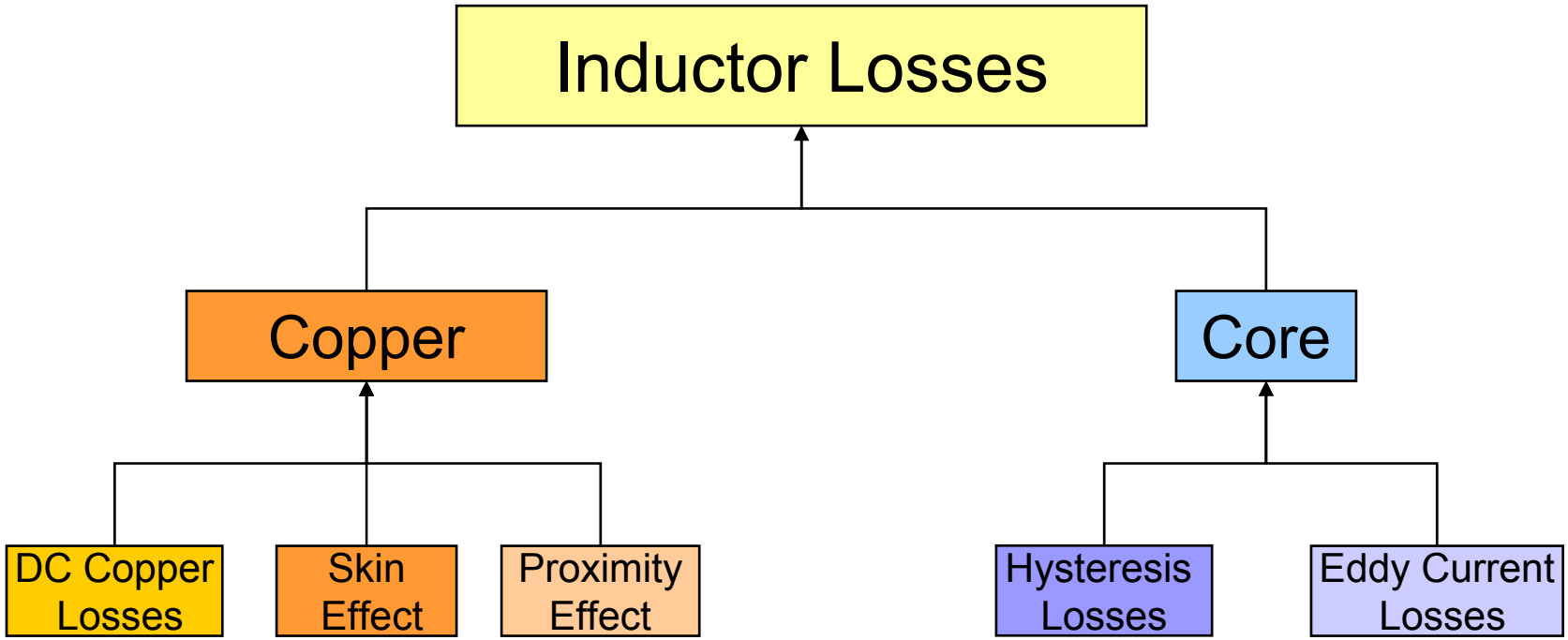
Loss contributions of the system will be tracked using a target table



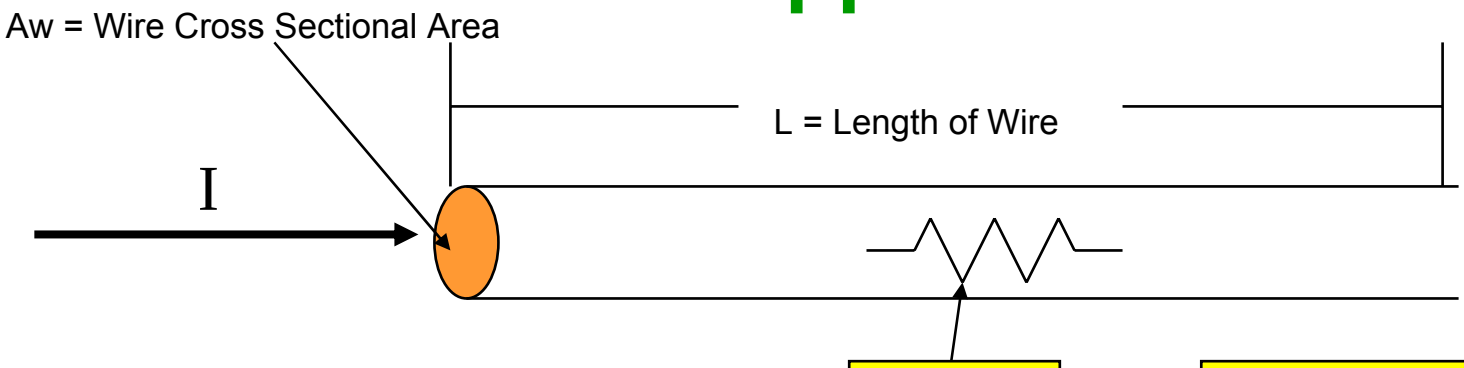


Passive Losses	Est. (W)	
Inductance		0%
Input / Output Cap		0%
Traces		0%
Active Losses		
MOSFETs		0%
Diodes		0%
Target	3.72	0%

Inductor losses in switch mode power supplies



DC copper losses



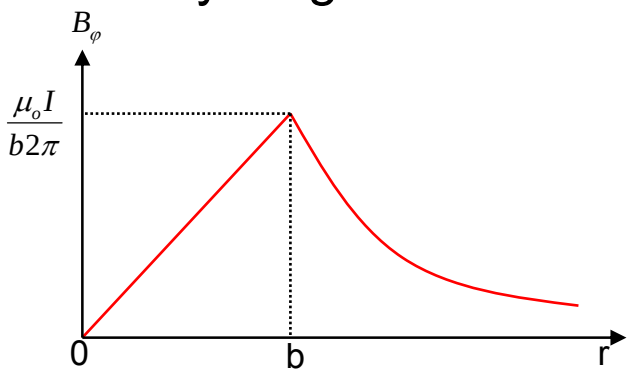
ρ = Resitivity of Wire

(copper = 2.3X10^{-6} Ωcm)

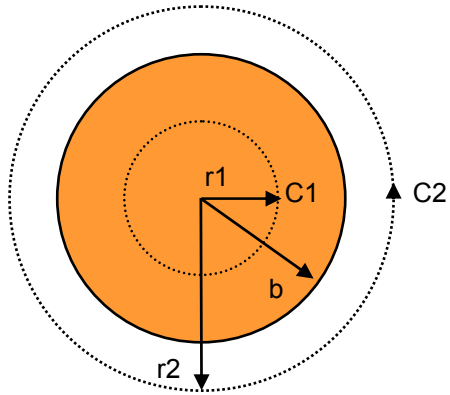
$$R = \frac{\rho \times L}{Aw}$$

$$P_{DC} = I_{DC}^{\ 2} \times R_{DC}$$

- If a current is flowing in a conductor then Ampere's Law can be used to calculate the flux density both inside and outside a conductor for an infinitely long wire



$$\oint_C B \bullet bl = \mu_o I$$



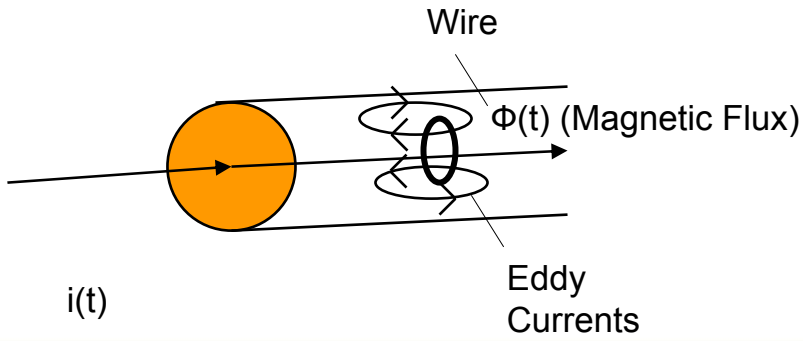
Eddy currents

- Since the current flowing inside the conductor is not dc, the effects to current flow must be considered
- Lenz's law indicates:

$$\mathcal{E} = -N\frac{d\Phi_B}{dt}$$

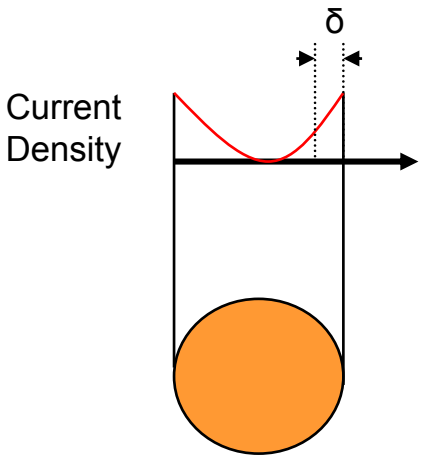
Electromotive Force (EMF) in Volts
Magnetic Flux in Webers where Φ_B = B*Area
Change in Time
Number of Turns

- If the ac current produces a changing B field and that in turn produces a voltage in a conductive medium, then by ohms law a current must flow
- The diagram below shows that eddy currents decrease the current flow at the center of a conductor



Skin effect

- Eddy current produced by the ac current adds to the outer conductor current and subtracts from the inner current
- When frequency increases, the majority of the current flows on the surface
- The wave attenuation factor can be expressed as $e^{-\alpha z}$, where skin depth is the point where $e^{-1} = 0.368$ or 63.2 % of the wave flows:



ρ = Resistivity of a Wire

ρ_{CU} = 2.3X10-6 Ωcm

Permeability of Free Space

$4\pi x10^{-7}\ N \cdot A^{-2}$

$$\delta = \sqrt{\frac{\rho}{\pi \times \mu \times f}}$$

Frequency

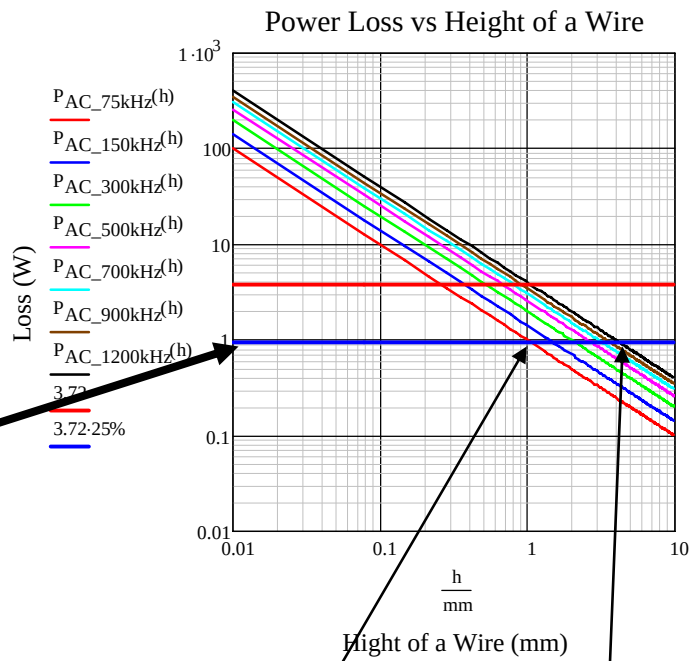
$$.129mm = \sqrt{\frac{2.3X10^{-6}\Omega * cm}{\pi \times 4 \times \pi \times 10^{-7} \times N \times A^{-2} \times 350 * kHz}}$$

Skin effect

- The DC resistance calculated earlier will now have to be modified to account for AC currents

$$R_{AC} = \frac{h}{\delta} \times R_{DC}$$

With a Wire Length of 12 cm



Target 25% of Total Losses

Select Frequency based on targeted power loss *(50 – 350 kHz)*

- Power loss increases at higher frequency because of increasing AC resistance

$$P_{1Layer} = I_{L,RMS}^2 \times R_{AC}$$

Proximity effect

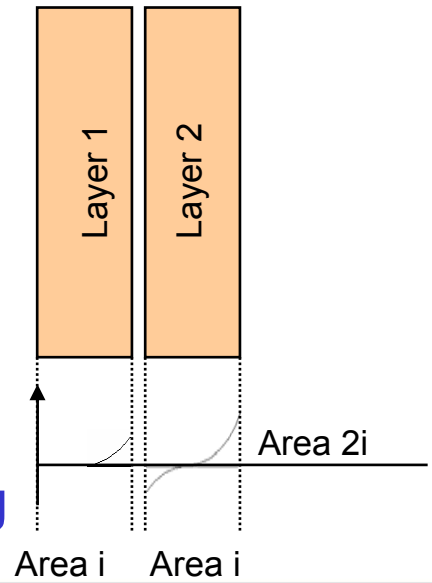
- When two conductors, thicker than δ, are in proximity and carry opposing currents, the high frequency current components spread across the surfaces facing each other in order to minimize magnetic field energy transfer
- Thus an equal and opposite current is induced on the adjacent conductor

$$P_{Layer\,2} = \left(2 \times I_{L,RMS}\right)^2 \times R_{AC\_Layer\,2} \rightarrow 4P_{Layer1}$$

Second Layer has 4X the loss of the First !!

$$P_{winding} = \left[I_{L,RMS}^2 \times \frac{h}{\delta} \times R_{DC} \right] + 4\left[I_{L,RMS}^2 \times \frac{h}{\delta} \times R_{DC} \right] + \ldots\ldots$$

Goal: Minimize the number of # of Layers in the Winding



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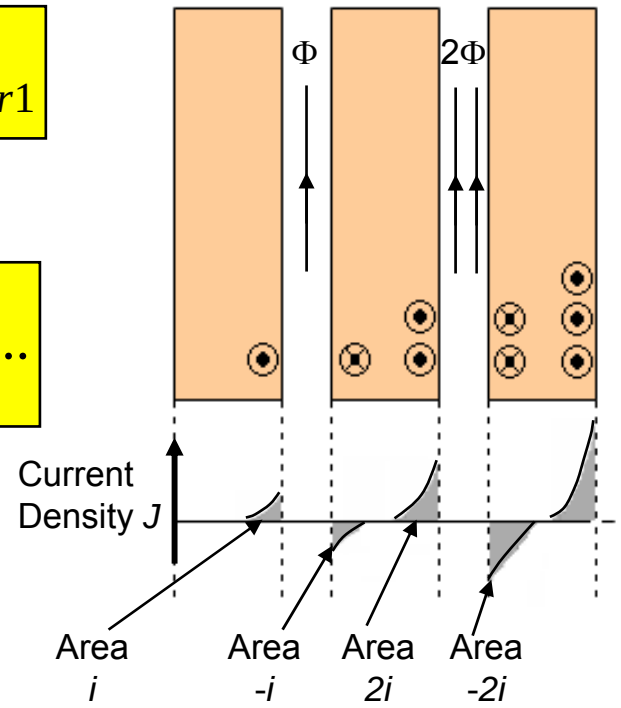
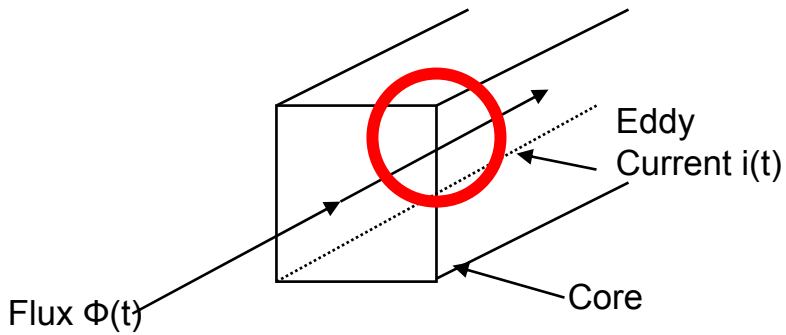


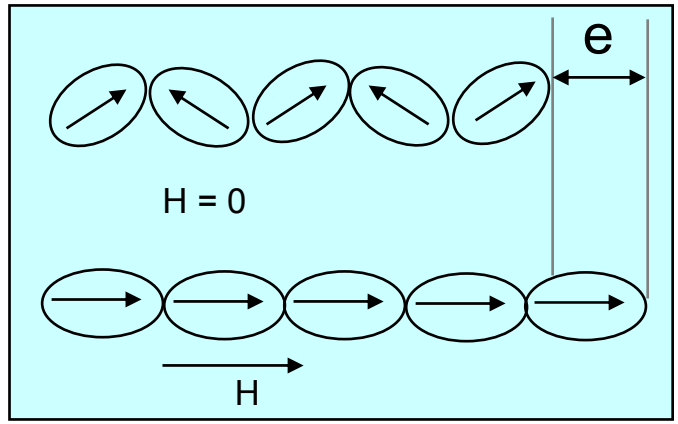
Magnetic eddy current losses

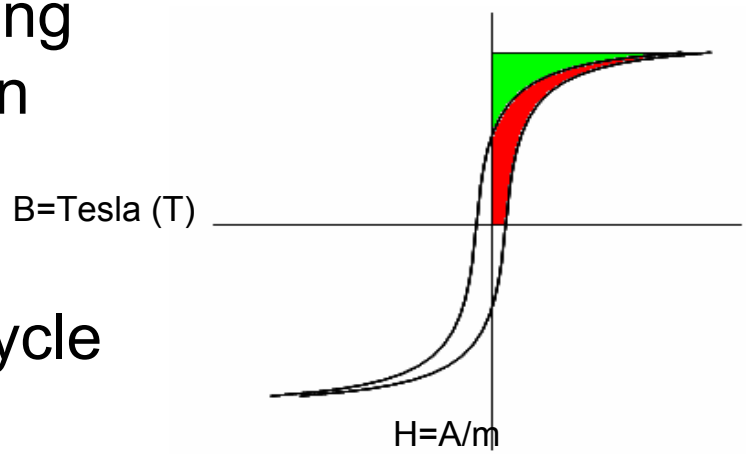
- Magnetic eddy current losses are similar to the losses experienced in copper
- Instead of having current moving inside of a copper conductor, a field is moving within a core material
- The faster the field moves in the material, the greater the magnetic eddy current losses
- Magnetic eddy current can be decreased by increasing the resistivity of the magnetic material



Hysteresis losses

- Hysteresis losses are caused from friction between magnetic domains as they align to the applied fields
- The larger the area of the hysteresis loop, the more loss per cycle. Hysteresis loss gets worse at lower frequencies
- The red indicates power lost during one switching cycle due to friction between magnetic domains
- The green indicates power delivered during one switching cycle





Core losses

- The hysteresis and magnetic eddy current losses are grouped into one general volumetric loss equation not calculated directly

- Manufacturer provide a loss curves of tested data at various frequencies
- Manufacturers may also provide loss coefficients a, c and d are found by curve fitting the charted data.

Frequency

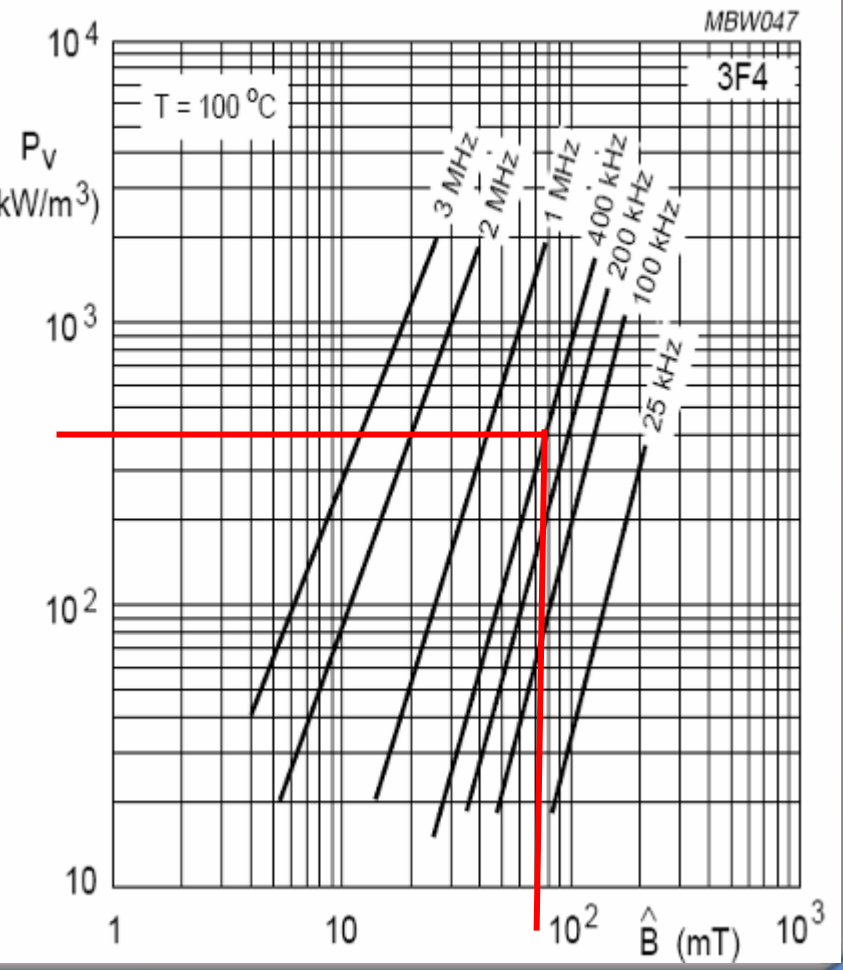
Change in Flux

$$P = a \times f^{c} \times (\Delta B)^{d}$$

kW/m^3 or 10^{-3} W/cm^3

From a Curve Fit

- The loss per unit volume is dependent on the material selected, frequency and temperature.

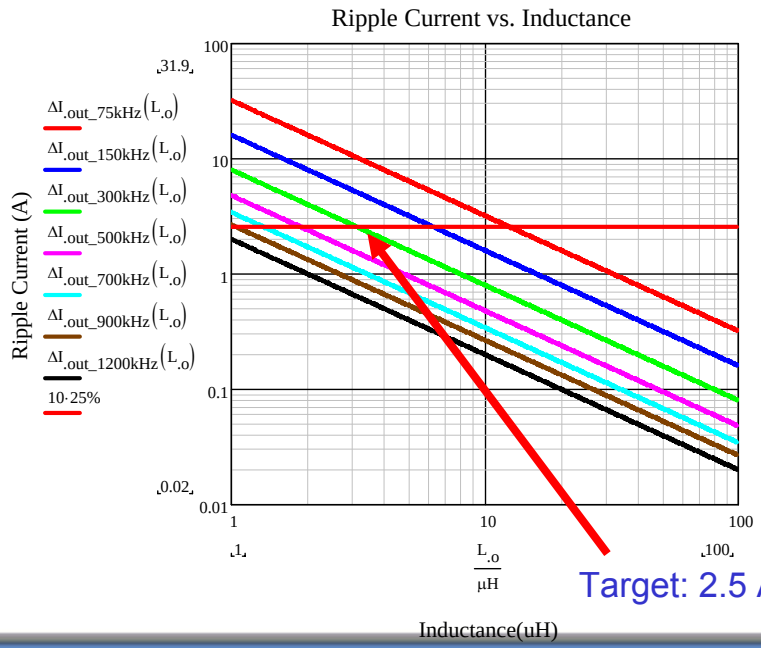


Choosing core materials

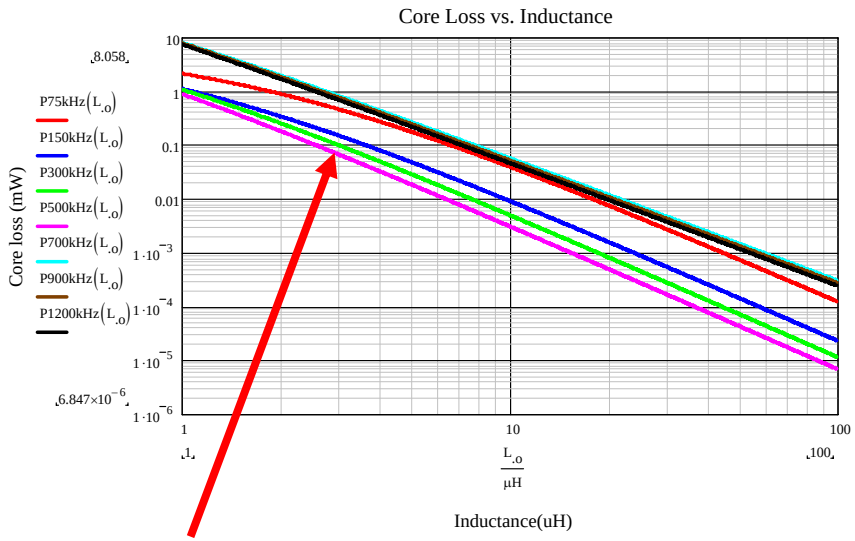
	Advantage	Disadvantage
Ferrite- MnZn	Low core loss, High perm, High frequency up to MHz	Fast roll off, Low B sat, Temp stability, gap losses
Ferrite- NiZn	Low conductivity, Wind on core, High frequency up to 300 MHz	Higher core losses than MnZn, Low B sat, Low permeability
Powder Iron	Low cost	High core losses, Low frequency, Possible aging issues
Permalloy	Good DC bias, Low core loss	High cost, Excellent temperature stability
High Flux	Best DC bias, High B sat, Low core losses	Average cost

Ripple current inductance and core loss

- Ampere's law, Faraday's Law, and core characteristics are the only tools needed to choose a proper core
- Inductor ripple current at full load is characterized by $\Delta I_{LO} = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L_O \times F_{SW}}$
- Using the loss equation for Magnetics INC R type material with a standard drum core with a volume of 1.73 cm^3
- The change in B can be calculated by $\Delta B_{MAX} = B_{MAX} \frac{\Delta I_{pp}}{I_{SCpk}}$



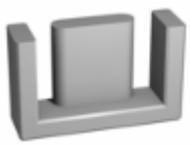
Target: 2.5 A p-p MAX



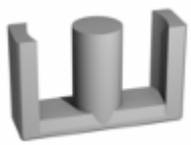
Target: 3.3 uH

Core technology choices

Classical *E*



EFD



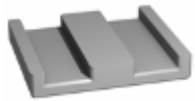
ER

EP

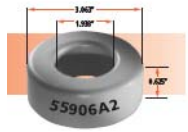
Pot core of 'RM' type

U-shaped

C-shaped



Planar 'E'



Toroid

Unshielded drum

Shielded drum

Shielded toroid

Axial lead

1. Surface Mount
2. Inexpensive
3. Time Constraints
4. Size Requirement
5. NO EMI Requirement

Leaded toroid

Vertical mount

Power wafer

Integrated inductor

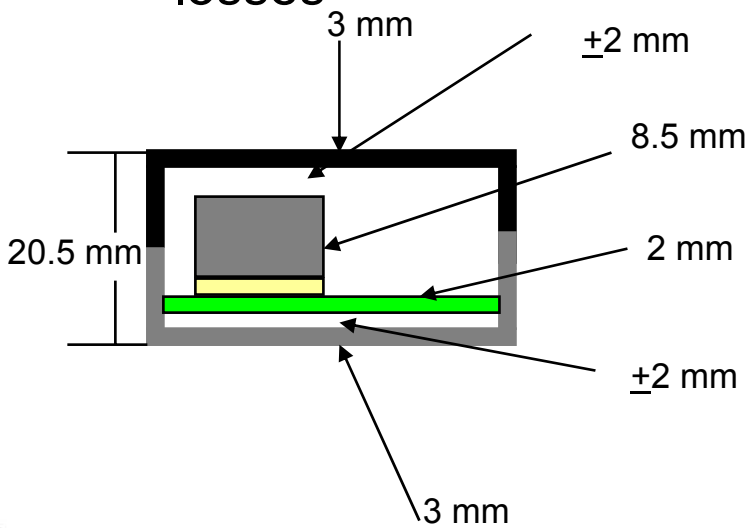
Gapped ferrite bead

Off the shelf solutions

- The inductors shown meet the size and electrical requirements at 350 kHz
- Inductor 1 was chosen as it has lower temperature rise and losses

Results *(estimated)* Coilcraft

	Inductor 1	Inductor 2	Inductor 3
	DO5010H-332	DO5022P-332	DO3316H-332
Total inductor loss	888.68 mW	1846.39 mW	1451.81 mW
Inductor core loss	0.10 mW	0.10 mW	12.75 mW
DCR loss	860.00 mW	1800.00 mW	1400.00 mW
AC winding loss	28.58 mW	46.29 mW	39.06 mW
Temperature rise	40.73 °C	105.04 °C	117.46 °C



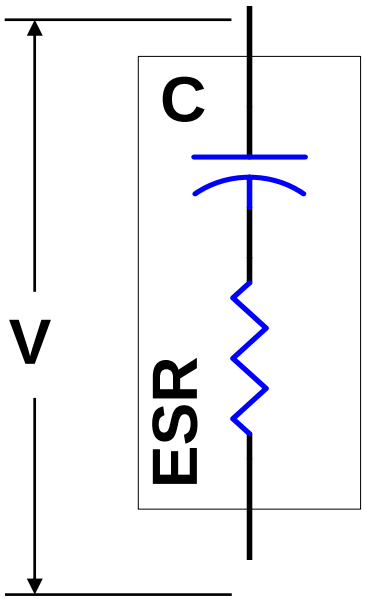
Passive Losses	Est. (W)	
Inductance	0.889	24%
Input / Output Cap		0%
Traces		0%

Active Losses		
MOSFETs		0%
Diodes		0%

Target	3.72	24%

Input / output capacitor selection

ESR = Equivalent Series Resistance

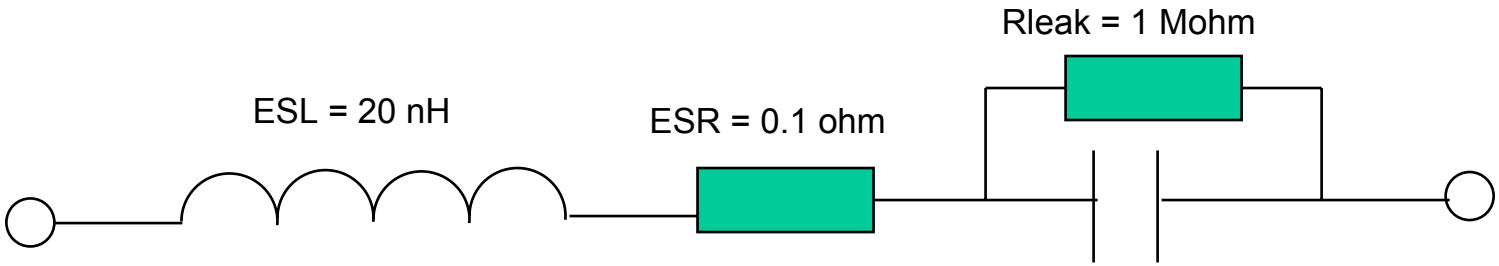


Typical ESR

	Electrolytic	Tantalum	Ceramic
100 nF	N/A	N/A	10 mΩ
1 µF	1 Ω	2 Ω	20 mΩ
10 µF	50 mΩ	3 Ω	35 mΩ
100 µF	50 mΩ	1 Ω	45 mΩ

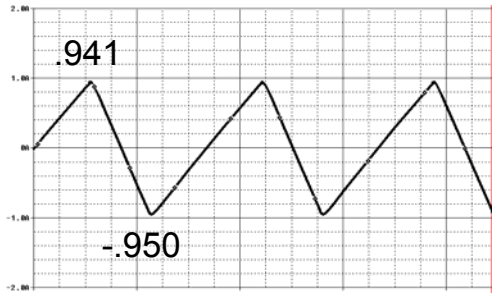
Realistic Capacitor Value on the PCB

Capacitor electrical model



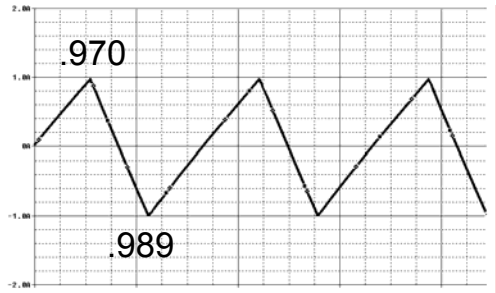
$$\Delta V_{OUT} = \left(ESR_{OUT} \times \Delta I_{OUT} + ESL \times \frac{d_i}{d_t} \right)$$

Full Model

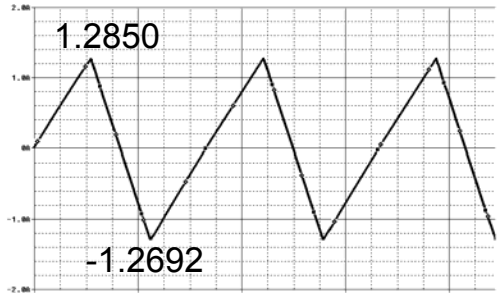


Ripple Current (A)

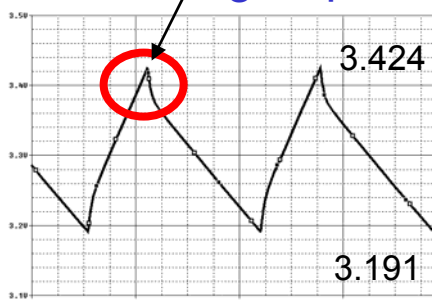
Removing the Inductor



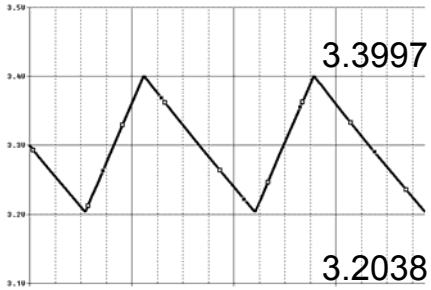
Removing the Inductor and ESR

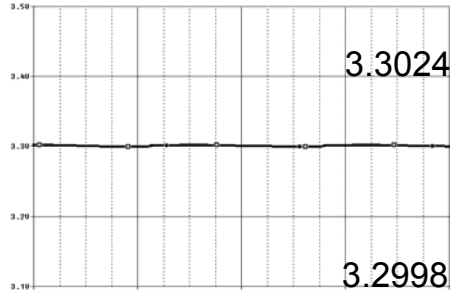


Voltage Spike from Inductance



Ripple Voltage (V)





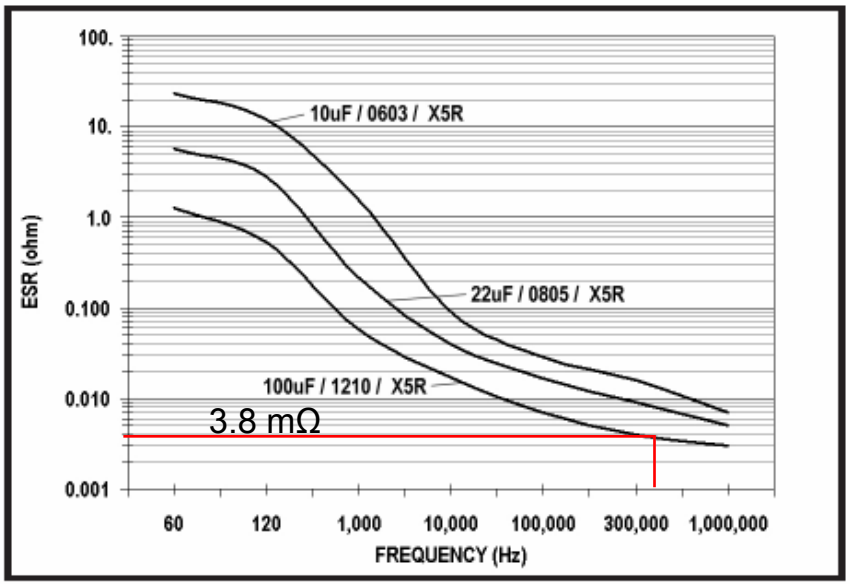
Ripple voltage

- Ripple voltage can be simplified by eliminating package inductance

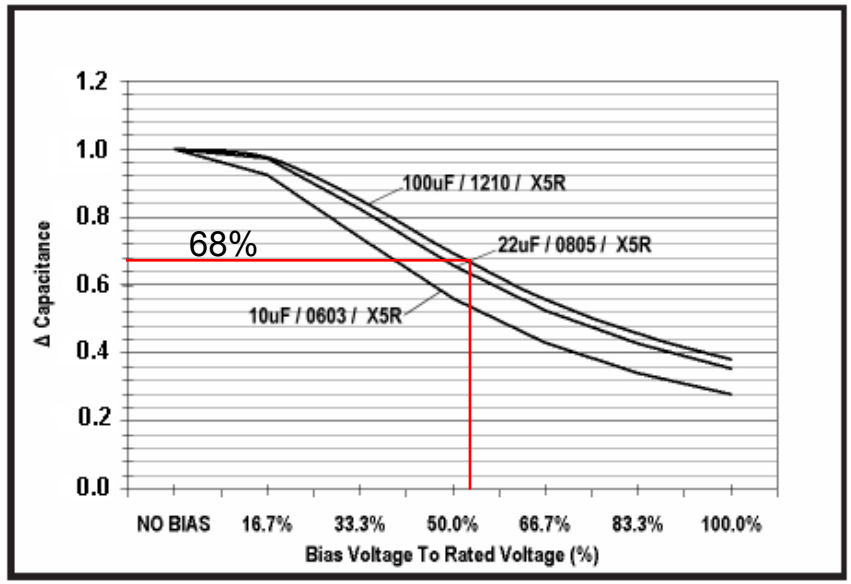
$$\Delta Vout = ESR \times \Delta I_{OUT} \rightarrow \frac{\Delta Vout}{\Delta I_{OUT}} = ESR \rightarrow \frac{30mV}{2.41A} = 12m\Omega$$

- The low ESR requirement will prompt the use of ceramic capacitors
- The designer must be aware of the derating over voltage and frequency when using ceramic capacitors

Typical ESR versus Frequency



Typical Capacitance versus Bias Voltage



Losses

- Input Capacitor Losses

4 x 47 uF Capacitors

$$P_{Cin} = \left[\frac{I_{OUT}}{2}\right]^2 \times ESR_{IN} \rightarrow \left[\frac{10A}{2}\right]^2 \times .714m\Omega = 17.8mW$$

- Output Capacitor Losses

4 x 100 uF Capacitors

$$P_{Cin} = [\Delta I_{OUT}]^2 \times ESR_{OUT} \rightarrow [2.41]^2 \times .95m\Omega = 5.5mW$$

Passive Losses	Est. (W)	
Inductance	0.889	24%
Input / Output Cap	0.023	1%
Traces		0%
Active Losses		
MOSFETs		0%
Diodes		0%
Target	3.72	25%

Power loss in PCB traces

Copper Area Required for Temperature Rise

$$C_{Area} = (I_{OUT}/(0.0647*(\Delta T)\text{^}0.4281))\text{^}(1/0.6732)$$

Output Current

ΔT= Surface Temperature – Ambient Temperature

Required Trace Width for Temperature Rise

$$W_{REQ} = C_{AREA}/(C_{thick}*1.378)$$

Copper Thickness in oz per square feet

Resistance of a Trace

$$R_{Trace} = Con_{length}*(0.6255 + 0.00267*(T_{amb} + \Delta T))/C_{AREA}$$

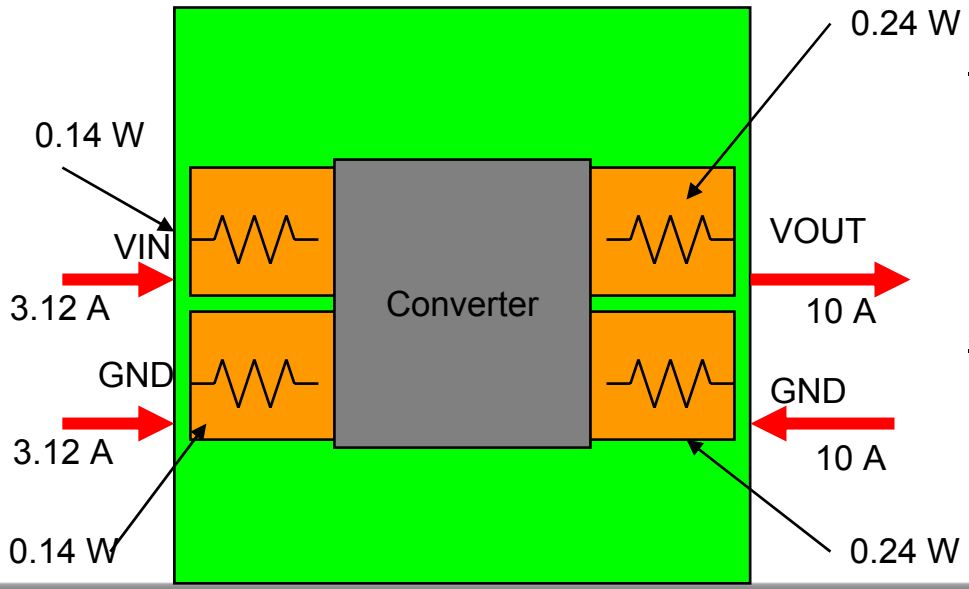
Length of the trace

Power Dissipation of a Trace

$$P_{Trace} = I_{OUT}^{\ 2} \times R_{TRACE}$$

Trace resistance

- The dimensions required from the surface temperature calculation combined with the fact that power must be carried from one end of the PCB to the other, gives the diagram shown
- ½ of the design is input ½ of the design is output
- The design uses a 10 °C rise with an ambient of 25 °C
- Other components contribute to the final temperature of the traces

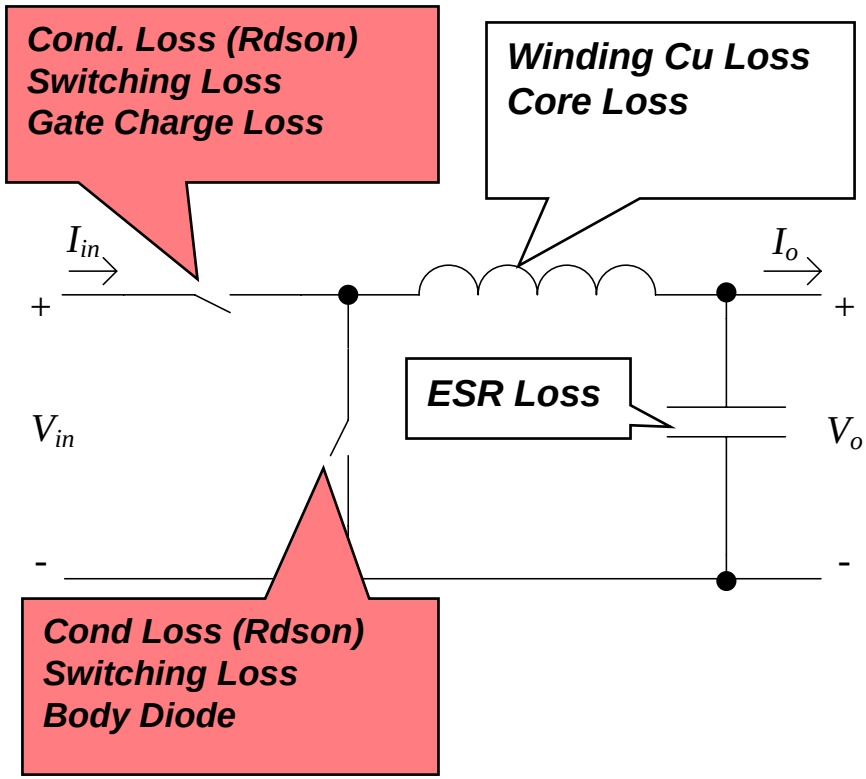


Passive Losses	Est. (W)	
Inductance	0.889	24%
Input / Output Cap	0.023	1%
Traces	0.76	20%

Active Losses		
MOSFETs		0%
Diodes		0%

Target:	3.72	45%

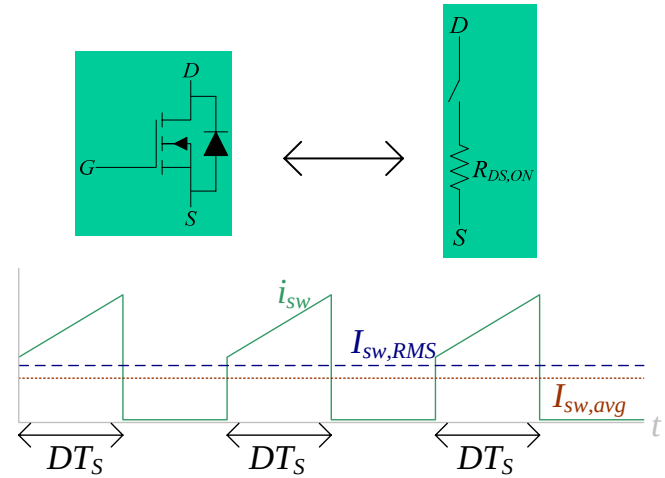
Review of the active losses



Conduction losses

MOSFET Conduction Loss

- MOSFET are selected based on peak current & voltage.
- Conduction loss calculated as shown in figure
- A range of MOSFETs with different R_{dson} can be selected.



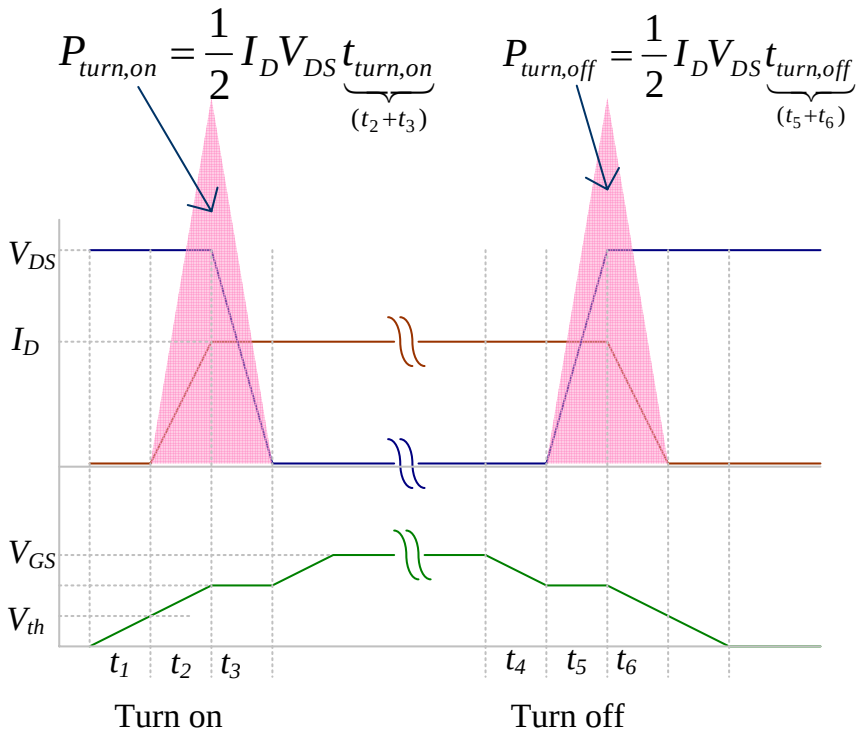
$$P_{sw,cond} = I_{sw,RMS}^2 \times R_{DS,ON} \approx DI_o^2 R_{DS,ON}$$

Switching losses

Switching Losses: High Side Switch

- During turn on (t_2+t_3) and turn off (t_5+t_6) both I_D and V_{DS} are non-zero
- This results in significant power loss during switching transitions

$$P_{switching} = \frac{1}{2} I_{DS} V_{DS} \underbrace{(t_{turn,on} + t_{turn,off})}_{switch-transition-time} \cdot f_{sw}$$



- Switching Losses are dominant loss components at higher switching frequencies
- MOSFET datasheet provides information for estimation of switching losses.

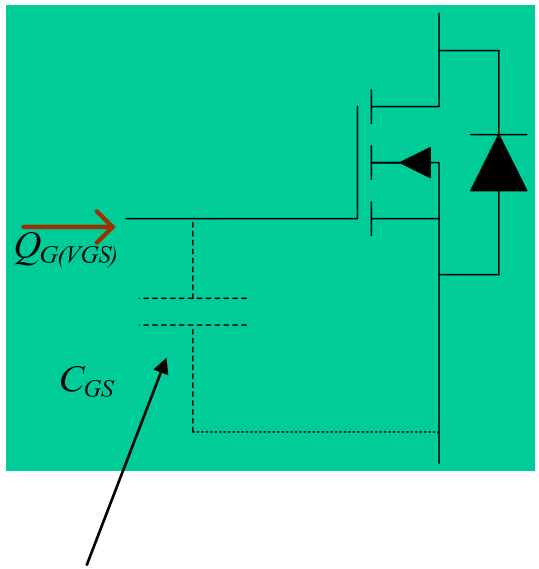
Gate charge losses

•There is a power loss associated with the gate charge supplied at turn on. This power loss can be calculated as

$$P_{sw,GATE} = Q_{G(V_{GS})} V_{GS} f_s$$

•$Q_{G(VGS)}$ can be found from the gate charge curve in Power MOSFET datasheets

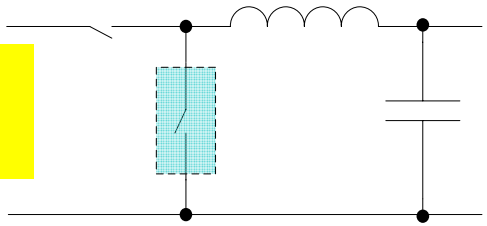
•Gate Charge Losses can be appreciable at very high switching frequency



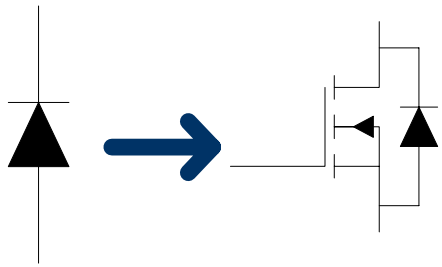
Parasitic Capacitance

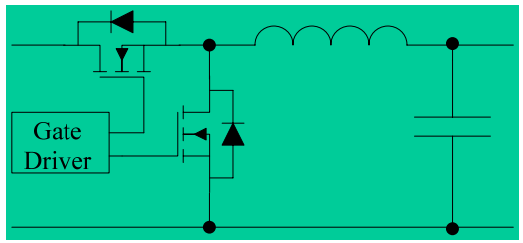
Synchronous rectifier

*At V_{in}=12 V, Vo=3.3 V, Losses in Diode (V_F= 0.6 V) alone will cause a **15%** drop in efficiency!*



- In *Synchronous Rectifier* Diode is replaced by a MOSFET
- Low RDSON of MOSFET allows higher efficiency
- Introduces extra gate drive



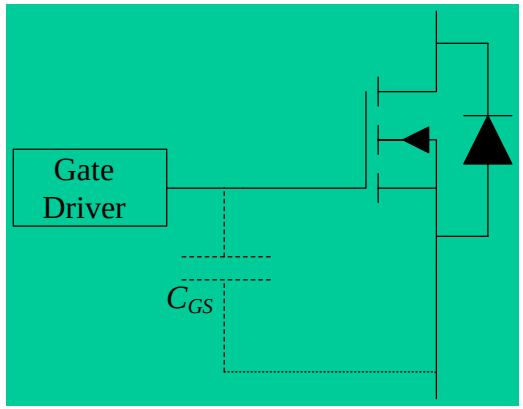


Synchronous rectifier

•Synchronous Rectifier introduces additional gate drive circuit

•*Gate Charge Loss* of synchronous rectifier should be taken into account while estimating efficiency gain

•The gate can be driven by a low voltage supply to reduce gate charge losses

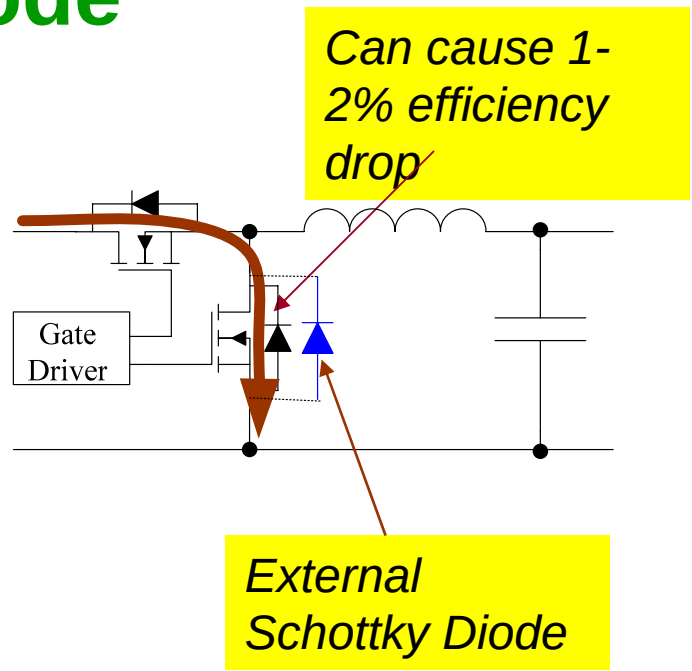


$$P_{sw,GATE} = Q_{G(V_{GS})} V_{GS} f_s$$

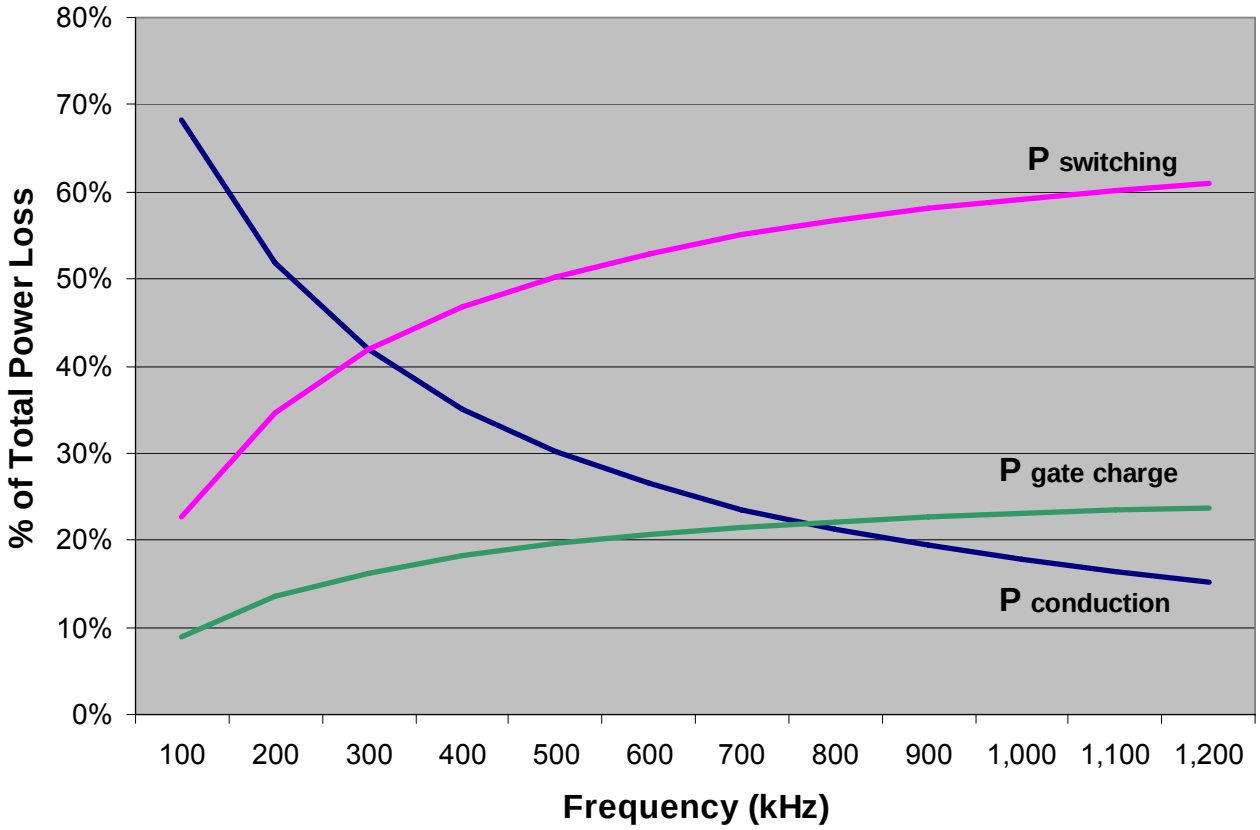
•Low gate drive voltage results in higher R_{dson} from being only partially turned on resulting in higher conduction loss

Body diode

- Non-overlap/Dead Time to avoid cross conduction
- Body diode of synchronous switch conducts during dead time.
- Body diode is lossy and is slow to turn on/off
- A Schottky diode is used in parallel with synchronous rectifier MOSFET
- Non-overlap time conduction can be significant at high switching frequencies

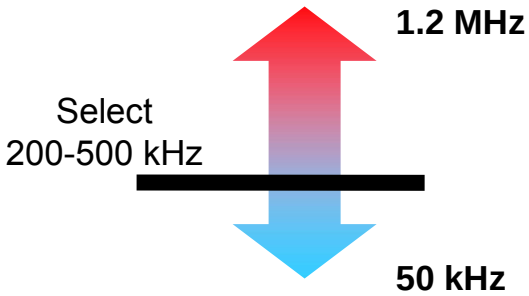


Frequency selection



High Power Density/Small Size

High Frequency Design



High Efficiency

Low Frequency to Limit Switching Losses

Summary

- In order to design high power density products it's important to understand the passive and active losses in the system
- PCB layout plays a key part in achieving the desired performance
- ON Semiconductor offers several products to meet your high power density design needs
  - Complete System: Regulators, Controllers, FETs, Diodes