Standby Power Reduction Techniques
Agenda

• Regulatory requirements
• Sources for standby power losses
• Methods to lower the standby power consumption
• Measured results versus calculated results
• Conclusion
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Regulatory challenges

- Standby Power Reduction
  - 25% of total energy consumption is in low power/sleep/standby mode
  - Concerted effort by CECP, Energy Star, IEA and other international agencies to limit standby power

- Active Mode Efficiency Improvement
  - 75% of total energy consumption is in active mode
  - Changing efficiency from 60% to 75% can result in 15% energy savings
  - Next focus area for agencies

- Power Factor Correction (or Harmonic Reduction)
  - Applicable with IEC 1000-3-2 (Europe, Japan)
  - Some efficiency specifications also require >0.9 PF
Standby certification programs
(external power supplies)

<table>
<thead>
<tr>
<th>Code</th>
<th>Region/Country &amp; Timing</th>
<th>No Load Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>CUC1</td>
<td>CECP (China) &amp; Energy Star (US) From January, 2005 (Tier 1)</td>
<td>≤ 0.50 W for 0-&lt;10 W ≤ 0.75 W for ≥10-250 W</td>
</tr>
<tr>
<td>CUC2</td>
<td>CECP and Energy Star From July 1, 2006 (Tier 2)</td>
<td>≤ 0.30 W for 0-&lt;10 W ≤ 0.50 W for ≥10-250 W</td>
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<td>CE1</td>
<td>Europe (EC Code of Conduct) From January 1, 2005</td>
<td>≤ 0.30 W for &lt;15 W ≤ 0.50 W for 15-50 W ≤ 0.75 W for 50-60 W ≤ 1.00 W for 60-150 W</td>
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<tr>
<td>CE2</td>
<td>Europe (EC Code of Conduct) From January 1, 2007</td>
<td>≤ 0.30 W for non-PFC ≤ 0.50 W for PFC</td>
</tr>
<tr>
<td>CA1</td>
<td>Australia (High Efficiency) From April, 2006</td>
<td>≤ 0.50 W For 0-180 W</td>
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# Standby mandatory programs

<table>
<thead>
<tr>
<th>Code</th>
<th>Region/Country &amp; Timing</th>
<th>No Load Power Consumption</th>
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</thead>
<tbody>
<tr>
<td>MU0</td>
<td>US – FEMP DOE (Final 2011)</td>
<td>≤ 1.00 W for most applications</td>
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<tr>
<td>MC1</td>
<td>China GB (Guo Biao) Standards (From January, 2005)</td>
<td>≤ 0.75 W for 0-10 W &lt;br&gt;≤ 1.00 W for 10-250 W</td>
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<tr>
<td>MC2</td>
<td>China GB (Guo Biao) Standards (From October, 2007)</td>
<td>≤ 0.50 W for 0-10 W &lt;br&gt;≤ 0.75 W for 10-250 W</td>
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<tr>
<td>MA1</td>
<td>Australia (MEPS) From April, 2006</td>
<td>≤ 0.75 W for 0-180 W</td>
</tr>
<tr>
<td>MA2</td>
<td>Australia (MEPS) From 2008/9</td>
<td>≤ 0.50 W for 0-180 W</td>
</tr>
</tbody>
</table>
Agenda

• Regulatory requirements

• **Sources for standby power losses**

• Methods to lower the standby power consumption
• Measured results versus calculated results
• Conclusion
Application overview

- One application was selected.
- Notebook adaptor operating in a flyback topology.
  - Universal input 85 - 265 Vac
  - Vout 19 Vdc @ 90 W
  - Frequency 65 kHz
  - No power factor correction pre-regulation stage.
- Standby power losses calculations
  - Start-up resistors 70 Vac, or 100 Vdc
  - Standby power calculations 230 Vac (required)
- Standby power measured data
  - Measured data 230 Vac, or 325 Vdc
- Goal to have a standby power < 0.5 W minimum
- Desired < 0.3 W
What are the sources for standby power losses?

- Switching losses
- Gate charge losses
- Start-up circuits
- Bias circuits
- Snubbers
Switching losses

- Switching losses are associated with the controller turning on the power MOSFET each oscillator cycle.

\[
P = \frac{1}{2} \cdot C_{OSS} \cdot V_{DS}^2 \cdot Freq
\]

\[
P = \frac{1}{2} \cdot 390 \, \text{pF} \cdot 325 \, \text{V}^2 \cdot 65 \, \text{kHz} = 1.33 \, \text{W}
\]

Where:
Operating frequency = 65 kHz

MOSFET Characteristics:
\(V_{DS} = 650 \, \text{V}\)
\(I_D = 11 \, \text{A}\)
\(C_{OSS} = 390 \, \text{pF}\)
\(Q = \text{Gate Charge} = 45 \, \text{nC}\)

230 Vac \(\times 1.414 = 325 \, \text{V}\)
Gate charge loss

- The loss due to the controller charging and discharging the power MOSFET’s gate

\[ P = V_g \cdot Q \cdot F_{sw} = 13 \, V \cdot 45 \, nC \cdot 65 \, kHz = 38 \, mW \]

Q = Gate Charge = 45 nC

Lower gate charge devices are available, but they typically have a higher \( R_{DS(on)} \), decreasing the active efficiency of the SMPS at full load
Start-up circuits

- Start-up circuits are used in SMPS to start the controller when the input power is first applied to the power supply.

The start-up time is 5 s
CVcc 39 µF,
Vcon 12 V
50 µA is the start-up current of the controller

- The start-up current:
\[ I_{\text{TOTAL}} = I_{\text{START-UP Controller}} + C \frac{dV}{dt} \]

\[ I_{\text{TOTAL}} = 50 \, \mu A + 94 \, \mu A > 144 \, \mu A \text{ (Use 150 } \mu A) \]

Where:
\( dV = 12 \, V \) the controller turn-on threshold (VCCON)
\( dt = 5 \, s \) (the start-up time)
\( C = CVcc = 39 \, \mu F \)
Start-up circuits continued

\[ R_{\text{START} - \text{UP}} = \frac{V_{dc}}{I_{\text{Total}}} \]

\[ R_{\text{START} - \text{UP}} = \frac{100}{150} \frac{V_{dc}}{\mu A} = 667 \text{ k}\Omega \]

\[ P_{\text{START} - \text{UP}} = \frac{V_{\text{Bulk}}}{R_{\text{START} - \text{UP}}} \frac{2}{667} \frac{2}{k\Omega} = 160 \text{ mW} \]

\( P_{\text{START_UP}} \) is calculated at 230 Vac
**Start-up time vs. standby power**

Changing the start-up time to 500 ms
CVcc 39 µF,
Vccon 12 V
I\textsubscript{Vcc} = 50 µA is the start-up current of the controller

\[
I_{VCC} = C_{VCC} \frac{VCC \text{ \text{ON}}}{T_{\text{start\,-\,up}}} = 39 \, \mu F \times \frac{12 \, V}{500 \, ms} = 936 \, \mu A
\]

\[
I_{Total} = I_{VCC} + I_{\text{controller}} = 936 \, \mu A + 50 \, \mu A = 986 \, \mu A
\]

\[
R_{\text{START\,-\,UP}} = \frac{Vdc}{I_{\text{Total}}} = \frac{100 \, \mu A}{986 \, \mu A} = 100.4 \, k
\]

\[
P_{\text{START\,-\,UP}} = \frac{V_{\text{Bulk}}}{R_{\text{START\,-\,UP}}} = \frac{325 \, V}{101 \times .4 \, k} = 1.04 \, W
\]

To increase the start-up time, \(R_{\text{start-up}}\) must be lowered increasing the standby power.
Half-wave connection

\[ R_{\text{start-up}} = \frac{100 \text{ Vpk}}{150 \mu\text{A} \cdot \pi} = 212 \text{ k}\Omega \]

\[ P_{\text{start-up}} = \frac{V_{\text{in}}^2}{2 \cdot R_{\text{start-up}}} = \frac{230V_{\text{ac}}^2}{2 \cdot 212 \text{ k}\Omega} = 125 \text{ mW} \]

\[ P_{\text{start-up}}@ 230 \text{ Vac} = 125 \text{ mW, a 22\% reduction} \]
Integrated high voltage start-up MOSFETs

- The high voltage MOSFET is used as a current source that charges up the controllers Vcc capacitor when the input ac power is applied to the Power Supply.

Controller with a High Voltage Start-Up FET

Typical Isource 4 mA

The Start-Up time is 118 ms

Typical ILeakage 30 µA

\[ P_d = I_{Leakage} \cdot V_{Bulk} = 30 \mu A \cdot 325Vdc = 9.75mW \]

Advantages:

- Can reduce the standby power consumption by approximately **150 mW** (compared to a SMPS with the start-up resistors connected to the bulk capacitor) down to **9.75 mW**
- Faster start-up time.
Bias currents

- In any power supply there are a number of circuits that, if not carefully selected, can consume a significant amount of standby power.
  - TL431 Shunt Regulator (TL431 needs a minimum of 1 mA of cathode current).
  - Optocoupler for the output feedback signal.
  - Resistive dividers

- Output sensing and divider network impedance needs to be as high as possible

\[
V_{\text{sense}} = \frac{R_{\text{lower}}}{R_{\text{upper}} + R_{\text{lower}}} \quad V_{\text{out}} = \frac{7.4 \, k}{49.0 \, k + 7.4 \, k} \quad 19V = 2.5V
\]
Bias networks

\[
\text{Psense} = \frac{V_o^2}{R_{\text{upper}} + R_{\text{lower}}} = \frac{19^2}{57.3k} = 6.3 \text{ mW}
\]

\[V_{\text{Rin}} = 1 \text{ mA} \cdot 1 \text{k}\Omega = 1 \text{ V}\]

\[P_{\text{Rin}} = 1 \text{ mA}^2 \cdot 1 \text{k}\Omega = 1 \text{ mW}\]

\[\text{PTL431} = (V_o - V_{\text{Rin}} - V_{\text{opto}}) \cdot 1 \text{ mA} = (19 \text{ V} - 1 \text{ V} - 1 \text{ V}) \cdot 1 \text{ mA} = 17 \text{ mW}\]

\[P_{T_{\text{SECONDARY Side}}} = 24.3 \text{ mW}\]

The primary side controller bias current = 2 mA

\[P_{\text{controller}} = ICC \cdot V_{\text{cc}} = 2 \text{ mA} \cdot 13 \text{ V} = 26 \text{ mW}\]

The total losses due to bias currents are:

\[P_{\text{Total}} = P_{\text{sense}} + P_{\text{Rin}} + P_{\text{PTL431}} + P_{\text{controller}}\]

\[6.3 \text{ mW} + 1 \text{ mW} + 17 \text{ mW} + 26 \text{ mW} = 50.3 \text{ mW}\]

The goal was to keep the bias current losses on the secondary to less than 20 mW.
Snubber/clamp losses

**RDC snubber**

\[ P_R = \frac{1}{2} L_{LK} \cdot I_{pk}^2 \cdot Freq \cdot \frac{V_{clamp}}{V_{clamp} - V_{out} \cdot n} \]

**Zener clamp**

\[ P_Z = \frac{1}{2} I_{pk}^2 L_{LK} \cdot Freq \cdot \frac{V_{dc} - V_Z}{V_Z - V_{out} \cdot n} \]

Where:

- \( L_{LK} \) is the transformer leakage inductance
- \( I_{pk} \) is the transformer peak primary current
- \( Freq \) is the SMPS operating frequency
- \( V_{dc} \) is the SMPS HV dc bus
- \( V_Z \) is the zener break down voltage
- \( V_{clamp} \) is the RDC snubber clamp voltage
- \( V_{out} \) is the output voltage
- \( N \) is the transformer turns ratio
Losses summary

\[ PT_{\text{stand-by}} = P_{\text{Switching}} + P_{\text{Gate}} + P_{\text{Start-up}} + P_{\text{Bias}} \]

With 667 kΩ start-up resistors.

\[ PT_{\text{stand-by}} = 1.33 \text{ W} + 38 \text{ mW} + 160 \text{ mW} + 50.3 \text{ mW} = 1.58 \text{ W} \]

With HV start-up

\[ PT_{\text{stand-by}} = 1.33 \text{ W} + 38 \text{ mW} + 9.75 \text{ mW} + 50.3 \text{ mW} = 1.43 \text{ W} \]

Using Fixed frequency will not get us to the low standby power requirements.
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Methods to lower the standby power consumption

• Switching losses
  • Frequency foldback
  • Skip cycle operation

• Startup circuits

• Bias circuits
Frequency foldback

Operating frequency = 65 kHz → 24 kHz

\[ P = \frac{1}{2} \times 390 \text{ pF} \times 325 \text{ V}^2 \times 24 \text{ kHz} = 494 \text{ mW} \]

\[ \text{62% reduction in standby power losses, compared to Example 1 where the } P_{SW} = 1.33 \text{ W} \]

With 667 kΩ start-up resistor

\[ P_{STANDBY} = P_{SWITCHING} + P_{GATE} + P_{START\_UP} + P_{BIAS} = 494 \text{ mW} + 14 \text{ mW} + 160 \text{ mW} + 50.3 \text{ mW} = 720 \text{ mW} \]

With HV start-up

\[ 494 \text{ mW} + 14 \text{ mW} + 9.75 \text{ mW} + 50.3 \text{ mW} = 568 \text{ mW} \]
Skip cycle

\[ P = \frac{1}{2} \cdot C_{OSS} \cdot V_{DS}^2 \cdot \text{Freq} \cdot D_{\text{SKIP}} \]
Skip cycle with start-up resistors

Skip cycle switching loss calculation

\[ D_{\text{SKIP\_CYCLE}} = 7\% \text{ (measured)} \]

\[ P = \frac{1}{2} \cdot 390\text{pF} \cdot 325V^2 \cdot 65\text{kHz} \cdot 0.07 = 93\text{mW} \]

EQ 18: (With 667 kΩ start-up resistors)

\[ P_{\text{TSTANDBY\_Skip}} = P_{\text{SWITCHING}} \cdot D + P_{\text{GATE}} \cdot D + P_{\text{START\_UP}} + P_{\text{BIAS}} = \]

93 mW + 1.4 mW + 160 mW + 50.3 mW = **304 mW**

With HV start-up

93 mW + 1.4 mW + 9.75 mW + 50.3 mW = **155 mW**

Frequency foldback with HV start-up

PTSTANDBY frequency foldback = **568 mW**

Frequency foldback with 667 kΩ start-up resistor

PTSTANDBY = **720 mW**
Soft skip cycle

Skip cycle operation can lead to audible noise due to the instantaneous peak current which causes a mechanical resonance with the snubber capacitor and magnetic winding, and core.

Soft skip primary current waveform

- Soft skip reduces the high instantaneous peak current by ramping up the primary current
- This reduces the audible noise
- This increases the skip duty cycle
- Increasing the standby power
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Standby power results with start-up resistors

667 kΩ start-up resistors

<table>
<thead>
<tr>
<th>Vin</th>
<th>Fixed Frequency (65 kHz)</th>
<th>Frequency Foldback (65 kHz→24 kHz)</th>
<th>Skip cycle (65 kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>230 Vac</td>
<td>Calculated- 1.58 W Measured-1.7 W</td>
<td>Calculated- 720 mW Measured- 710 mW</td>
<td>Calculated- 304 mW Measured- 320 mW</td>
</tr>
</tbody>
</table>
## Standby power results with a HV start-up

<table>
<thead>
<tr>
<th>Vin</th>
<th>Skip with HV Start-Up (65 kHz)</th>
<th>Soft Skip with HV Start-Up (65 kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>230 Vac</td>
<td>Calculated-155 mW Measured- 160 mW</td>
<td>Measured- 190 mW</td>
</tr>
</tbody>
</table>
Conclusion

• Regulatory requirements worldwide are driving the reduction of standby power consumption

• Identification of sources for standby power losses:
  • Switching losses
  • Gate charge losses
  • Start-up circuits

• Identification of methods to lower the standby power
  • Switching losses
    • Frequency foldback
    • Skip cycle operation
  • Startup circuits
  • Bias circuits

• Very good correlation between calculated and measured results