TL594

Precision Switchmode Pulse Width Modulation Control Circuit

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

Features

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout
- Pb-Free Packages are Available*

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>VCC</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>Collector Output Voltage</td>
<td>VC1, VC2</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>Collector Output Current</td>
<td>IC1, IC2</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>Amplifier Input Voltage Range</td>
<td>VIR</td>
<td>−0.3 to +42</td>
<td>V</td>
</tr>
<tr>
<td>Power Dissipation @ TA ≤ 45°C</td>
<td>PD</td>
<td>1000</td>
<td>mW</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>RθUA</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-Ambient (PDIP)</td>
<td></td>
<td>140</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-Air (TSSOP)</td>
<td></td>
<td>135</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>TJ</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tslg</td>
<td>−55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>TA</td>
<td>−40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Derating Ambient Temperature</td>
<td>TA</td>
<td>45</td>
<td>°C</td>
</tr>
</tbody>
</table>

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum thermal limits must be observed.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>VCC</td>
<td>7.0</td>
<td>15</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Collector Output Voltage</td>
<td>V_{C1}, V_{C2}</td>
<td>–</td>
<td>30</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Collector Output Current (Each transistor)</td>
<td>I_{C1}, I_{C2}</td>
<td>–</td>
<td>–</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Amplified Input Voltage</td>
<td>V_{in}</td>
<td>0.3</td>
<td>–</td>
<td>V_{CC} − 2.0</td>
<td>V</td>
</tr>
<tr>
<td>Current Into Feedback Terminal</td>
<td>I_{fb}</td>
<td>–</td>
<td>–</td>
<td>0.3</td>
<td>mA</td>
</tr>
<tr>
<td>Reference Output Current</td>
<td>I_{ref}</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Timing Resistor</td>
<td>R_T</td>
<td>1.8</td>
<td>30</td>
<td>500</td>
<td>kΩ</td>
</tr>
<tr>
<td>Timing Capacitor</td>
<td>C_T</td>
<td>0.0047</td>
<td>0.001</td>
<td>10</td>
<td>µF</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>f_{osc}</td>
<td>1.0</td>
<td>40</td>
<td>300</td>
<td>kHz</td>
</tr>
<tr>
<td>PWM Input Voltage (Pins 3, 4, 13)</td>
<td>–</td>
<td>0.3</td>
<td>–</td>
<td>5.3</td>
<td>V</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)

#### For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REFERENCE SECTION</strong></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Reference Voltage</td>
<td>V_{ref}</td>
<td>4.925</td>
<td>5.0</td>
<td>5.075</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation (V_{CC} = 7.0 V to 40 V)</td>
<td>Reg_{line}</td>
<td>–</td>
<td>2.0</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>Load Regulation (I_O = 1.0 mA to 10 mA)</td>
<td>Reg_{load}</td>
<td>–</td>
<td>2.0</td>
<td>15</td>
<td>mV</td>
</tr>
<tr>
<td>Short Circuit Output Current (V_{ref} = 0 V)</td>
<td>I_{SC}</td>
<td>15</td>
<td>40</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td><strong>OUTPUT SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)</td>
<td>I_{C(off)}</td>
<td>–</td>
<td>2.0</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>Emitter Off-State Current (V_{CC} = 40 V, V_{C} = 40 V, V_E = 0 V)</td>
<td>I_{E(off)}</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>100</td>
</tr>
<tr>
<td>Collector–Emitter Saturation Voltage (Note 1)</td>
<td>V_{SAT(C)}</td>
<td>–</td>
<td>1.1</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Common–Emitter (V_E = 0 V, I_C = 200 mA)</td>
<td>–</td>
<td>1.5</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter–Follower (V_C = 15 V, I_E = −200 mA)</td>
<td>V_{SAT(E)}</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Output Control Pin Current</td>
<td>I_{OCL}</td>
<td>–</td>
<td>0.1</td>
<td>–</td>
<td>µA</td>
</tr>
<tr>
<td>Low State (V_OC ≤ 0.4 V)</td>
<td>–</td>
<td>2.0</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High State (V_OC = V_{ref})</td>
<td>I_{OCH}</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Rise Time</td>
<td>t_r</td>
<td>–</td>
<td>100</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Common–Emitter (See Figure 13)</td>
<td>–</td>
<td>100</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter–Follower (See Figure 14)</td>
<td>–</td>
<td>40</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Fall Time</td>
<td>t_r</td>
<td>–</td>
<td>40</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Common–Emitter (See Figure 13)</td>
<td>–</td>
<td>40</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter–Follower (See Figure 14)</td>
<td>–</td>
<td>40</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ERROR AMPLIFIER SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage (V_O (Pin 3) = 2.5 V)</td>
<td>V_{IO}</td>
<td>–</td>
<td>2.0</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Current (V_O (Pin 3) = 2.5 V)</td>
<td>I_{IO}</td>
<td>–</td>
<td>5.0</td>
<td>250</td>
<td>nA</td>
</tr>
<tr>
<td>Input Bias Current (V_O (Pin 3) = 2.5 V)</td>
<td>I_{IB}</td>
<td>–</td>
<td>–</td>
<td>−0.1</td>
<td>−1.0</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)</td>
<td>V_{ICR}</td>
<td>0</td>
<td>V_{CC}–2.0</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Inverting Input Voltage Range</td>
<td>V_{IR(INV)}</td>
<td>–</td>
<td>−0.3</td>
<td>V_{CC}–2.0</td>
<td>V</td>
</tr>
<tr>
<td>Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)</td>
<td>A_{VOL}</td>
<td>70</td>
<td>95</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)</td>
<td>f_C</td>
<td>–</td>
<td>700</td>
<td>–</td>
<td>kHz</td>
</tr>
<tr>
<td>Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)</td>
<td>φ_m</td>
<td>–</td>
<td>65</td>
<td>–</td>
<td>deg</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio (V_{CC} = 40 V)</td>
<td>CMRR</td>
<td>65</td>
<td>90</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)</td>
<td>PSRR</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Output Sink Current (V_O (Pin 3) = 0.7 V)</td>
<td>I_{O−}</td>
<td>0.3</td>
<td>0.7</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Output Source Current (V_O (Pin 3) = 3.5 V)</td>
<td>I_{O+}</td>
<td>–</td>
<td>−2.0</td>
<td>−4.0</td>
<td>–</td>
</tr>
</tbody>
</table>

1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

http://onsemi.com
### ELECTRICAL CHARACTERISTICS (VCC = 15 V, CT = 0.01 μF, RT = 12 kΩ, unless otherwise noted.)

For typical values TA = 25°C, for min/max values TA is the operating ambient temperature range that applies, unless otherwise noted.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PWM COMPARATOR SECTION</strong> <em>(Test Circuit Figure 11)</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Threshold Voltage (Zero Duty Cycle)</td>
<td>( V_{TH} )</td>
<td>–</td>
<td>3.6</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>Input Sink Current ( (V_{Pin,3} = 0.7 , \text{V}) )</td>
<td>( I_l )</td>
<td>0.3</td>
<td>0.7</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td><strong>DEADTIME CONTROL SECTION</strong> <em>(Test Circuit Figure 11)</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (Pin 4) ( (V_{Pin,4} = 0 , \text{V} , \text{to} , 5.25 , \text{V}) )</td>
<td>( I_{IB,(DT)} )</td>
<td>–</td>
<td>–2.0</td>
<td>–10</td>
<td>μA</td>
</tr>
<tr>
<td>Maximum Duty Cycle, Each Output, Push-Pull Mode ( (V_{Pin,4} = 0 , \text{V}, , C_T = 0.01 , \mu\text{F}, , R_T = 12 , \text{kΩ}) )</td>
<td>( DC_{max} )</td>
<td>45</td>
<td>48</td>
<td>50</td>
<td>%</td>
</tr>
<tr>
<td>( (V_{Pin,4} = 0 , \text{V}, , C_T = 0.001 , \mu\text{F}, , R_T = 30 , \text{kΩ}) )</td>
<td></td>
<td>–</td>
<td>45</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Input Threshold Voltage (Pin 4) ( (\text{Zero Duty Cycle}) )</td>
<td>( V_{TH} )</td>
<td>–</td>
<td>2.8</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>(Maximum Duty Cycle)</td>
<td></td>
<td>0</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td><strong>OSCILLATOR SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency ( (C_T = 0.001 , \mu\text{F}, , R_T = 30 , \text{kΩ}) )</td>
<td>( f_{osc} )</td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>kHz</td>
</tr>
<tr>
<td>( (C_T = 0.01 , \mu\text{F}, , R_T = 12 , \text{kΩ}, , TA = 25°C) )</td>
<td></td>
<td>9.2</td>
<td>10</td>
<td>10.8</td>
<td></td>
</tr>
<tr>
<td>( (C_T = 0.01 , \mu\text{F}, , R_T = 12 , \text{kΩ}, , TA = T_{low} , \text{to} , T_{high}) )</td>
<td></td>
<td>9.0</td>
<td>–</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Standard Deviation of Frequency* ( (C_T = 0.001 , \mu\text{F}, , R_T = 30 , \text{kΩ}) )</td>
<td>( \sigma_{f_{osc}} )</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Frequency Change with Voltage ( (V_{CC} = 7.0 , \text{V} , \text{to} , 40 , \text{V}, , TA = 25°C) )</td>
<td>( \Delta f_{osc} ,(\Delta V) )</td>
<td>–</td>
<td>0.2</td>
<td>1.0</td>
<td>%</td>
</tr>
<tr>
<td>Frequency Change with Temperature ( (\Delta T_A = T_{low} , \text{to} , T_{high}, , C_T = 0.01 , \mu\text{F}, , R_T = 12 , \text{kΩ}) )</td>
<td>( \Delta f_{osc} ,(\Delta T) )</td>
<td>–</td>
<td>4.0</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td><strong>UNDERVOLTAGE LOCKOUT SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Threshold ( (V_{CC} , \text{Increasing}, , I_{ref} = 1.0 , \text{mA}) )</td>
<td>( V_{th} )</td>
<td>4.0</td>
<td>5.2</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>( T_A = 25°C )</td>
<td></td>
<td>3.5</td>
<td>–</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td>( T_A = T_{low} , \text{to} , T_{high} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td>( V_{H} )</td>
<td>100</td>
<td>150</td>
<td>300</td>
<td>mV</td>
</tr>
<tr>
<td>TL594 C/I</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TL594M</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>TOTAL DEVICE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby Supply Current ( (\text{Pin 6 at} , V_{ref}, , \text{All other inputs and outputs open}) )</td>
<td>( I_{CC} )</td>
<td>–</td>
<td>8.0</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>( (V_{CC} = 15 , \text{V}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( (V_{CC} = 40 , \text{V}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average Supply Current ( (V_{Pin,4} = 2.0 , \text{V}, , C_T = 0.01 , \mu\text{F}, , R_T = 12 , \text{kΩ}, , V_{CC} = 15 , \text{V}, , \text{See Figure 11}) )</td>
<td></td>
<td>–</td>
<td>11</td>
<td>–</td>
<td>mA</td>
</tr>
</tbody>
</table>

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula,
\[
\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}
\]
This device contains 46 active transistors.

Figure 1. Representative Block Diagram

Figure 2. Timing Diagram
Description
The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1) An internal-linear sawtooth oscillator is frequency-programmable by two external components, $R_T$ and $C_T$. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \cdot C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $C_T$ to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to $(V_{CC} − 2$ V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor $C_T$ is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse-steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $±1.5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

### Functional Table

<table>
<thead>
<tr>
<th>Input/Output Controls</th>
<th>Output Function</th>
<th>$f_{out}$/$f_{osc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grounded</td>
<td>Single-ended PWM @ Q1 and Q2</td>
<td>1.0</td>
</tr>
<tr>
<td>@ $V_{ref}$</td>
<td>Push–pull Operation</td>
<td>0.5</td>
</tr>
</tbody>
</table>

### Figure 3. Oscillator Frequency versus Timing Resistance

### Figure 4. Open Loop Voltage Gain and Phase versus Frequency
Figure 5. Percent Deadtime versus Oscillator Frequency

Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

Figure 9. Standby Supply Current versus Supply Voltage

Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current
Figure 11. Error−Amplifier Characteristics

Figure 12. Deadtime and Feedback Control Circuit

Figure 13. Common−Emitter Configuration Test Circuit and Waveform

Figure 14. Emitter−Follower Configuration Test Circuit and Waveform
Figure 15. Error-Amplifier Sensing Techniques

\[
V_O = V_{\text{ref}} \left( 1 + \frac{R_1}{R_2} \right)
\]

Figure 16. Deadtime Control Circuit

Max. % on Time, each output = 45 - \left( \frac{80}{1 + \frac{R_1}{R_2}} \right)

Figure 17. Soft-Start Circuit

Figure 18. Output Connections for Single-Ended and Push-Pull Configurations
Figure 19. Slaving Two or More Control Circuits

Figure 20. Operation with $V_{in} > 40$ V Using External Zener

Figure 21. Pulse Width Modulated Push–Pull Converter

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 10$ V to 40 V</td>
<td>14 mV 0.28%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 28$ V, $I_O = 1.0$ mA to 1.0 A</td>
<td>3.0 mV 0.06%</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 28$ V, $I_O = 1.0$ A</td>
<td>65 mVpp P.A.R.D.</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>$V_{in} = 28$ V, $R_L = 0.1$ Ω</td>
<td>1.6 A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 28$ V, $I_O = 1.0$ A</td>
<td>71%</td>
</tr>
</tbody>
</table>

$V_O = 28$ V
$I_O = 0.2$ A

$+V_{in} = 8.0$ V to 20V

All capacitors in μF

http://onsemi.com
Figure 22. Pulse Width Modulated Step-Down Converter

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 8.0$ V to 40 V</td>
<td>3.0 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.01%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 12.6$ V, $I_O = 0.2$ mA to 200 mA</td>
<td>5.0 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.02%</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 12.6$ V, $I_O = 200$ mA</td>
<td>40 mVpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P.A.R.D.</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>$V_{in} = 12.6$ V, $R_L = 0.1$ $\Omega$</td>
<td>250 mA</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 12.6$ V, $I_O = 200$ mA</td>
<td>72%</td>
</tr>
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</table>

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL594CD</td>
<td>−40 to 85°C</td>
<td>SOIC−16</td>
<td>48 Units/Rail</td>
</tr>
<tr>
<td>TL594CDG</td>
<td>−40 to 85°C</td>
<td>SOIC−16 (Pb−Free)</td>
<td>48 Units/Rail</td>
</tr>
<tr>
<td>TL594CDR2</td>
<td>−40 to 85°C</td>
<td>SOIC−16</td>
<td>2400 Tape &amp; Reel</td>
</tr>
<tr>
<td>TL594CDR2G</td>
<td>−40 to 85°C</td>
<td>SOIC−16 (Pb−Free)</td>
<td>2400 Tape &amp; Reel</td>
</tr>
<tr>
<td>TL594CN</td>
<td>−40 to 85°C</td>
<td>PDIP−16</td>
<td>25 Units/Rail</td>
</tr>
<tr>
<td>TL594CNG</td>
<td>−40 to 85°C</td>
<td>PDIP−16 (Pb−Free)</td>
<td>25 Units/Rail</td>
</tr>
<tr>
<td>TL594CDTBG*</td>
<td>−40 to 85°C</td>
<td>TSSOP−16*</td>
<td>96 Units/Rail</td>
</tr>
<tr>
<td>TL594CDTBR2G</td>
<td>−40 to 85°C</td>
<td>TSSOP−16*</td>
<td>2500 Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb−Free.
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

PDIP–16
CASE 648–08
ISSUE V

DATE 22 APR 2015

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
   AGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
   NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
   PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
   TO DATUM C.
6. DIMENSION eb IS MEASURED AT THE LEAD TIPS WITH THE
   LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
   LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
   CORNERS).

<table>
<thead>
<tr>
<th>DIM</th>
<th>INCHES</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.210</td>
<td>5.33</td>
</tr>
<tr>
<td>A1</td>
<td>0.015</td>
<td>0.38</td>
</tr>
<tr>
<td>A2</td>
<td>0.115</td>
<td>2.92</td>
</tr>
<tr>
<td>b</td>
<td>0.014</td>
<td>0.35</td>
</tr>
<tr>
<td>b2</td>
<td>0.060</td>
<td>1.52</td>
</tr>
<tr>
<td>b3</td>
<td>0.008</td>
<td>0.20</td>
</tr>
<tr>
<td>b2</td>
<td>0.014</td>
<td>0.35</td>
</tr>
<tr>
<td>C</td>
<td>0.735</td>
<td>18.77</td>
</tr>
<tr>
<td>D</td>
<td>0.775</td>
<td>19.77</td>
</tr>
<tr>
<td>D1</td>
<td>0.005</td>
<td>0.13</td>
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<tr>
<td>E</td>
<td>0.320</td>
<td>8.12</td>
</tr>
<tr>
<td>E1</td>
<td>0.240</td>
<td>6.10</td>
</tr>
<tr>
<td>e</td>
<td>0.100</td>
<td>2.54</td>
</tr>
<tr>
<td>M</td>
<td>10°</td>
<td>10°</td>
</tr>
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NOTE 1:

NOTE 2:
CONTROLLING DIMENSION: INCHES.

NOTE 3:
DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
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NOTE 4:
DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
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NOTE 5:
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PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
TO DATUM C.

NOTE 6:
DIMENSION eb IS MEASURED AT THE LEAD TIPS WITH THE
LEADS UNCONSTRAINED.

NOTE 7:
DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
LEADS, WHERE THE LEADS EXIT THE BODY.

NOTE 8:
PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
CORNERS).

STYLE 1:
PIN 1. CATHODE
PIN 2. CATHODE
PIN 3. CATHODE
PIN 4. CATHODE
PIN 5. CATHODE
PIN 6. CATHODE
PIN 7. CATHODE
PIN 8. CATHODE
PIN 9. ANODE
PIN 10. ANODE
PIN 11. ANODE
PIN 12. ANODE
PIN 13. ANODE
PIN 14. ANODE
PIN 15. ANODE
PIN 16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
PIN 2. COMMON DRAIN
PIN 3. COMMON DRAIN
PIN 4. COMMON DRAIN
PIN 5. COMMON DRAIN
PIN 6. COMMON DRAIN
PIN 7. COMMON DRAIN
PIN 8. COMMON DRAIN
PIN 9. GATE
PIN 10. GATE
PIN 11. GATE
PIN 12. GATE
PIN 13. SOURCE
PIN 14. SOURCE
PIN 15. SOURCE
PIN 16. SOURCE

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC–16
CASE 751B–05
ISSUE K

DATE 29 DEC 2006

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSION.
4. MAXIMUM MOLD PROTUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. Emitter
4. NO CONNECTION
5. Emitter
6. BASE
7. Collector
8. Collector
9. Collector
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. Collector
15. Collector
16. Collector

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #3
9. BASE, #3
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. ANODE
11. NO CONNECTION
12. NO CONNECTION
13. GATE, #3
14. GATE, #2
15. GATE, #2
16. GATE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. NO CONNECTION
11. NO CONNECTION
12. NO CONNECTION
13. NO CONNECTION
14. NO CONNECTION
15. NO CONNECTION
16. NO CONNECTION

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
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4. MAXIMUM MOLD PROTUSION 0.15 (0.006) PER SIDE.
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6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSION.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIMENSIONS: MILLIMETERS

PHOTO 1 OF 1

EXPLANATION: SOIC–16

DESCRIPTION: "SOIC–16"

DOCUMENT NUMBER: 98ASB42566B

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 CASE 948F−01 ISSUE B

DATE 19 OCT 2006

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
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SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
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SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
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6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
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6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
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6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

G PITCH 0.65

DETAIL E

SECTION N–N
SEATING PLANE
IDENT.

PIN 1

DETAIL E

NEAR SIDE

NONE

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
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