ESD and Surge Protection Device

Low Capacitance Surge Protection for High Speed Data

SZNSP8814L

The SZNSP8814L surge protector is designed specifically to protect 10/100 and GbE Ethernet signals from high levels of surge current. Low clamping voltage under high surge conditions make this device an ideal solution for protecting voltage sensitive lines leading to Ethernet transceiver chips. Low capacitance combined with flow-through style packaging allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high-speed differential lines.

Features

- Protection for the Following IEC Standards:
  IEC 61000−4−2 (ESD) ±30 kV (Contact)
  IEC 61000−4−5 (Lightning) 35 A (8/20 μs)
- Flow−Thru Routing Scheme
- Low Capacitance: 2 pF Max (I/O to I/O)
- UL Flammability Rating of 94 V−0
- Wettable Flank Package for optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

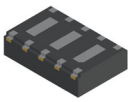
- In Vehicle Networking (IVN)
- Open Alliance BroadR−Reach (OABR)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8/20 Double Exponential Waveform	P_{PK}	562	W
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD) ISO 10605 330 pF / 330 Ω Contact ISO 10605 330 pF / 2 kΩ Contact ISO 10605 150 pF / 2 kΩ Contact	ESD	±8 ±30 ±30 ±30 ±30 ±30	kV
Maximum Peak Pulse Current 8/20 μs @ T_A = 25°C 10/700 μs @ T_A = 25°C	I_{PP}	 35 14	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



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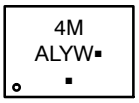
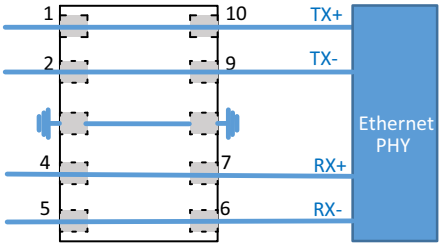
MARKING DIAGRAM



4M = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

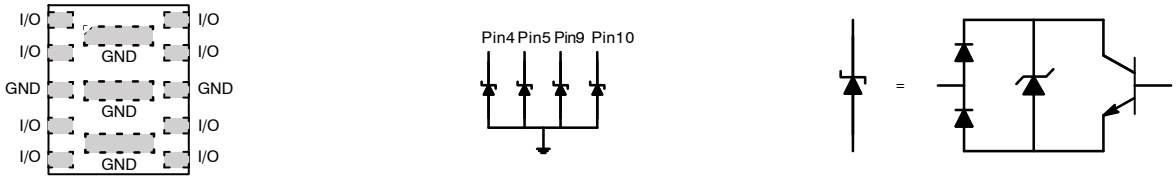
TYPICAL APPLICATION



ORDERING INFORMATION

Device	Package	Shipping†
SZNSP8814LMTWTAG	WDFNW10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

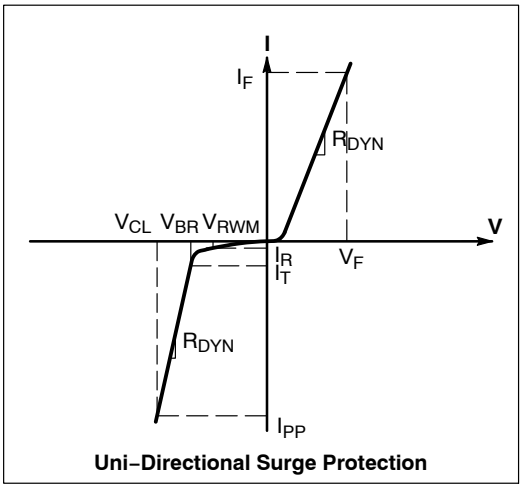


Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$
I_F	Forward Current
V_F	Forward Voltage @ I_F



Uni−Directional Surge Protection

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	Any I/O to GND (Note 1)			3.0	V
V_F	Forward Voltage	I_F = 10 mA, GND to All IO Pins	0.5	0.85	1.1	V
V_{BR}	Breakdown Voltage	I_T = 1 mA, I/O to GND	3.2	3.5	5.0	V
I_R	Reverse Leakage Current	V_{RWM} = 3.0 V, I/O to GND			0.5	μA
V_C	Clamping Voltage (Note 2)	I_{PP} = 1 A I_{PP} = 10 A I_{PP} = 25 A I_{PP} = 35 A		4.0 6.0 8.0 10	5.0 6.5 10 15	V
V_C	Clamping Voltage	IEC61000−4−2, ±8 kV Contact	See Figures 7 and 8			
C_J	Junction Capacitance	V_R = 0 V, f = 1 MHz between I/O Pins		1.5	2.0	pF
		V_R = 0 V, f = 1 MHz between I/O Pins and GND			5.0	
I_L	Insertion Loss	f = 1 GHz		−1		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. Any I/O to GND (8/20 μs pulse).

TYPICAL CHARACTERISTICS

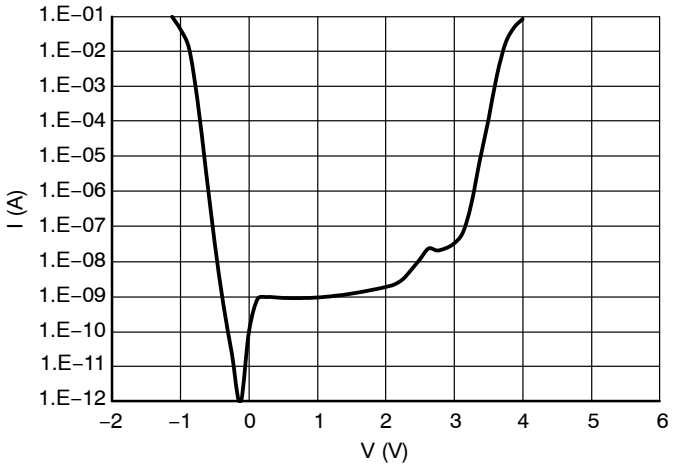


Figure 1. IV Characteristics

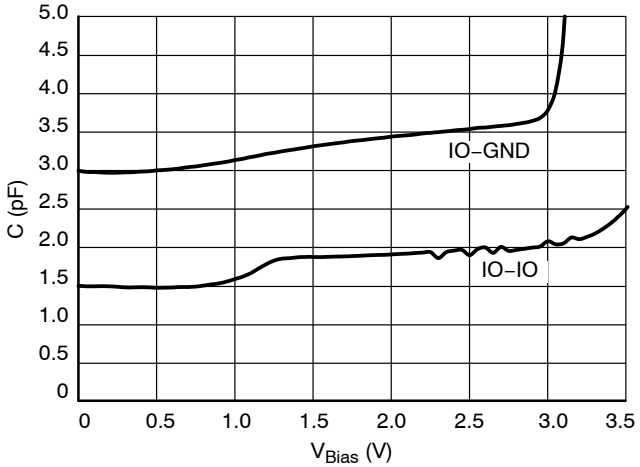


Figure 2. CV Characteristics

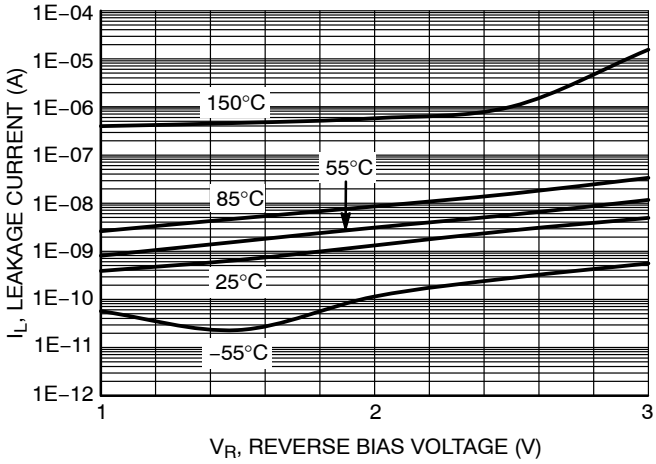


Figure 3. I_R vs. Temperature Characteristics

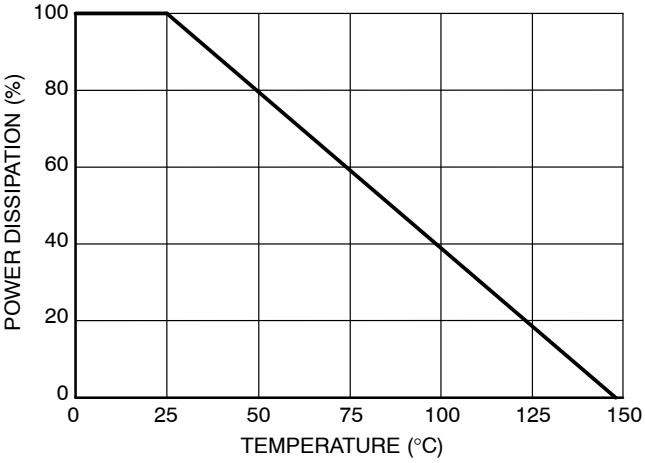


Figure 4. Steady State Power Derating

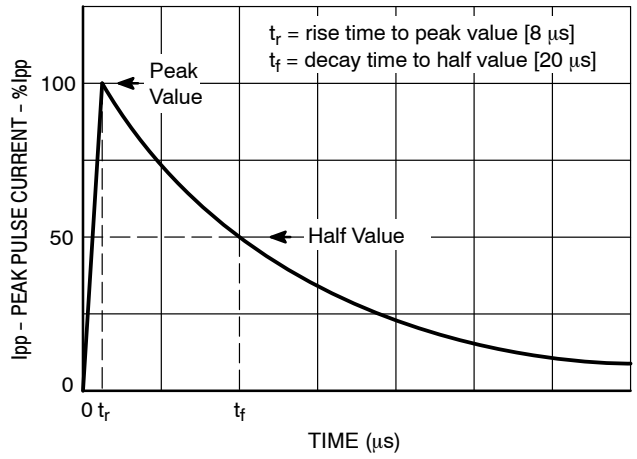


Figure 5. IEC61000−4−5 Pulse Waveform (8/20 μs)

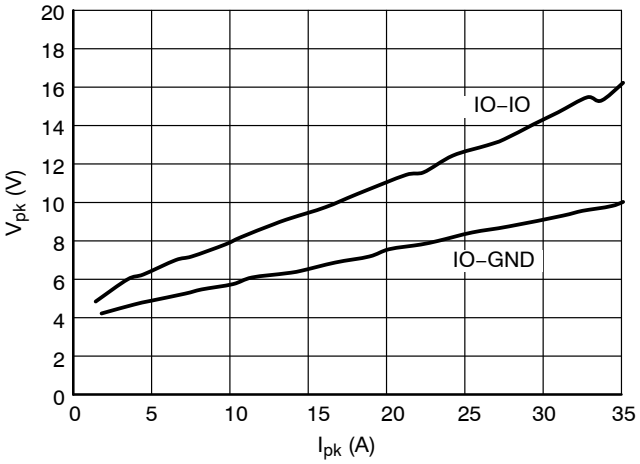


Figure 6. Clamping Voltage vs. Peak Pulse Current (8/20 μs)

TYPICAL CHARACTERISTICS

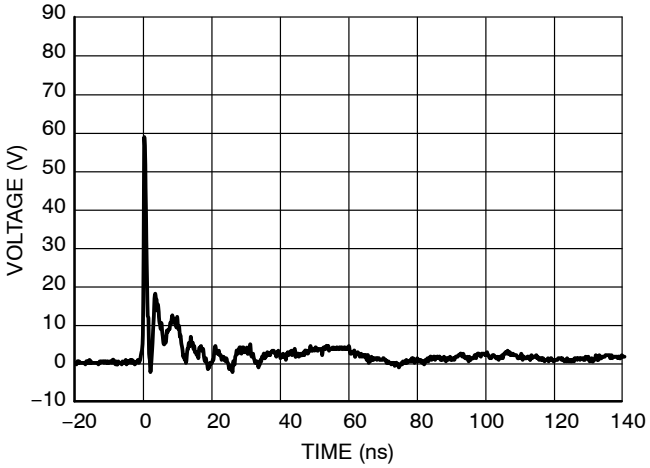


Figure 7. IEC61000−4−2 +8 kV Contact Clamping Voltage

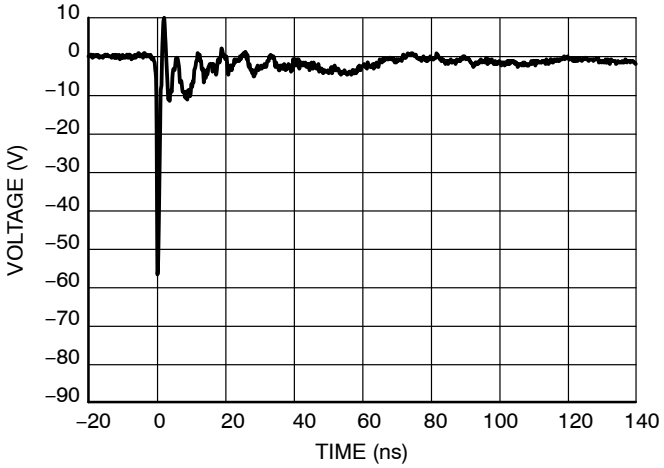


Figure 8. IEC61000−4−2 −8 kV Contact Clamping Voltage

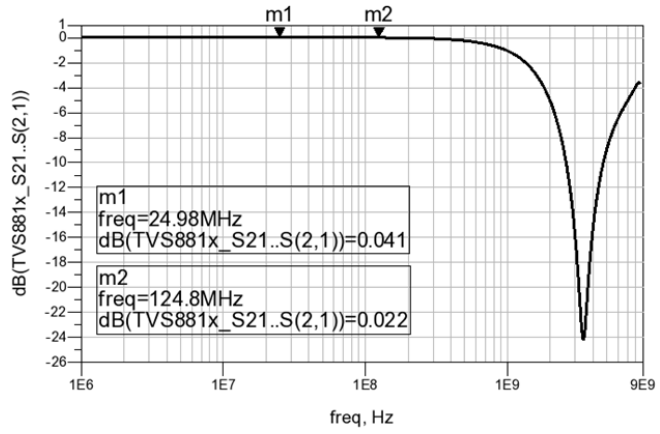


Figure 9. Typical Insertion Loss

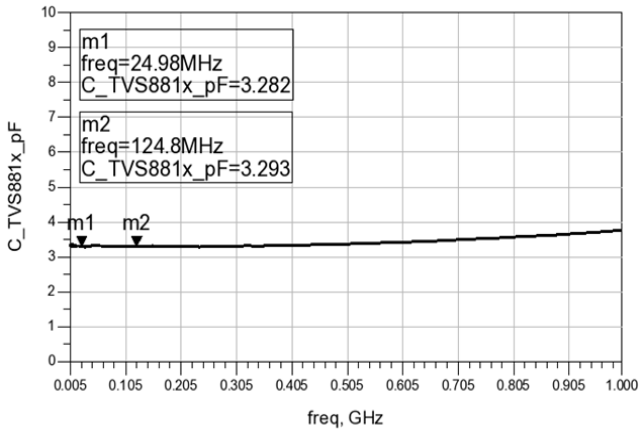


Figure 10. Typical Capacitance vs. Frequency

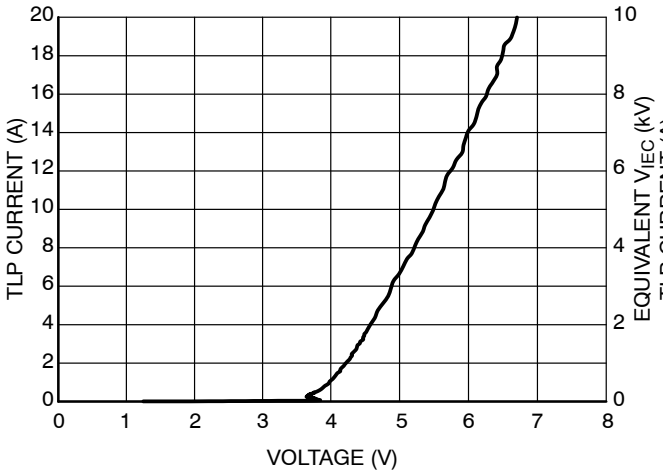


Figure 11. Positive TLP IV Curve

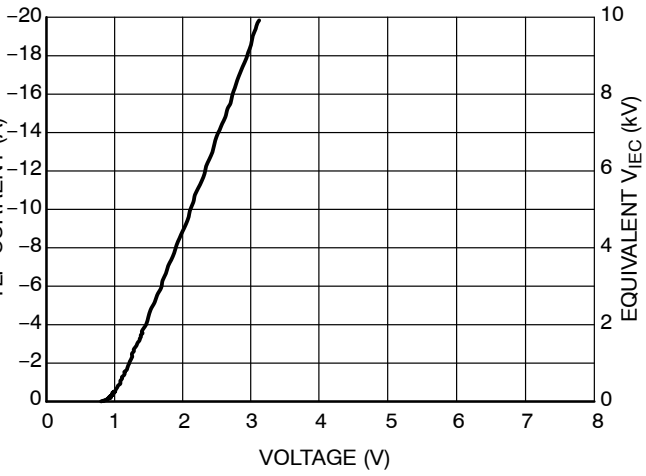
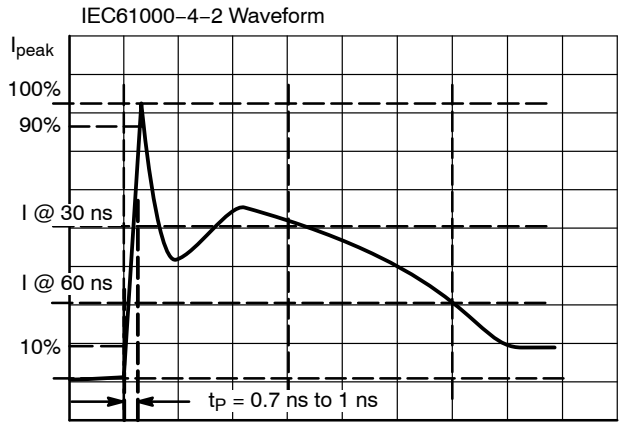


Figure 12. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.



IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

Figure 13. IEC61000−4−2 Spec

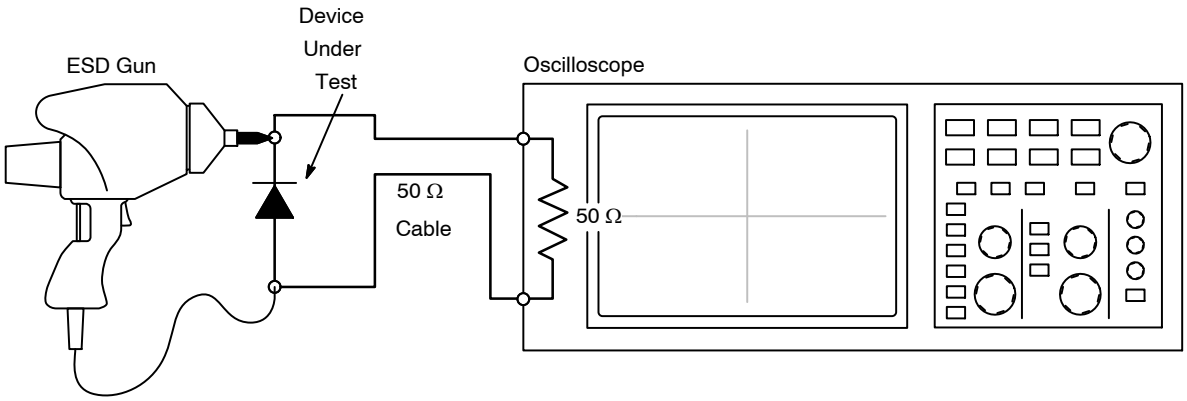


Figure 14. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 15. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 16 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

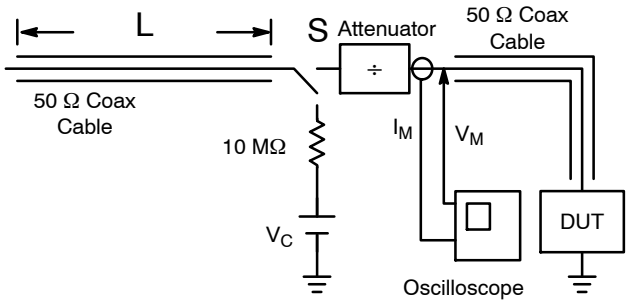


Figure 15. Simplified Schematic of a Typical TLP System

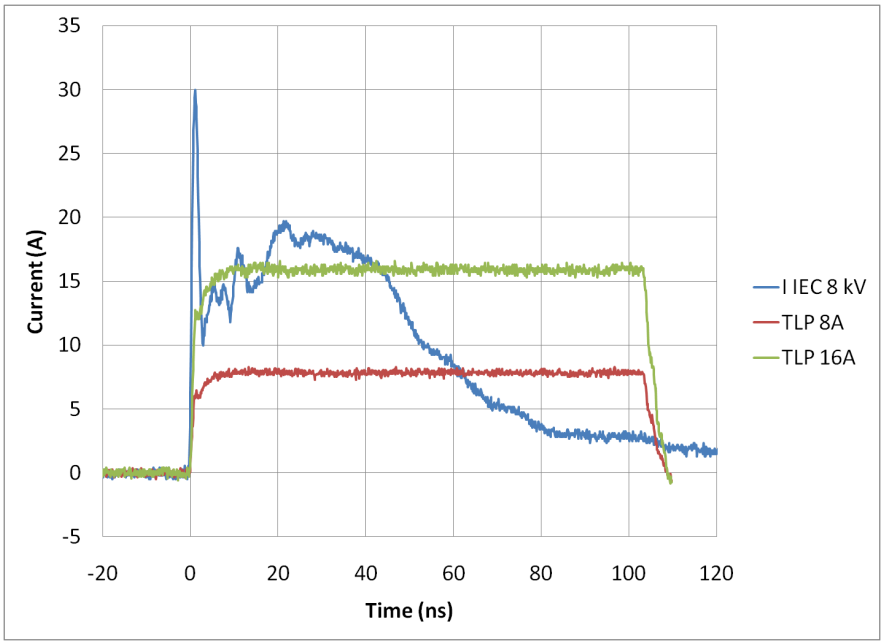
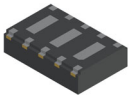


Figure 16. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms



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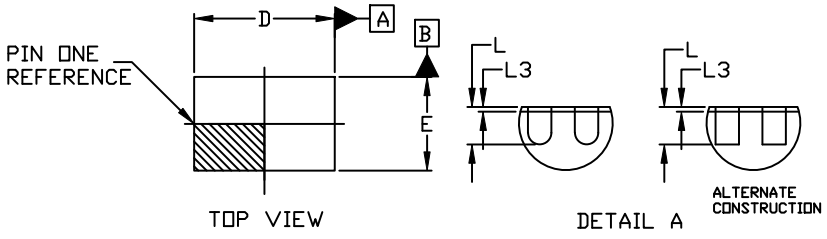
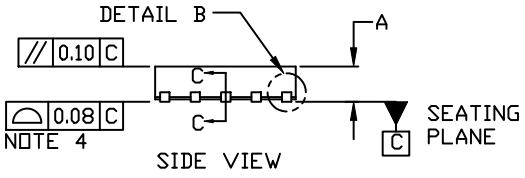
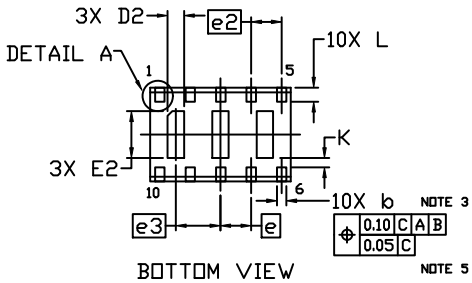
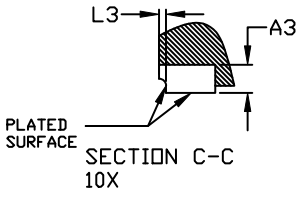
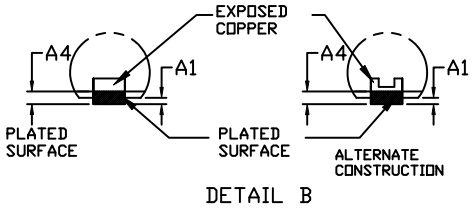
DATE 05 FEB 2020











NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

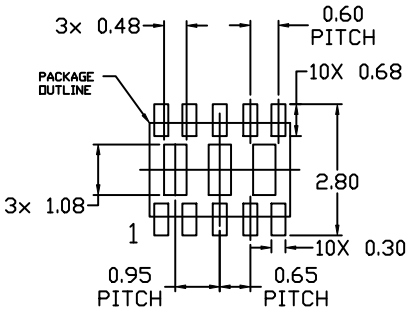
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	0.25	0.35	0.45
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
e2	0.60 BSC		
e3	0.95 BSC		
K	0.20 REF		
L	0.25	0.30	0.35
L3	---	---	0.09

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFNW10 3.0x2.0, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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onsemi Website: www.onsemi.com

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