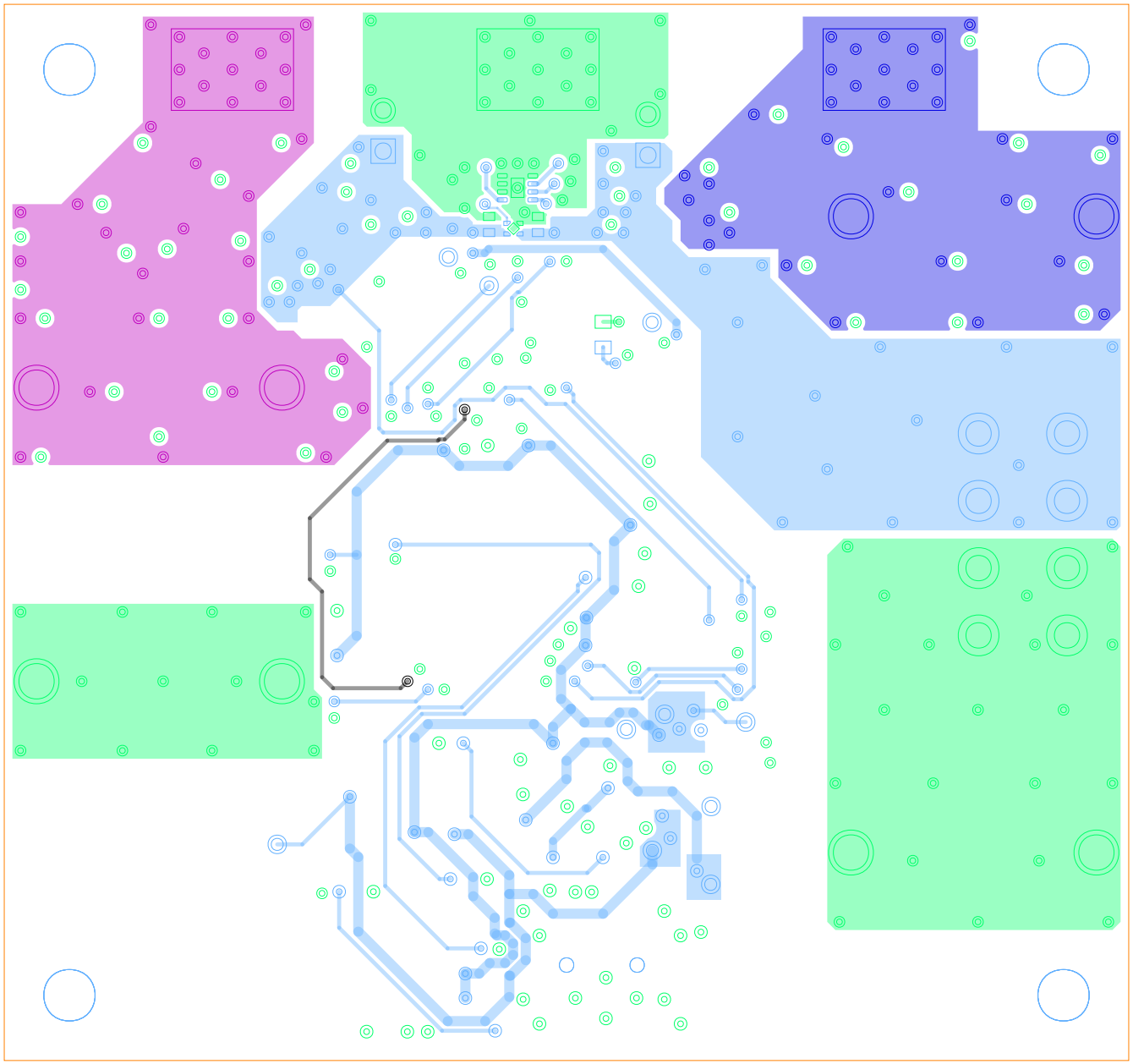
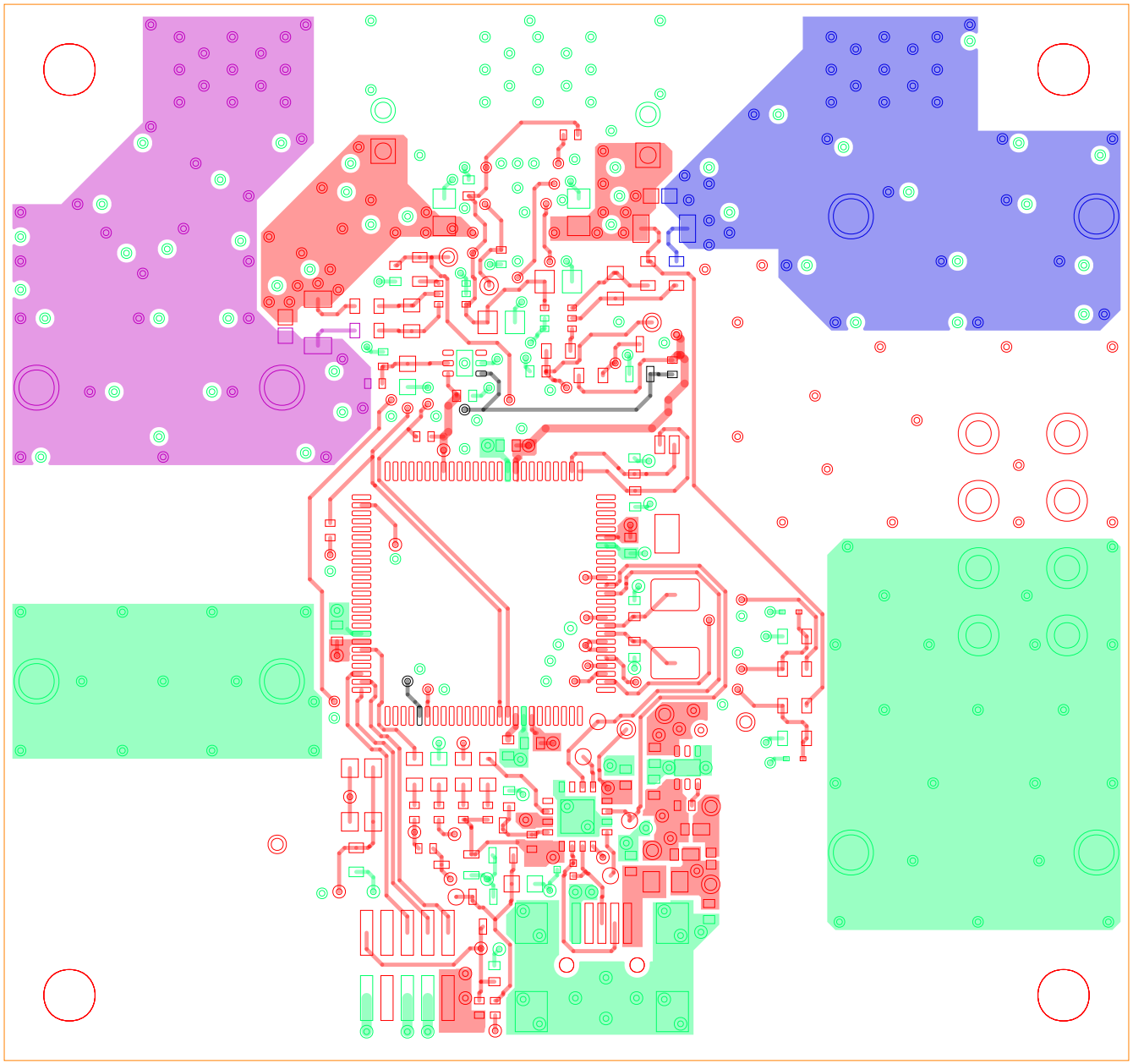
ART FILM - TOP

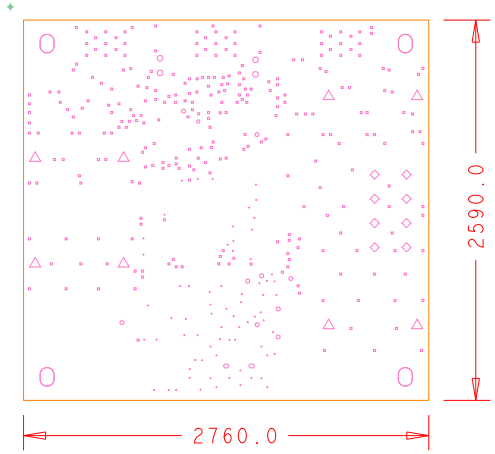


ART FILM - TOP

ART FILM - BOTTOM



ART FILM - BOTTOM



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
·	14.0	+2.0/-6.0	PLATED	70
▫	14.0	+2.0/-6.0	PLATED	279
○	23.6	+2.0/-2.0	PLATED	1
○	29.5	+2.0/-2.0	PLATED	9
○	40.0	+4.0/-4.0	PLATED	4
◇	62.0	+0.0/-0.0	PLATED	8
△	86.6	+3.9/-3.9	PLATED	8
○	35.4	+2.0/-2.0	NON-PLATED	2
○	126.0	+5.0/-5.0	NON-PLATED	8

STACKUP TABLE
Unit = Mils

#	NAME	TYPE	MATERIAL	THICKNESS
		SURFACE	AIR	0
1	TOP	CONDUCTOR	COPPER	1.4
		DIELECTRIC	FR-4	7
2	L2	PLANE	COPPER	1.2
		DIELECTRIC	FR-4	44
3	L3	PLANE	COPPER	1.2
		DIELECTRIC	FR-4	7
4	BOTTOM	CONDUCTOR	COPPER	1.4
		SURFACE	AIR	0
		TOTAL THICKNESS		63.2

NOTES (UNLESS OTHERWISE SPECIFIED):

1. BUILD IN ACCORDANCE WITH IPC 6011, IPC 6012, OR IPC 6013 DEPENDANT ON TYPE OF PRINTED CIRCUIT BOARD, CLASS 2.
2. LAMINATE MATERIAL SHALL MEET THE REQUIREMENTS OF IPC 4101 TYPE 370HR PER STACKUP DETAIL OR EQUIVALENT. (NOMINAL DIELECTRIC THICKNESS WITHIN +/- 10% OF STACKUP DETAIL).
3. ~~FINISH: ENIG 2-MICRO-INCHES MINIMUM OF GOLD OVER 118-236 MICRO-INCHES OF NICKEL.~~
4. TOP SIDE SHOWN.
5. HOLE DIAMETERS ARE AFTER PLATING, 0.8 MIL AVERAGE.
6. SILKSCREEN BOTH SIDES USING EPOXY OR ACRYLIC BASED WHITE NON-CONDUCTIVE SILKSCREEN. NOTE: LEGEND SHOULD BE REMOVED FROM ANY CONDUCTIVE SURFACE UNLESS OTHERWISE SPECIFIED. NO SILKSCREEN ON PADS.
7. SILK VENDOR ID, UL DESIGNATION, AND DATECODE ON THE BACKSIDE.
8. SOLDER MASK BOTH SIDES GREEN USING LIQUID PHOTO IMAGEABLE METHOD. NO SOLDERMASK ON PADS.
9. ~~IMPEDANCE REQUIREMENTS ARE AS FOLLOWS. +/- 10%. IF PRESENT, ALL OUTER 6.25 MIL WIDE TRACES 50 OHM SINGLE ENDED. IF PRESENT, ALL INNER 5.25 MIL WIDE TRACES 50 OHM SINGLE ENDED. TRACE WIDTHS SHALL NOT BE MODIFIED WITHOUT APPROVAL FROM ON SEMICONDUCTOR.~~
10. ALL ARTWORK AND DESIGN MEDIA SHALL BE SPECIFIED BY ON SEMICONDUCTOR. NO CHANGES WILL BE ALLOWED WITHOUT SPECIFIC APPROVAL FROM ON SEMICONDUCTOR.
11. TOOLING HOLES ARE TO BE DRILLED AWAY AT THE SAME TIME AS OTHER HOLES.
12. ALL MATERIALS ARE TO BE ROHS AND WEE COMPLIANT.
13. LAYER STACKUP INFORMATION INCLUDED IN THIS DRAWING SHOWS OUTER LAYER THICKNESS AFTER PLATING AND SUPERSEDES ANY OTHER DESIGN DOCUMENTATION.
14. ELECTRICALLY DISCONNECTED COPPER THIEVING IS ACCEPTABLE TO HELP MAINTAIN COPPER PLATING DISTRIBUTION IN LOW PRESSURE AREAS TO AVOID DELAMINATION.
15. REMOVAL OF NON-FUNCTIONAL PADS ON INNER LAYERS IS ACCEPTABLE.
16. ~~<DO NOT> PROVIDE BOARDS IN ARRAY FORMAT. ARRAYS SHOULD HAVE MINIMUM OF 250 MILS ON ALL SIDES.~~

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN MILS	DRAWN: MICHAEL OATMAN	01/29/19
TOLERANCES ON:	CHECKED: MICHAEL OATMAN	01/29/19
	ENGRG: MICHAEL OATMAN	01/29/19
	ISSUED: MICHAEL OATMAN	01/29/19

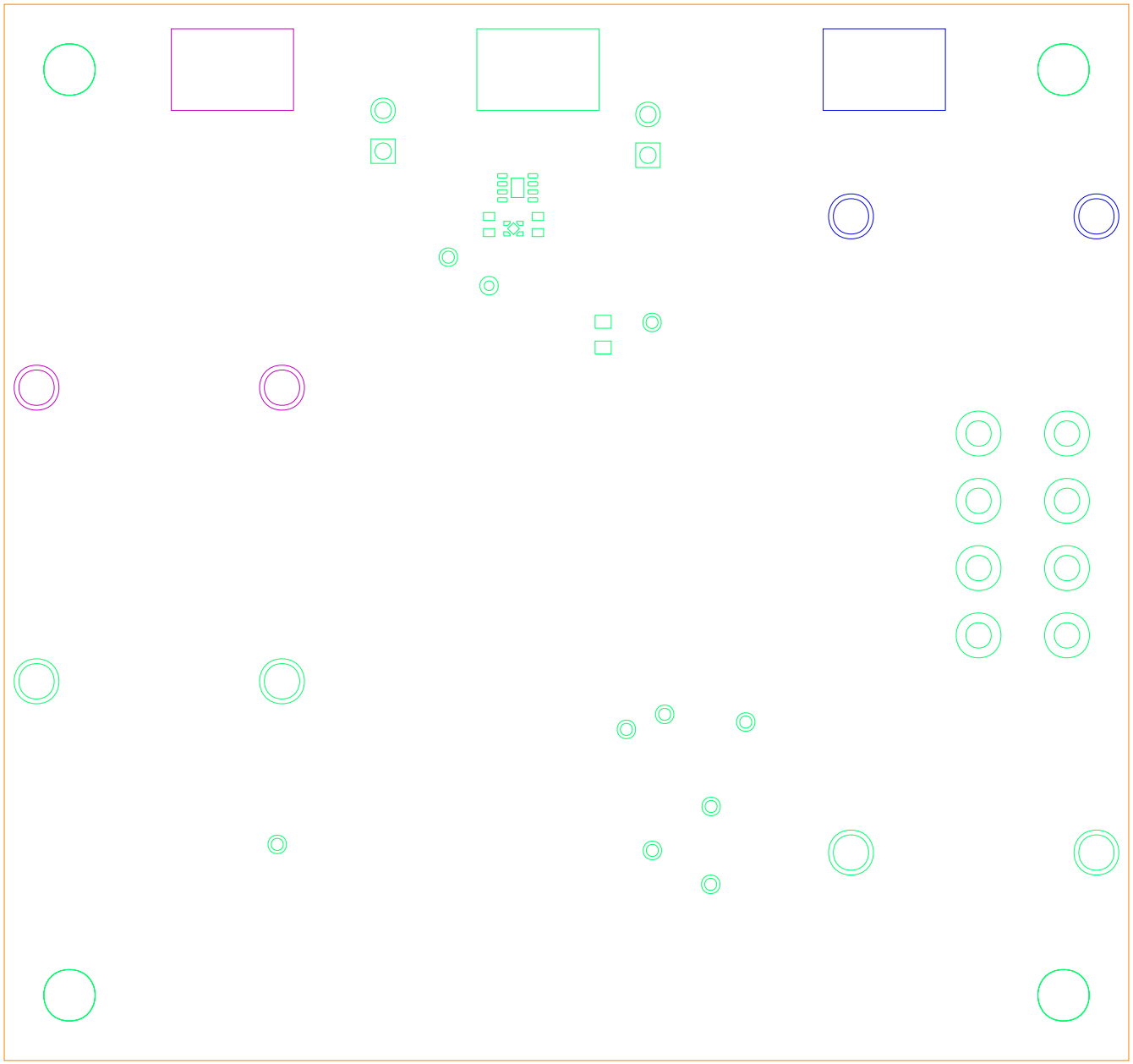
ON SEMICONDUCTOR

BU ENABLE XDFN LDO

SIZE	REVISION	DWG NO
A	REV1	ONSEC-18-016

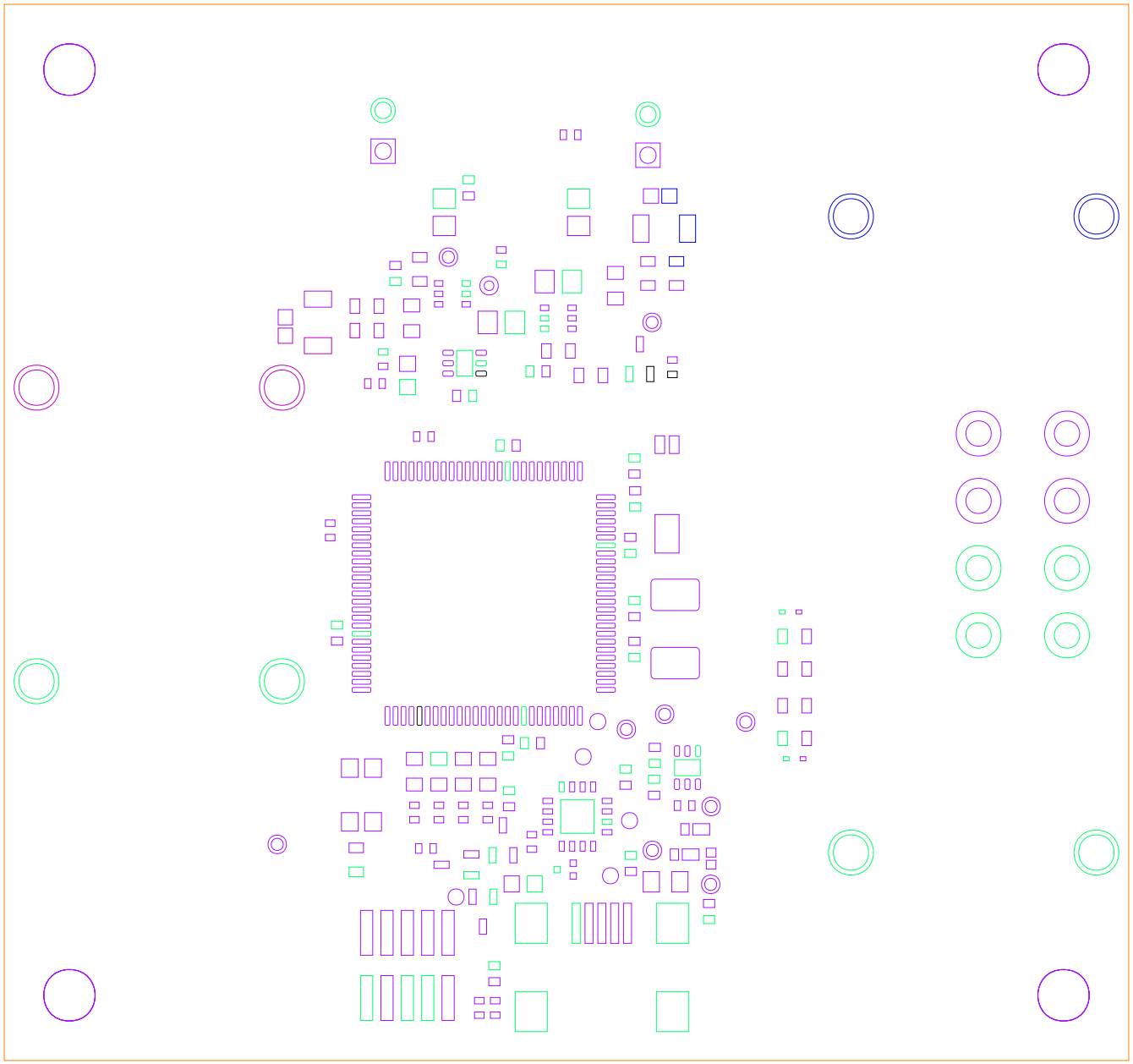
SCALE	DRAWING	SHEET
1/1	FABRICATION	1 OF 3

ART FILM - SMASKTOP



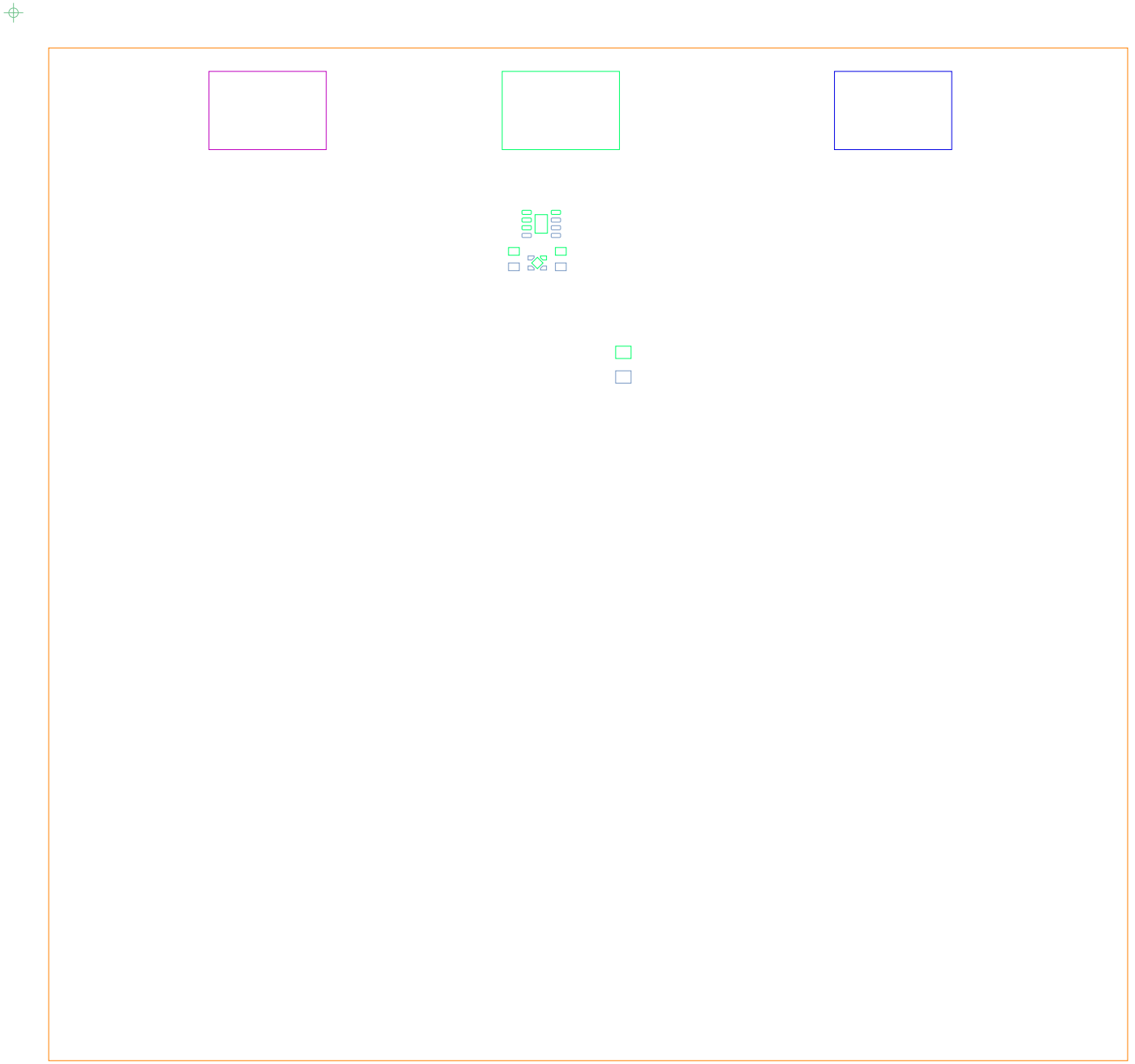
ART FILM - SMASKTOP

ART FILM - SMASKBOT



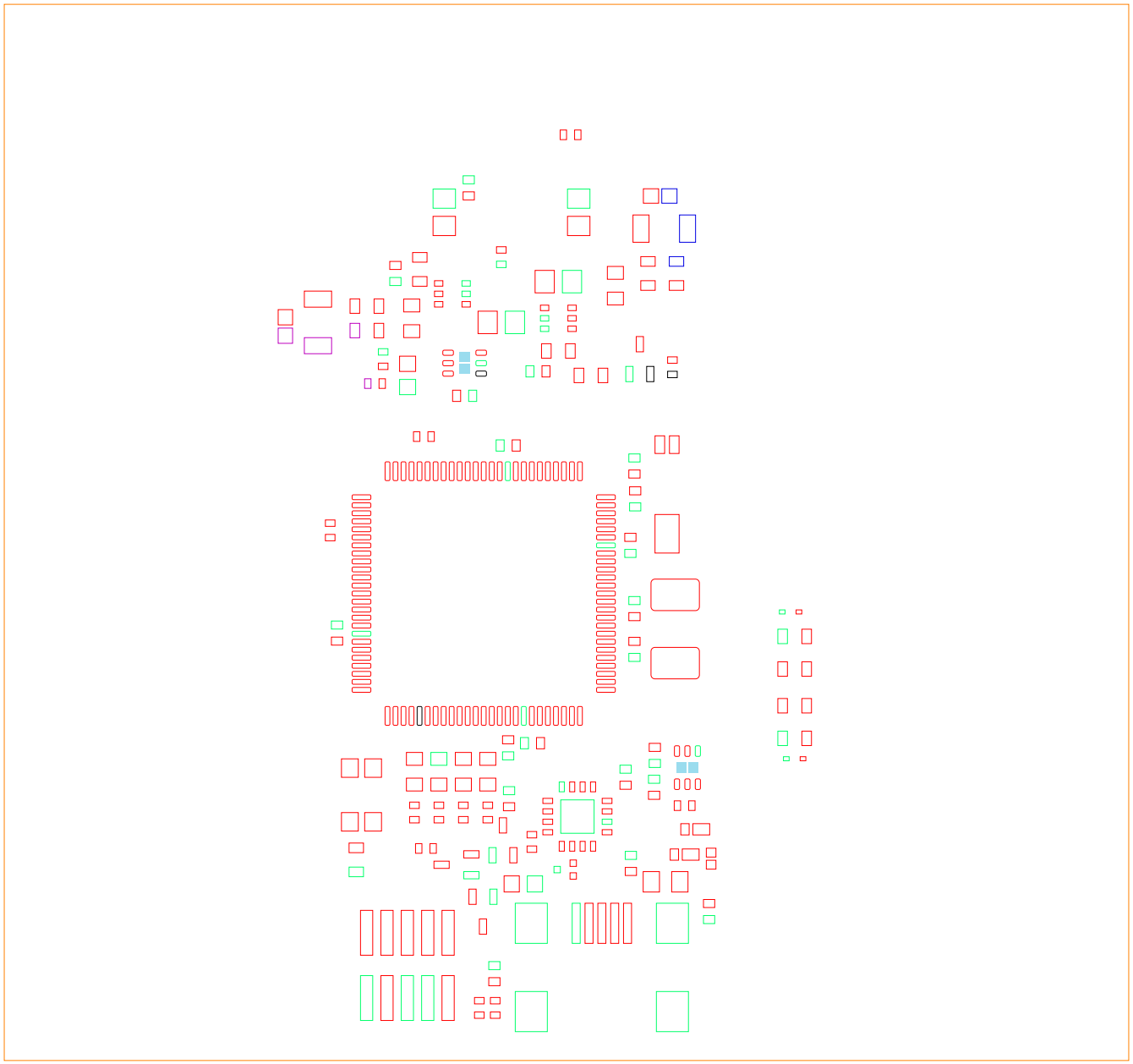
ART FILM - SMASKBOT

ART FILM - PMASKTOP

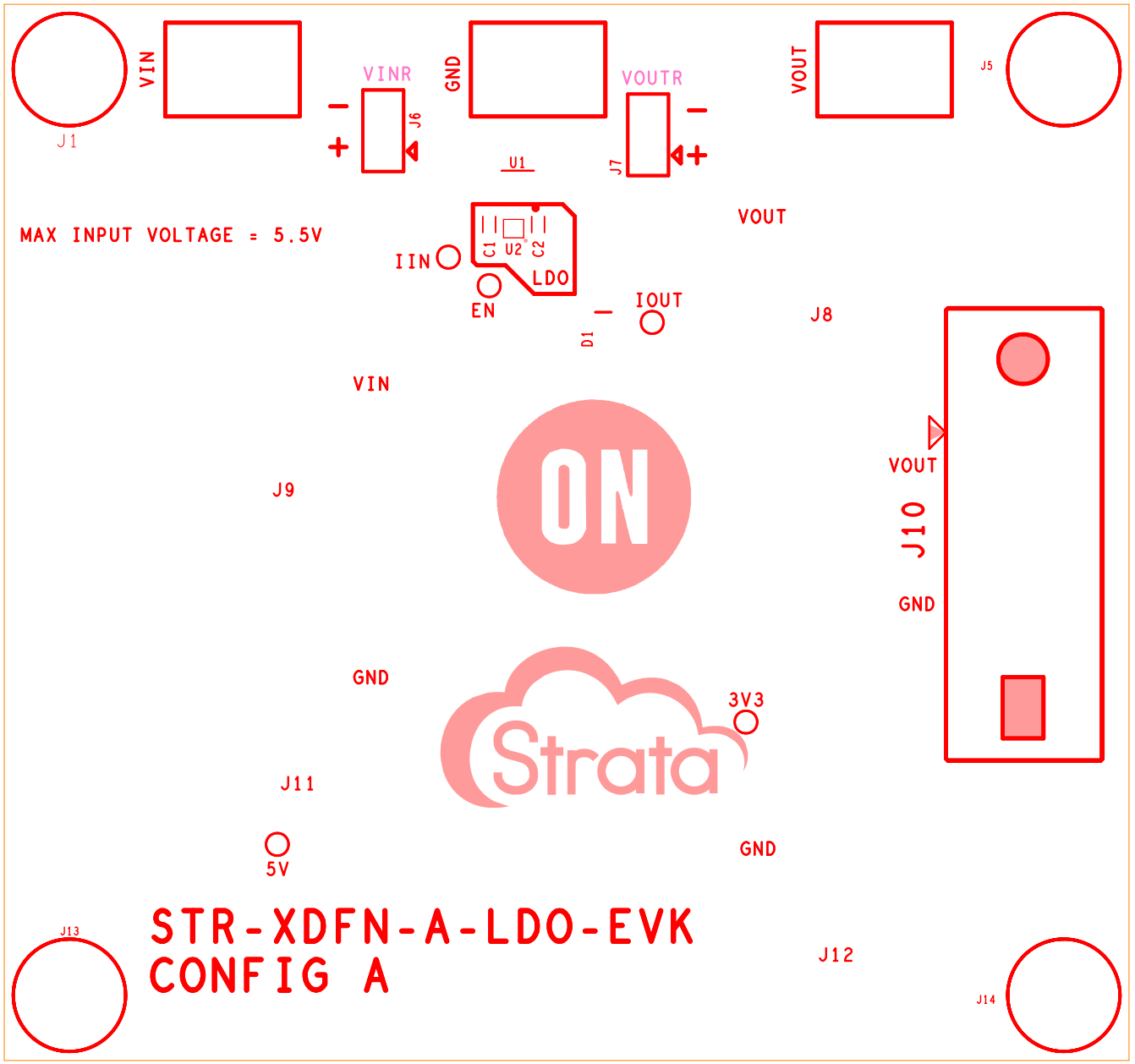


ART FILM - PMASKTOP

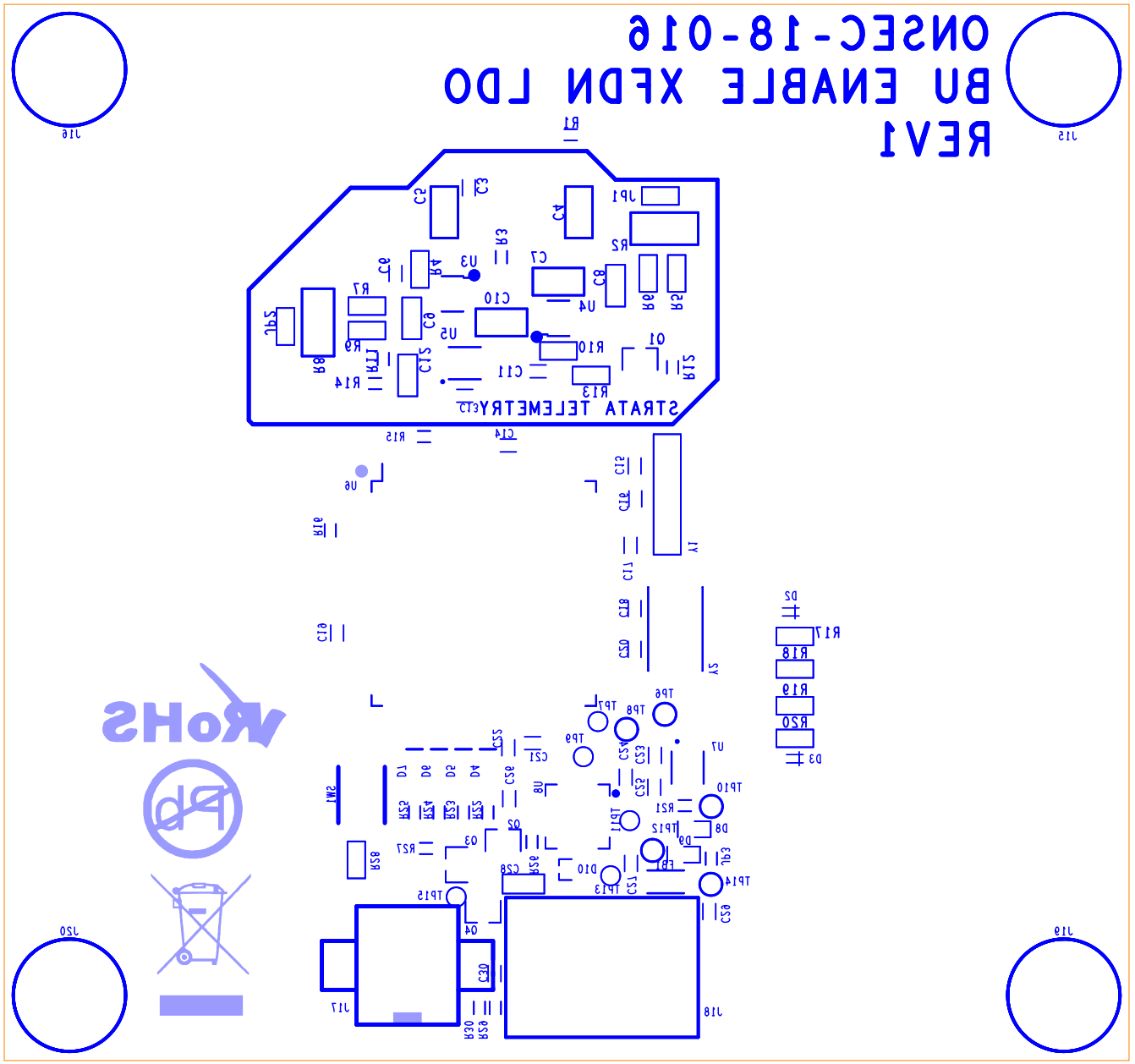
ART FILM - PMASKBOT

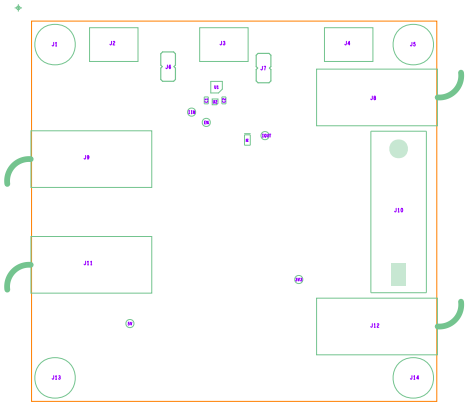


ART FILM - PMASKBOT



ART FILM - SILKTOP


ONSEC-18-016
BU ENABLE XFDN LDO
REV1
STRATA TELEMETRY



ASSEMBLY TOP NOTES (UNLESS OTHERWISE SPECIFIED):

1. ASSEMBLE AND INSPECT PER IPC-A-610 CLASS 3.
2. SOLDER, FLUX, AND ROHS TYPES SHOULD BE DEFINED IN QUOTATION FROM MANUFACTURER.
3. ~~IF BARE BOARDS ARE SUPPLIED BY ON SEMICONDUCTOR THEY WILL BE AN <ARRAY OR INDIVIDUAL PEICES>.~~
4. ONLY PARTS CONTAINED IN BILL OF MATERIALS SHALL USED FOR TURN-KEY ASSEMBLY UNLESS EQUIVALENT PART APPROVED BY ON SEMICONDUCTOR.
5. REMOVE ANY KAPTON TAPE COVERING COMPONENTS EXCEPT FOR IMAGE SENSORS WHERE IT SHOULD ONLY BE REMOVED IF LENS OR LENS HOLDER INTERFERE WITH KAPTON TAPE REMOVAL.
6. "DNI" REFERENCE IN BILL OF MATERIALS MEANS DO NOT INSTALL AND THESE PARTS ARE NOT REQUIRED FOR BOARD BUILD.
7. RETURN ALL CONSIGNED AND TURN-KEY UNASSEMBLED OR EXTRA COMPONENTS WITH ASSEMBLED PCBS.
8. REFLOW HEAT PROFILE IS REQUIRED BY ASSEMBLER TO ENSURE PROPER SOLDER ATTACH.
9. HIDDEN PINS SUCH AS BGA PACKAGES ARE REQUIRED TO BE X-RAY'ED FOR PROPER SOLDER ATTACH.
10. NO ARRAY MOUSE BITES ARE ALLOWED ON EDGE OF FINISHED PCB. USE PLUNGE ROUTER TO REMOVE AFTER ASSEMBLY.
11. SOLDERMASK BARREL RELIEF TO AVOID ASSEMBLY ISSUES ON LARGE SURFACE MOUNT PADS IS ACCEPTABLE.
12. IF ASSEMBLY BOTTOM NOTES ARE NOT FOUND USE TOP NOTES.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	SEMICONDUCTOR			
DIMENSIONS ARE IN MILS TOLERANCES ON:	DRAWN: MICHAEL OATMAN	01/29/19	BU ENABLE XDFN LDO			
	CHECKED: MICHAEL OATMAN	01/29/19				
	ENGRG: MICHAEL OATMAN	01/29/19				
	ISSUED: MICHAEL OATMAN	01/29/19	SIZE A	REVISION REV1	DWG NO ONSEC-18-016	
			SCALE 1/1	DRAWING ASSEMBLY TOP	SHEET 2 OF 3	

ASSEMBLY BOTTOM NOTES (UNLESS OTHERWISE SPECIFIED):
1. USE ASSEMBLY TOP NOTES.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN MILS TOLERANCES ON:	DRAWN: MICHAEL OATMAN	01/29/19
	CHECKED: MICHAEL OATMAN	01/29/19
	ENGR: MICHAEL OATMAN	01/29/19
	ISSUED: MICHAEL OATMAN	01/29/19

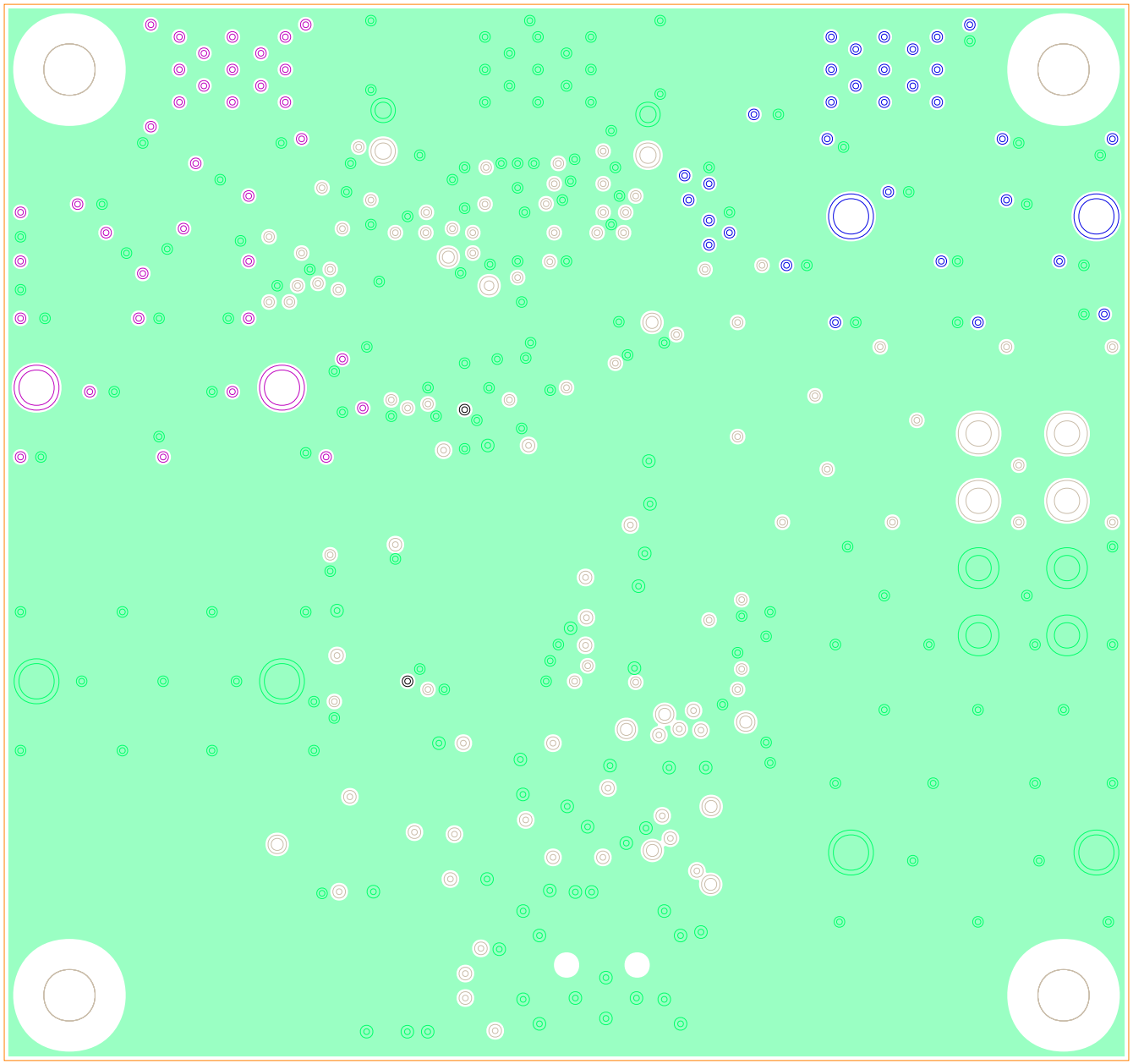
SEMICONDUCTOR

BU ENABLE XDFN LDO

SIZE	REVISION	DWG NO
A	REV1	ONSEC-18-016

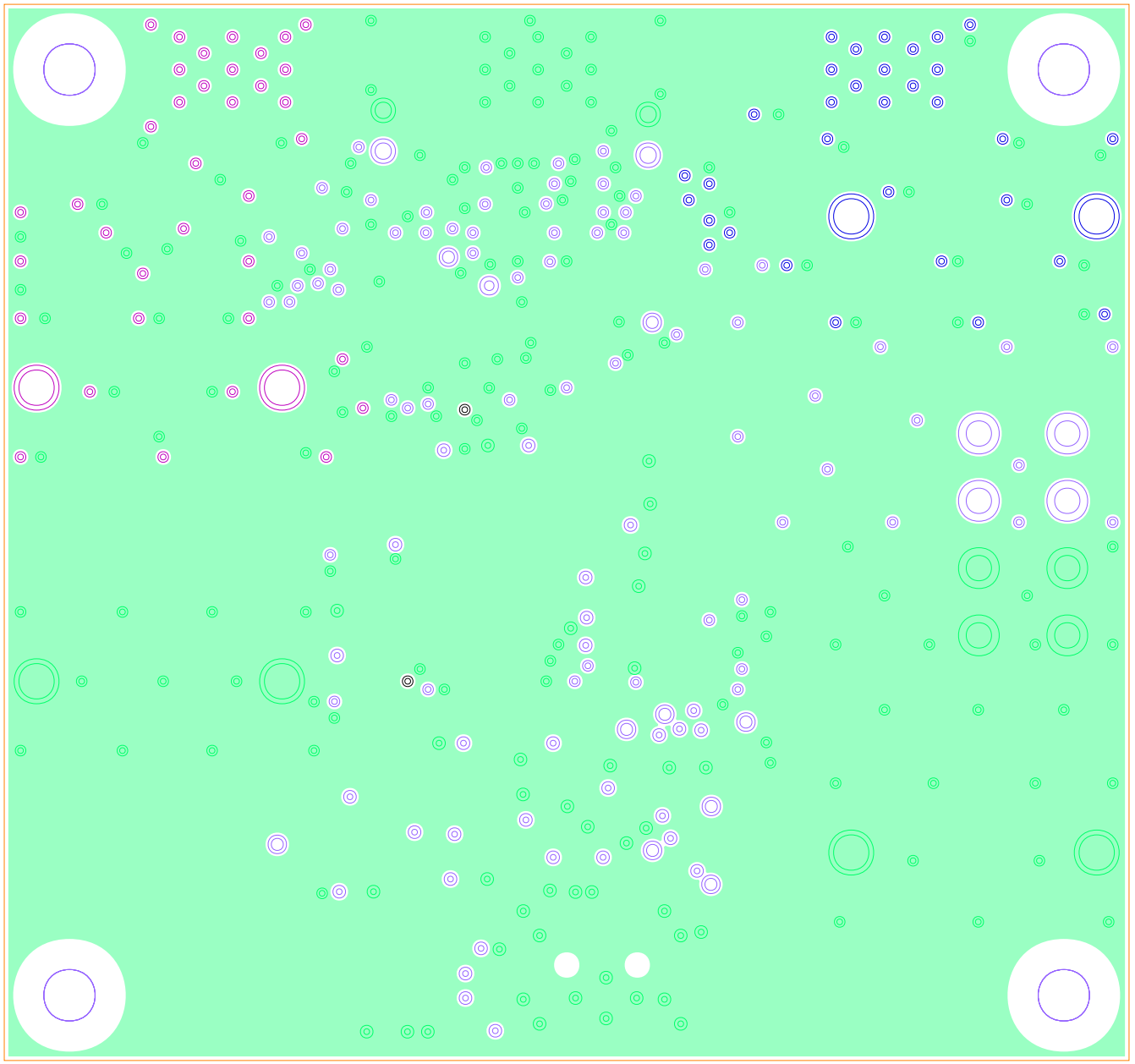
SCALE	DRAWING	SHEET
1/1	ASSEMBLY BOTTOM	3 OF 3

ART FILM - L2



ART FILM - L2

ART FILM - L3



ART FILM - L3