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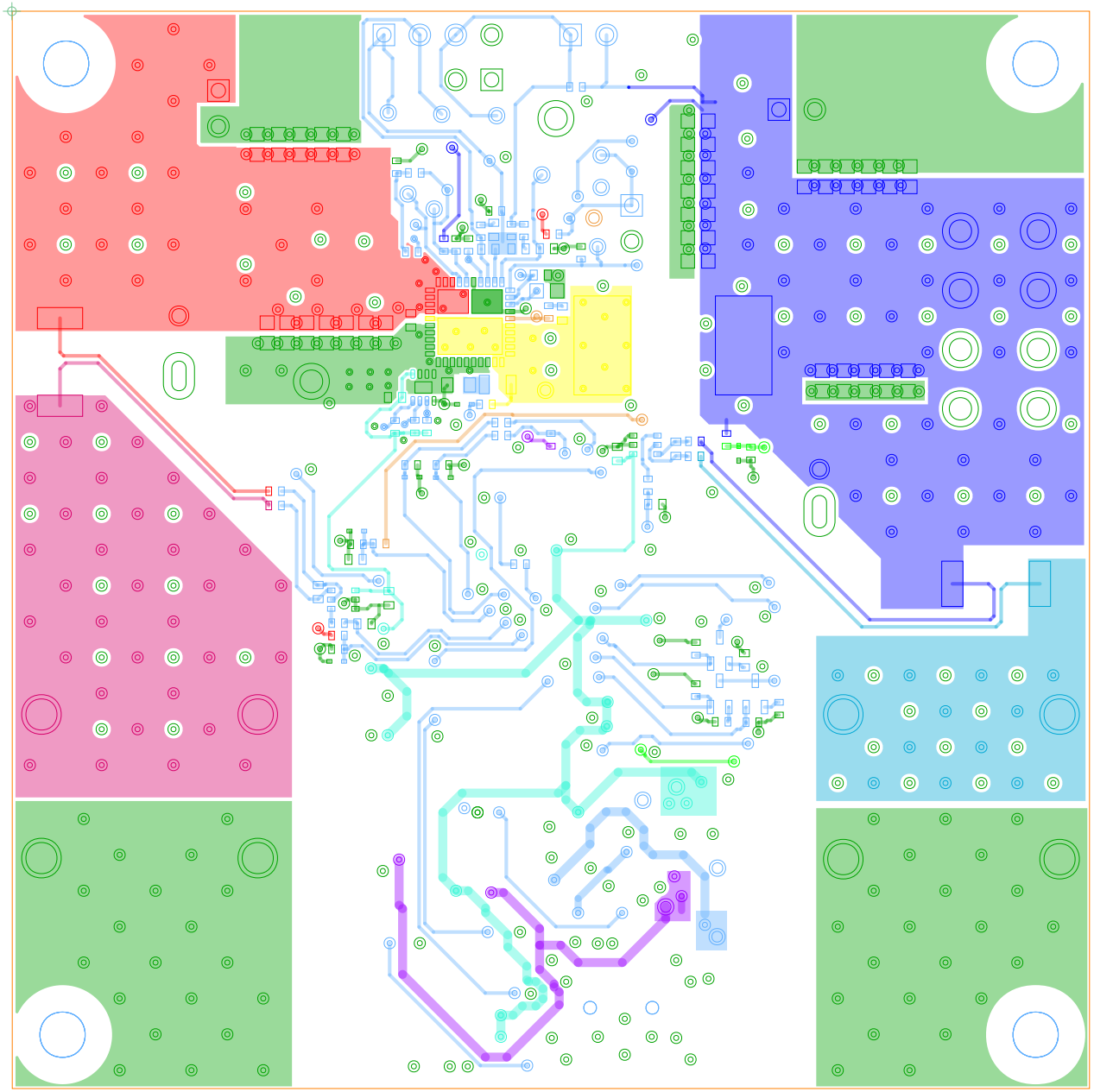
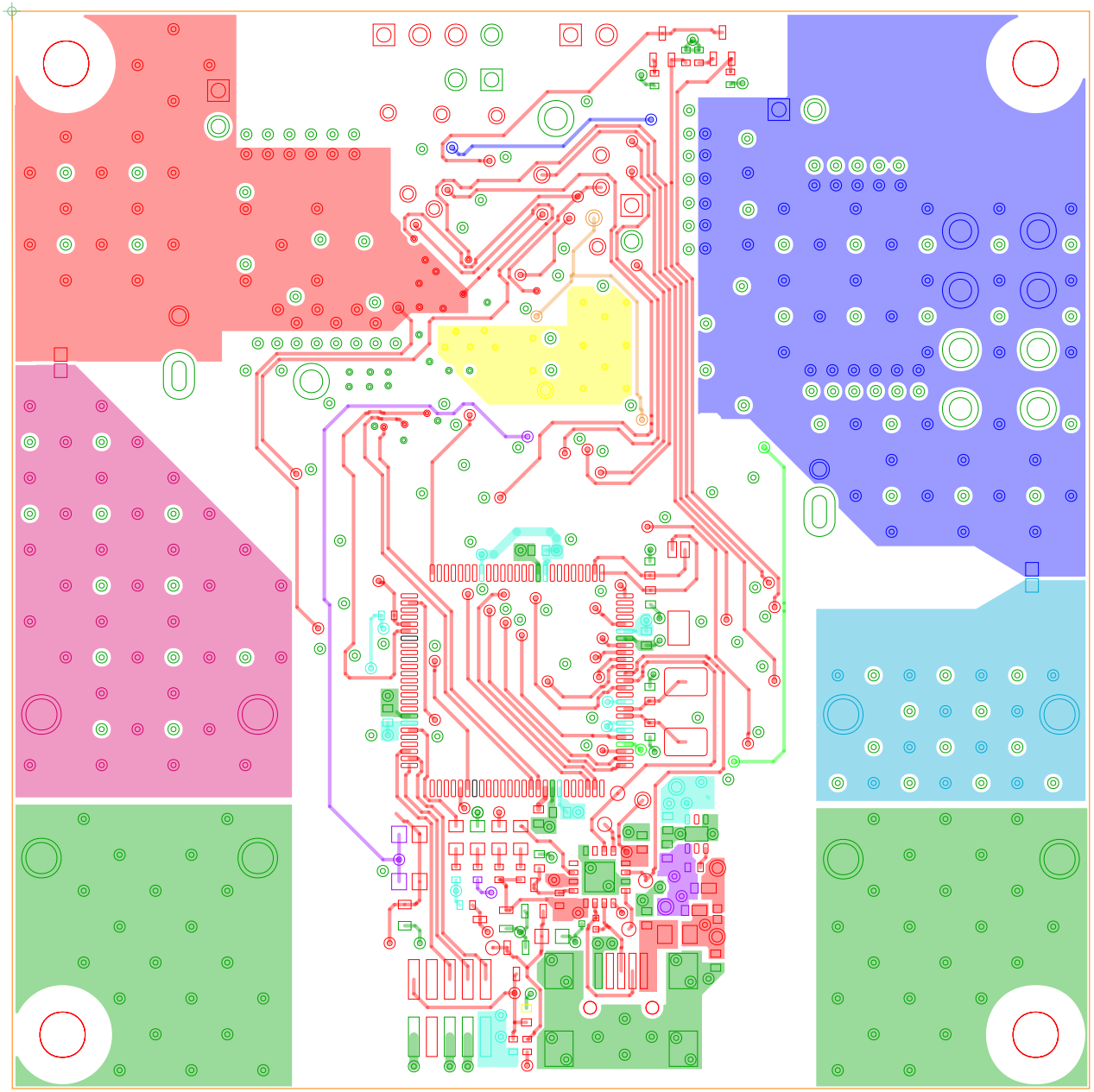


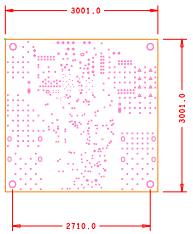
ART FILM - TOP

ART FILM - BOTTOM



ART FILM - BOTTOM

ART FILE - Fab



DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	QTY
·	10.0	-	+2.0/-6.0	-	PLATED	41
·	14.0	-	+2.0/-6.0	-	PLATED	148
·	14.0	-	+2.0/-6.0	-	PLATED	84
+	29.5	-	+2.0/-2.0	-	PLATED	16
+	40.0	-	+2.0/-2.0	-	PLATED	2
+	40.0	-	+2.0/-2.0	-	PLATED	14
^	62.0	-	+0.0/-0.0	-	PLATED	8
o	63.0	-	+2.0/-2.0	-	PLATED	2
O	86.6	-	+3.9/-3.9	-	PLATED	8
+	35.4	-	+2.0/-2.0	-	NON-PLATED	2
◯	126.0	-	+4.0/-4.0	-	NON-PLATED	8
▯	82.7x39.4	90.000	+0.0/-0.0	+4.0/-4.0	PLATED	1
▯	90.6x39.4	90.000	+0.0/-0.0	+4.0/-4.0	PLATED	1

STACKUP TABLE				
Unit = Mils				
#	NAME	TYPE	MATERIAL	THICKNESS
		SURFACE	AIR	0
1	TOP	CONDUCTOR	COPPER	1.7
		DIELECTRIC	FR-4	11.9
2	L2	PLANE	COPPER	1.4
		DIELECTRIC	FR-4	28
3	L3	PLANE	COPPER	1.4
		DIELECTRIC	FR-4	11.9
4	BOTTOM	CONDUCTOR	COPPER	1.7
		SURFACE	AIR	0
		TOTAL THICKNESS		58

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED):
IMPORT NOTES FROM Templates/notes/fab.txt

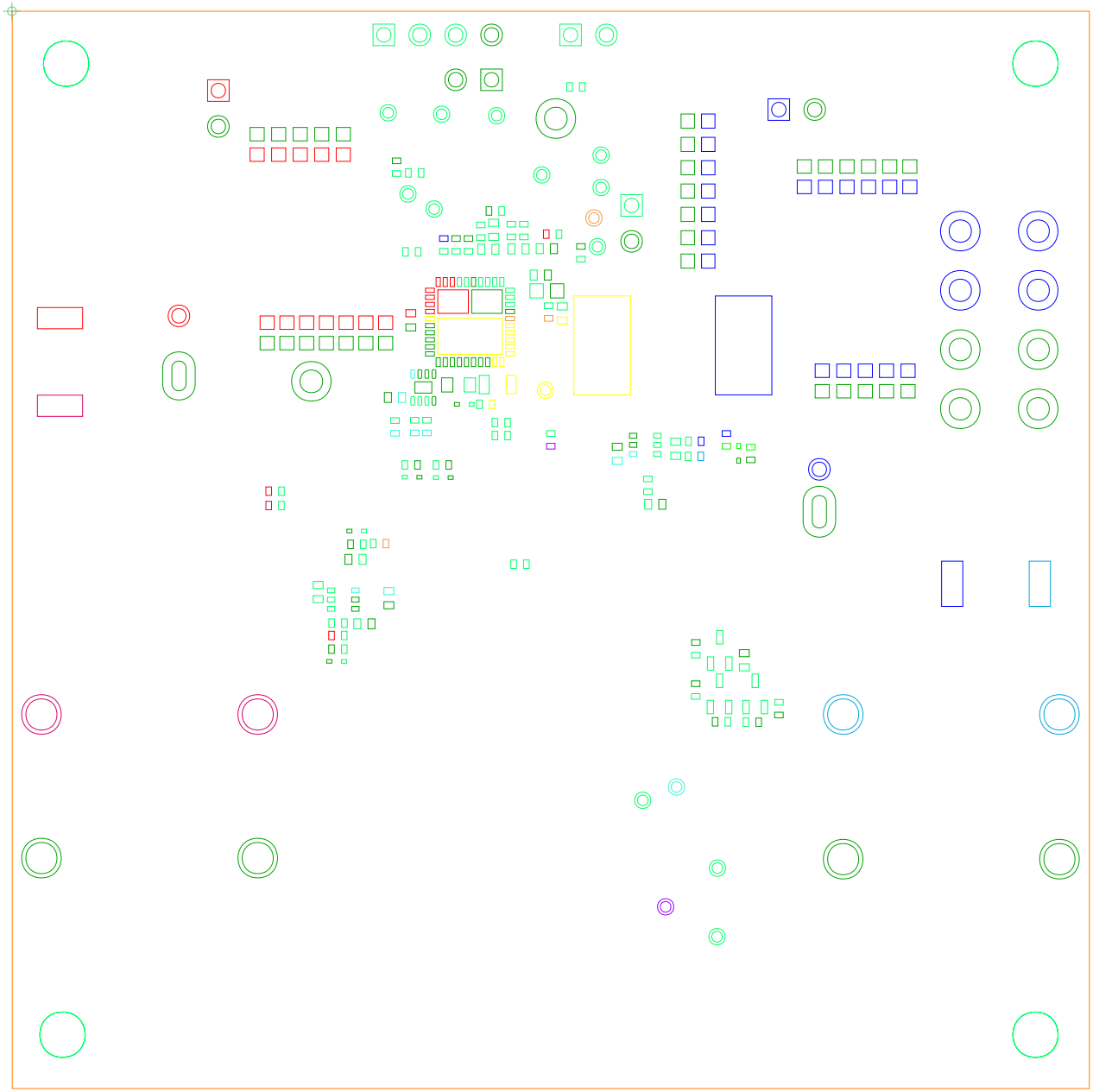
NOTES (UNLESS OTHERWISE SPECIFIED):

1. BUILD IN ACCORDANCE WITH IPC 4011, IPC 6012, OR IPC 6013 DEPENDANT ON TYPE OF PRINTED CIRCUIT BOARD, CLASS 2.
2. LAMINATE MATERIAL SHALL MEET THE REQUIREMENTS OF IPC 4101 TYPE 370HR PER STACKUP DETAIL OR EQUIVALENT. (NOMINAL DIELECTRIC THICKNESS WITHIN +/- 10% OF STACKUP DETAIL).
3. FINISH: ENIG 2 MICRO-INCHES MINIMUM OF GOLD OVER 118-236 MICRO-INCHES OF NICKEL.
4. TOP SIDE SHOWN.
5. HOLE DIAMETERS ARE AFTER PLATING, 0.8 MIL AVERAGE.
6. SILKSCREEN BOTH SIDES USING EPOXY OR ACRYLIC BASED WHITE NON-CONDUCTIVE SILKSCREEN. NOTE: LEGEND SHOULD BE REMOVED FROM ANY CONDUCTIVE SURFACE UNLESS OTHERWISE SPECIFIED. NO SILKSCREEN ON PADS.
7. <ETCH, SILK> VENDOR ID, UL DESIGNATION, AND DATECODE ON THE BACKSIDE.
8. SOLDER MASK BOTH SIDES GREEN USING LIQUID PHOTO IMAGEABLE METHOD. NO SOLDERMASR ON PADS.
9. IMPEDANCE REQUIREMENTS ARE AS FOLLOWS +/- 10%
   IF PRESENT, ALL OUTER 0.65 MIL WIDE TRACES 50 OHM SINGLE ENDED.
   IF PRESENT, ALL INNER 5.65 MIL WIDE TRACES 50 OHM SINGLE ENDED.
   TRACE WIDTHS SHALL NOT BE MODIFIED WITHOUT APPROVAL FROM ON SEMICONDUCTOR.
10. ALL ARTWORK AND DESIGN MEDIA SHALL BE SPECIFIED BY ON SEMICONDUCTOR. NO CHANGES WILL BE ALLOWED WITHOUT SPECIFIC APPROVAL FROM ON SEMICONDUCTOR.
11. TOOLING HOLES ARE TO BE DRILLED AWAY AT THE SAME TIME AS OTHER HOLES.
12. ALL MATERIALS ARE TO BE ROHS AND WEE COMPLIANT.
13. LAYER STACKUP INFORMATION INCLUDED IN THIS DRAWING SHOWS OUTER LAYER THICKNESS AFTER PLATING AND SUPERSEDES ANY OTHER DESIGN DOCUMENTATION.
14. ELECTRICALLY DISCONNECTED COPPER THIEVING IS ACCEPTABLE TO HELP MAINTAIN COPPER PLATING DISTRIBUTION IN LOW PRESSURE AREAS TO AVOID DELAMINATION.
15. REMOVAL OF NON-FUNCTIONAL PADS ON INNER LAYERS IS ACCEPTABLE.
16. DO NOT PROVIDE BOARDS IN ARRAY FORMAT. ARRAYS SHOULD HAVE MINIMUM OF 250 MILS ON ALL SIDES.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	SEMICONDUCTOR	
DIMENSIONS ARE IN MILS	DRAWN: Ryan Johnson	1/16/19		
TOLERANCES ON:	CHECKED: Ryan Johnson	1/16/19	BU Enable 15A Switcher	
	ENGRG: Ryan Johnson	1/16/19		
	ISSUED: Ryan Johnson	1/16/19	SIZE: D	REVISION: REV1
			DWG NO: ONSEC-18-017	
			SCALE: 1/1	DRAWING: FABRICATION
			SHEET: 1 OF 3	

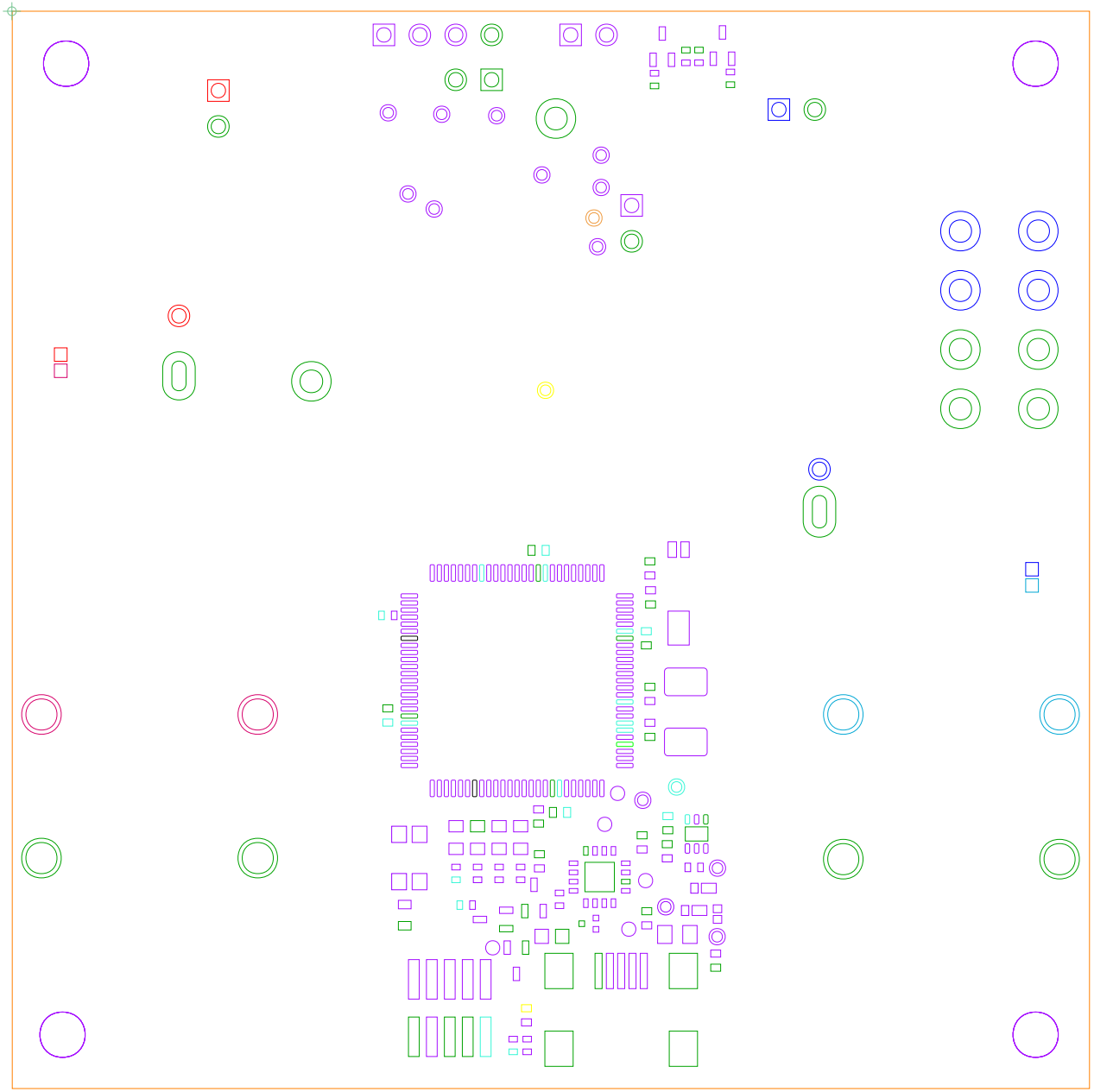
ART FILE - Fab

ART FILM - SMASKTOP



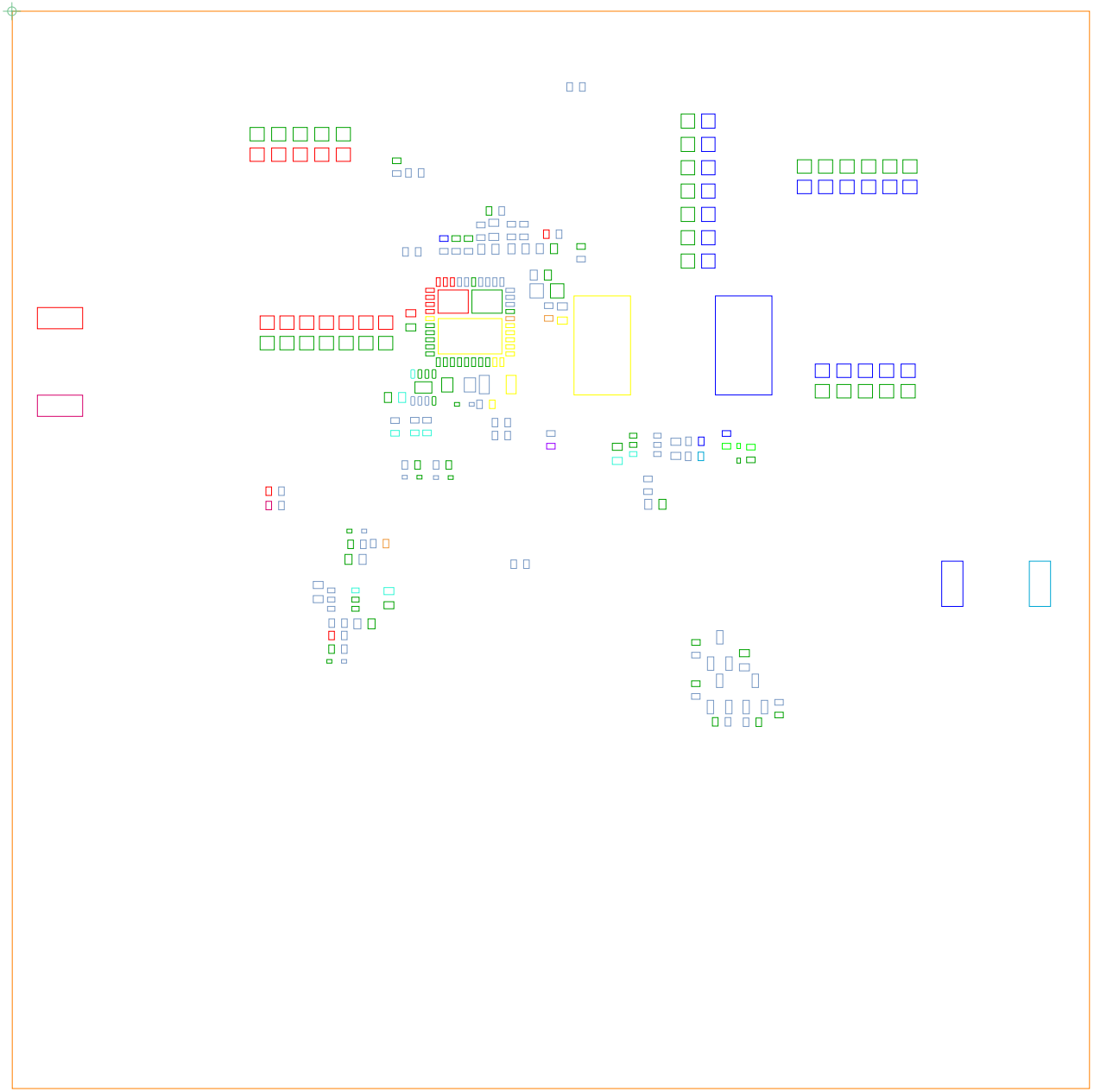
ART FILM - SMASKTOP

ART FILM - SMASKBOT



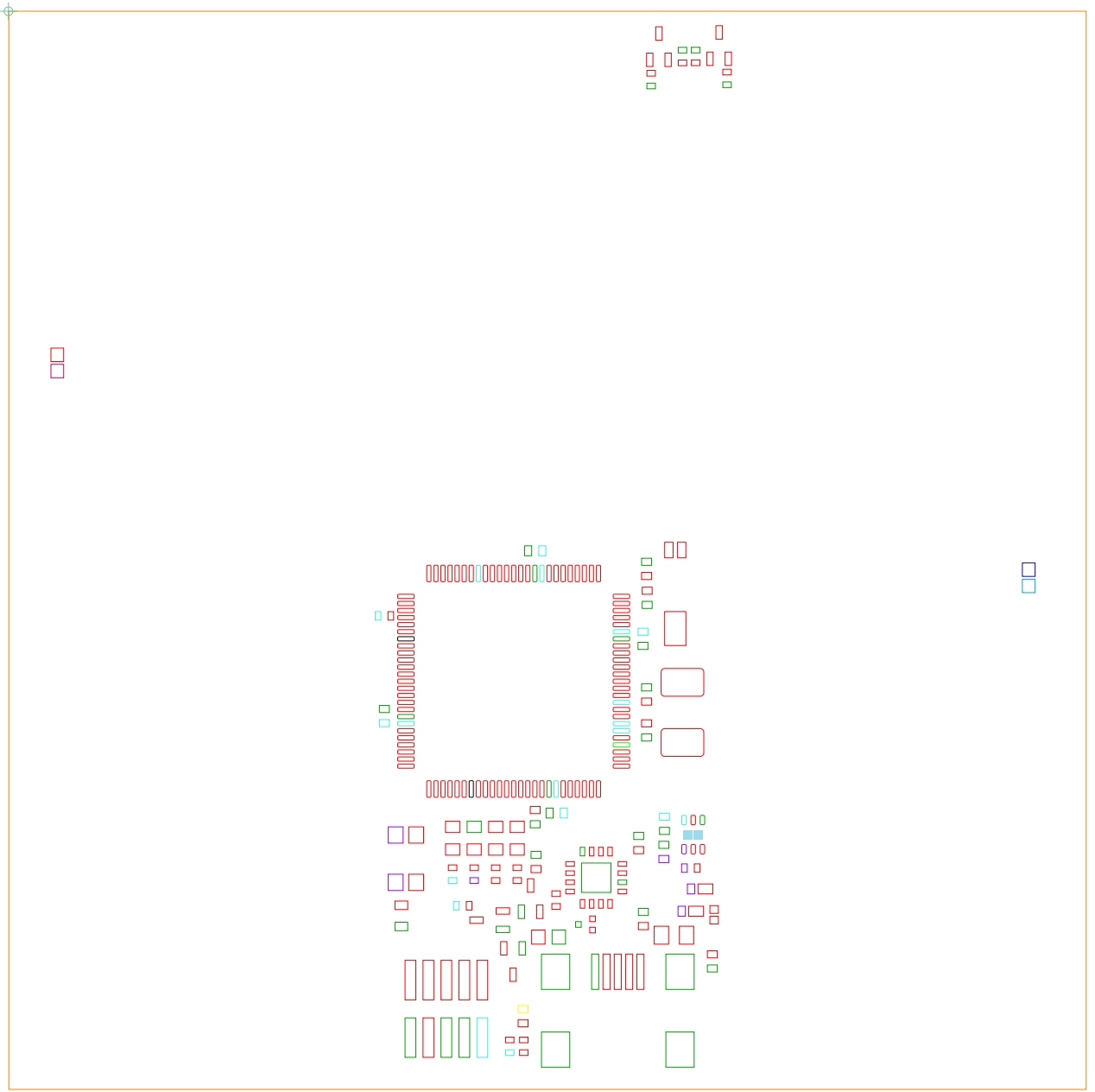
ART FILM - SMASKBOT

ART FILM - PMASKTOP

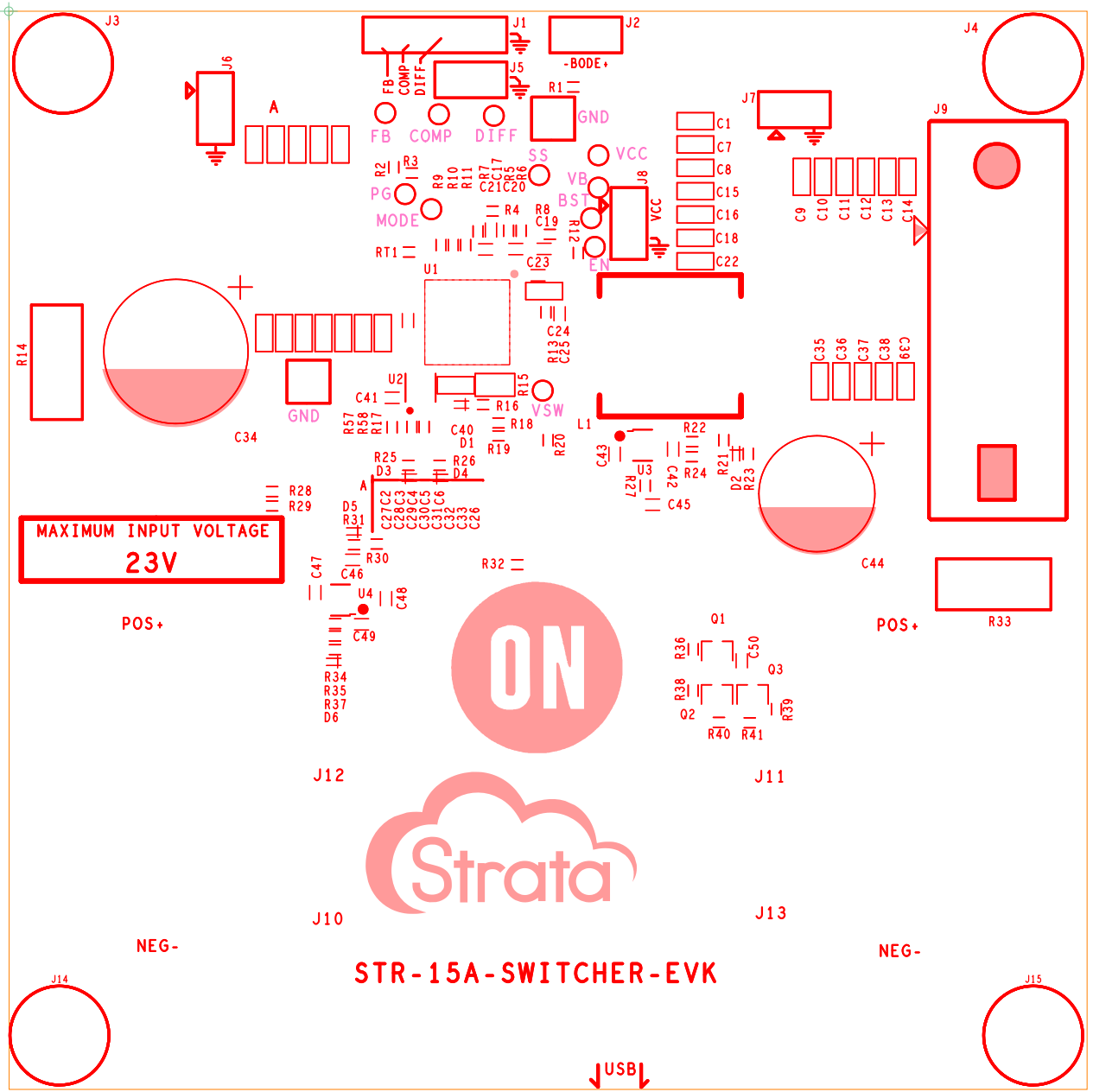


ART FILM - PMASKTOP

ART FILM - PMASKBOT



ART FILM - PMASKBOT


MAXIMUM INPUT VOLTAGE
23V
POS+
NEG-
POS+
NEG-
STR-15A-SWITCHER-EVK
USB
FB
COMP
DIFF
GND
SS
VCC
VB
BST
PG
MODE
EN
VSW
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
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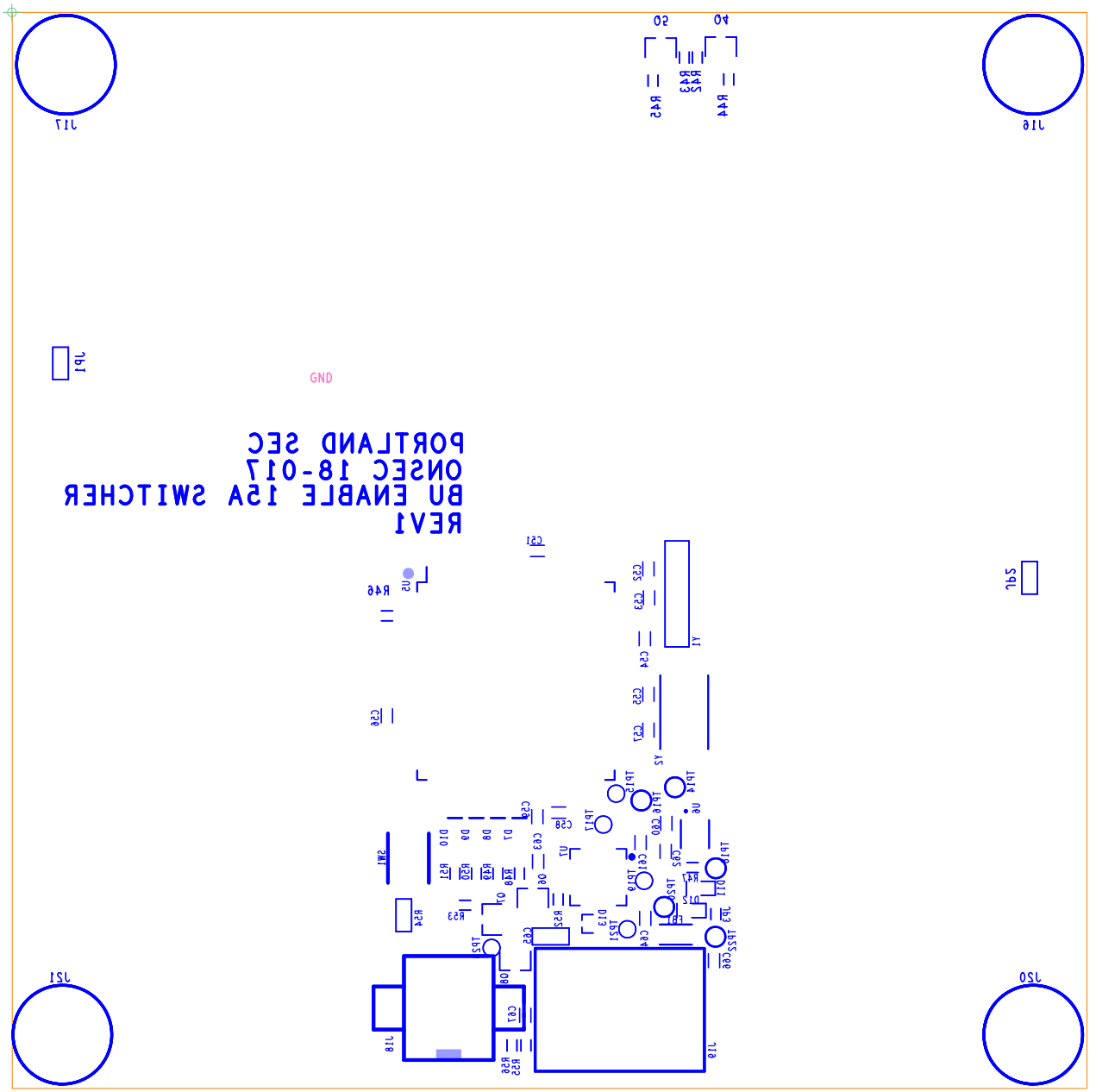
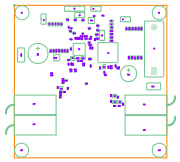
D2
D3
D4
D5
D6
L1
-BODE+


PORTLAND SEC
ONSEC 18-017
BU ENABLE 15A SWITCHER
REV1
GND



ASSEMBLY TOP NOTES (UNLESS OTHERWISE SPECIFIED):
IMPORT NOTES FROM Templates/notes/assytop.txt

ASSEMBLY TOP NOTES (UNLESS OTHERWISE SPECIFIED):

1. ASSEMBLE AND INSPECT PER IPC-A-610 CLASS 3.
2. SOLDER, FLUX, AND ROHS TYPES SHOULD BE DEFINED IN QUOTATION FROM MANUFACTURER.
3. IF BARE BOARDS ARE SUPPLIED BY ON SEMICONDUCTOR THEY WILL BE IN CARRIER OR INDIVIDUAL PETCES>.
4. ONLY PARTS CONTAINED IN BILL OF MATERIALS SHALL USED FOR TURN-KEY ASSEMBLY UNLESS EQUIVALENT PART APPROVED BY ON SEMICONDUCTOR.
5. REMOVE ANY KAPTON TAPE COVERING COMPONENTS EXCEPT FOR IMAGE SENSORS WHERE IT SHOULD ONLY BE REMOVED IF LENS OR LENS HOLDER INTERFERE WITH KAPTON TAPE REMOVAL.
6. "DNI" REFERENCE IN BILL OF MATERIALS MEANS DO NOT INSTALL AND THESE PARTS ARE NOT REQUIRED FOR BOARD BUILD.
7. RETURN ALL CONSIGNED AND TURN-KEY UNASSEMBLED OR EXTRA COMPONENTS WITH ASSEMBLED PCBS.
8. REFLOW HEAT PROFILE IS REQUIRED BY ASSEMBLER TO ENSURE PROPER SOLDER ATTACH.
9. HIDDEN PINS SUCH AS BGA PACKAGES ARE REQUIRED TO BE X-RAY'ED FOR PROPER SOLDER ATTACH.
10. NO ARRAY MOUSE BITES ARE ALLOWED ON EDGE OF FINISHED PCB. USE PLUNGE ROUTER TO REMOVE AFTER ASSEMBLY.
11. SOLDERMASK BARREL RELIEF TO AVOID ASSEMBLY ISSUES ON LARGE SURFACE MOUNT PADS IS ACCEPTABLE.
12. IF ASSEMBLY BOTTOM NOTES ARE NOT FOUND USE TOP NOTES.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	SEMICONDUCTOR	
DIMENSIONS ARE IN MILS	DRAWN: Ryan Johnson	1/16/19	BU Enable 15A Switcher	
TOLERANCES ON:	CHECKED: Ryan Johnson	1/16/19		
	ENGRG: Ryan Johnson	1/16/19	SIZE: D	REVISION: REV1
	ISSUED: Ryan Johnson	1/16/19	DWG NO: ONSEC-18-017	
			SCALE: 1/1	DRAWING: ASSEMBLY TOP
				SHEET: 2 OF 3

ASSEMBLY BOTTOM NOTES (UNLESS OTHERWISE SPECIFIED):
IMPORT NOTES FROM Templates/notes/assybot.txt

ASSEMBLY BOTTOM NOTES (UNLESS OTHERWISE SPECIFIED):
1. USE ASSEMBLY TOP NOTES.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN MILS	DRAWN: Ryan Johnson	01/28/19
TOLERANCES ON:	CHECKED: Ryan Johnson	01/28/19
	ENGR: Ryan Johnson	01/28/19
	APPROVED: Ryan Johnson	01/28/19
	MFG:	

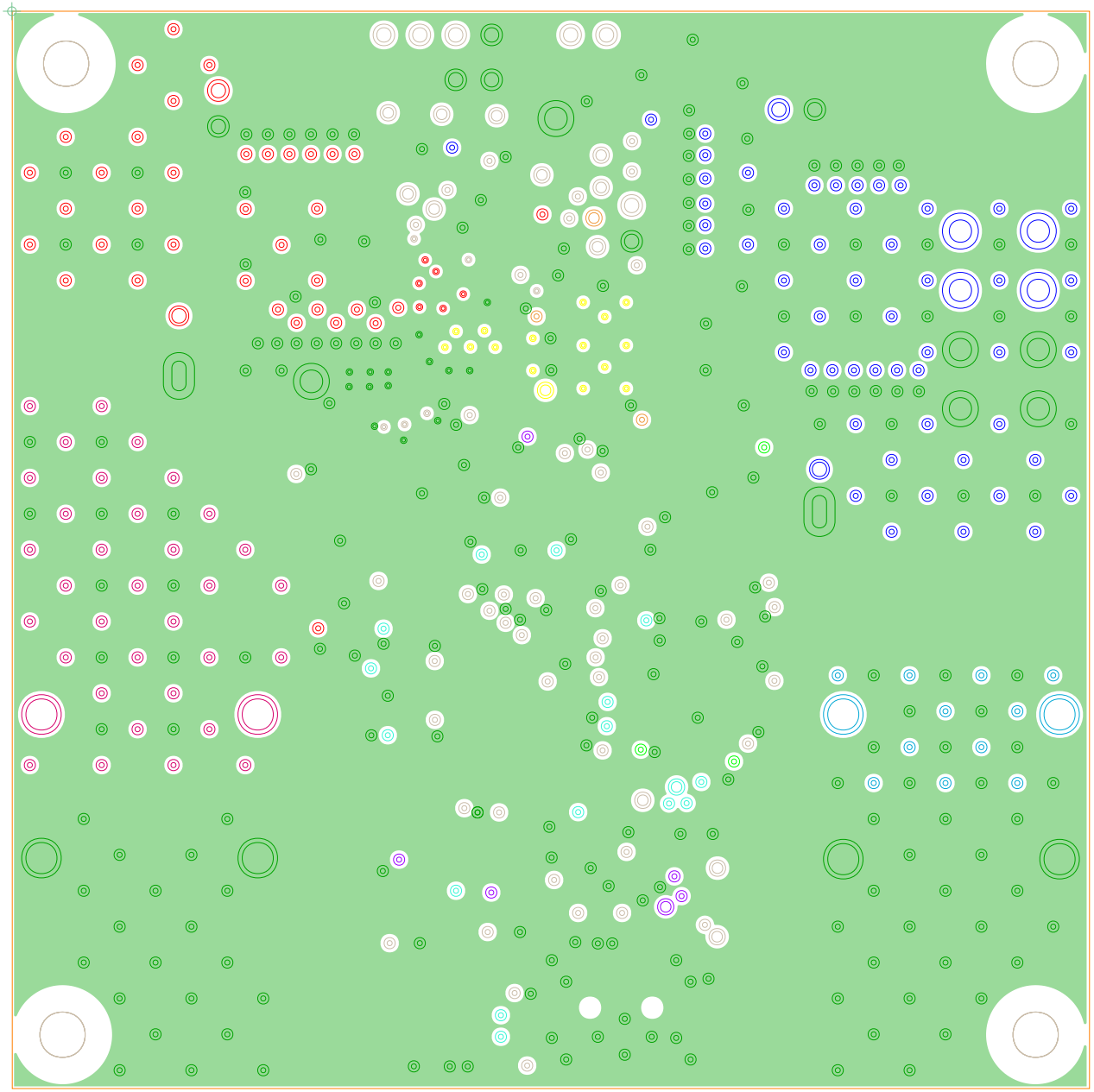
SEMICONDUCTOR

8U Enable 15A Switcher

SIZE	DWG NO	REV
D	ONSEC-18-017	

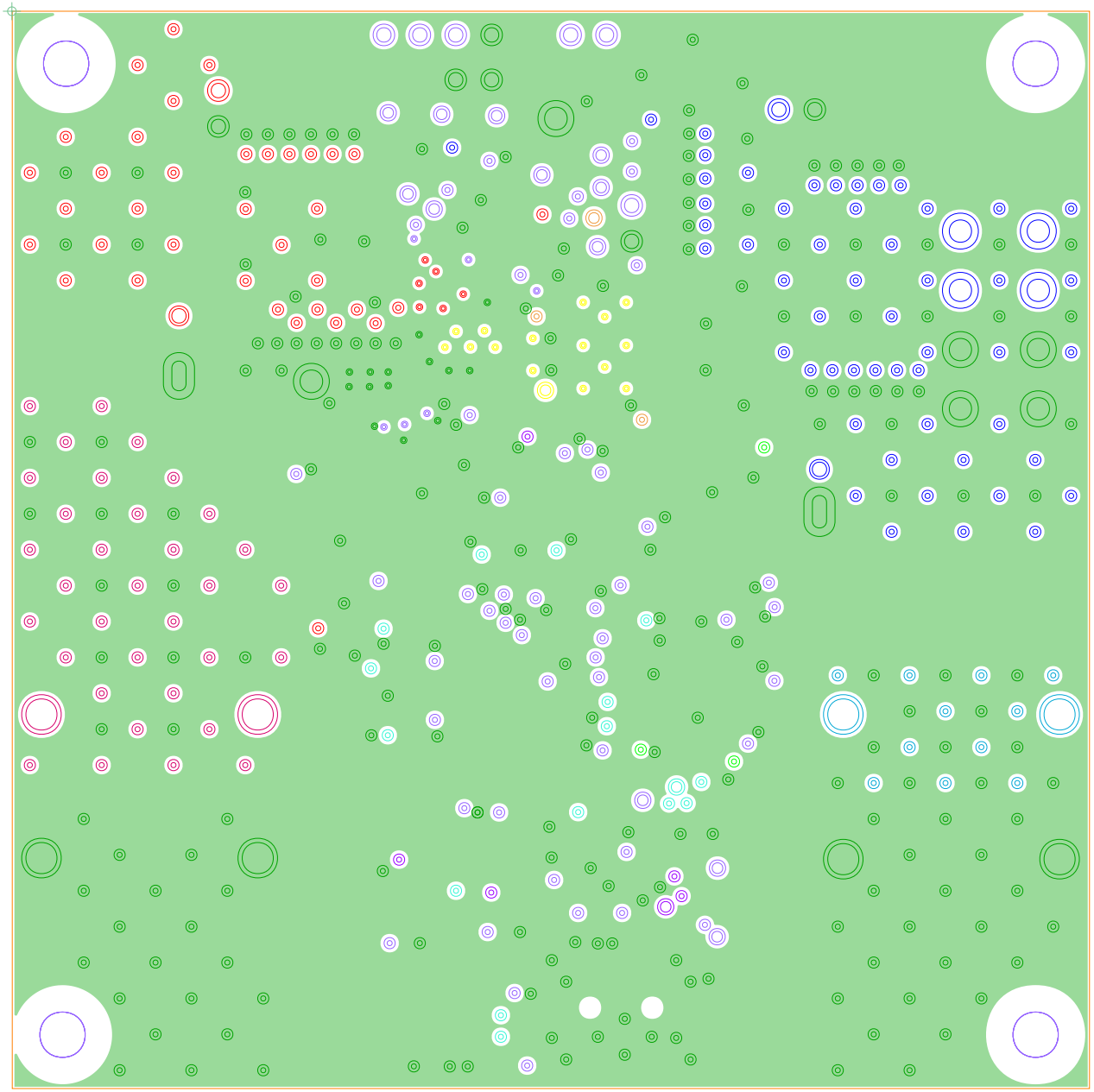
SCALE	DRAWING	SHEET
1\1	ASSEMBLY BOTTOM	3 OF 3

ART FILM - L2



ART FILM - L2

ART FILM - L3



ART FILM - L3