FDMF5833 Compact Thermal Model construction

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Compact model process:

1. FDMF5833 is a three-die device, so we need a three-input model
2. Build full 3D Finite Element Model (FEM)
3. Exercise model with individual die heat sources to locate leads with closest thermal connections to each of the die
   a. Boundary conditions for this exercise
      i. Die power inputs
      ii. Free convection from exposed surfaces (package and PCB)
4. Using leads identified in step 3, re-run simulations using those leads as fixed-temperature boundary constraints to generate a linear model with 3 Pd's, 3 lead temps, and 1 ambient as independent variables
5. Verify that linear model derived in step 4 "predicts" junction temperatures of step 2 given lead temperatures from step 2
6. Convert linear model into resistor network

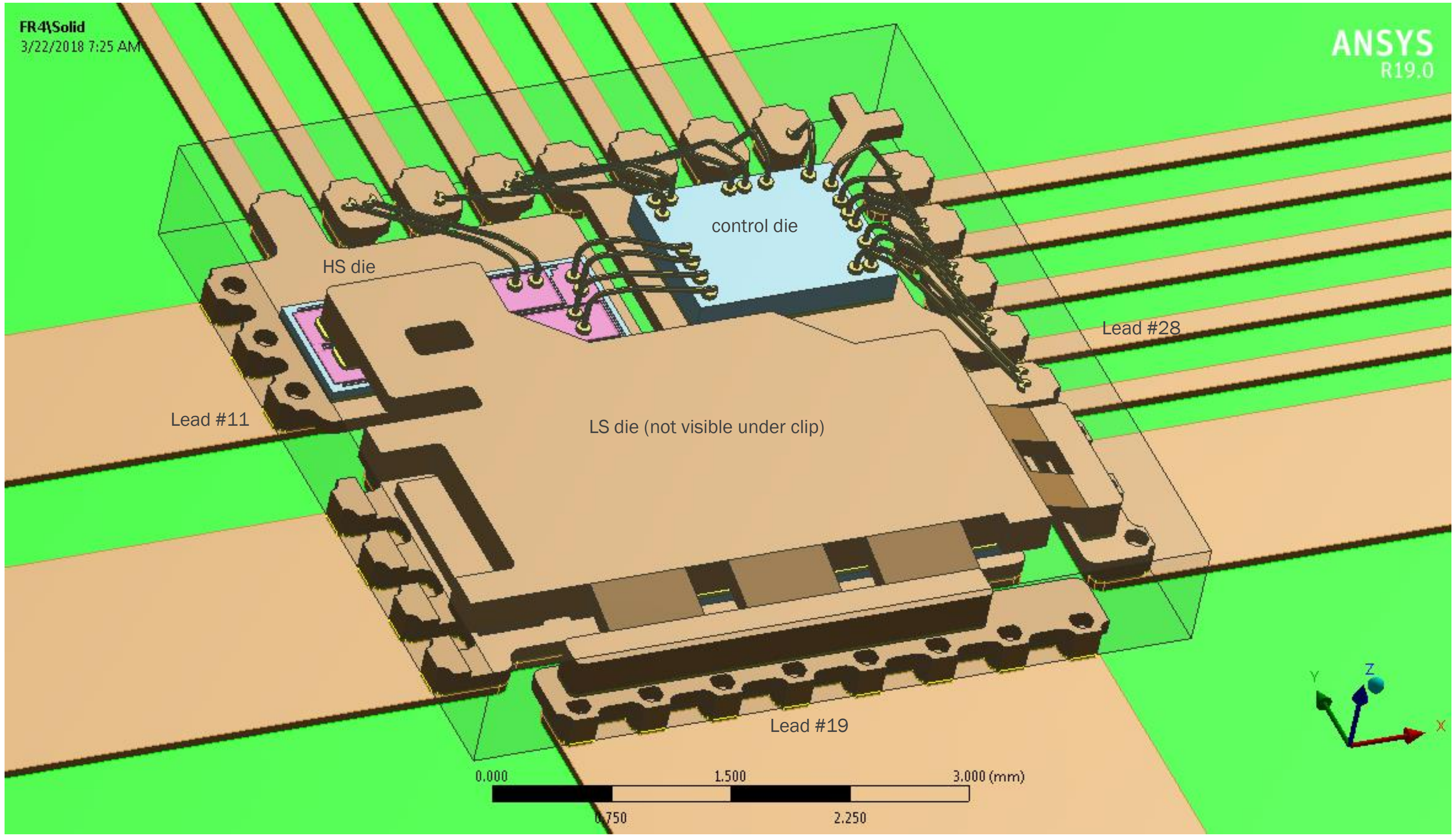
Finite Element Model

1) We were supplied with 3D geometry (STP) file
   a) Minimal changes were required (one "error" was corrected – an internal gap not filled with any material)
2) A "standard" thermal test board was added
   a) 80x80x1.5 mm, single layer
   b) Maximum width "traces" were established on top surface corresponding to Vin, PGND, and SW leads; this provides a rough approximation of how much "heat spreader" area might be possible in an actual application
3) Material properties for steady-state thermal analysis were assigned as appropriate for all model entities

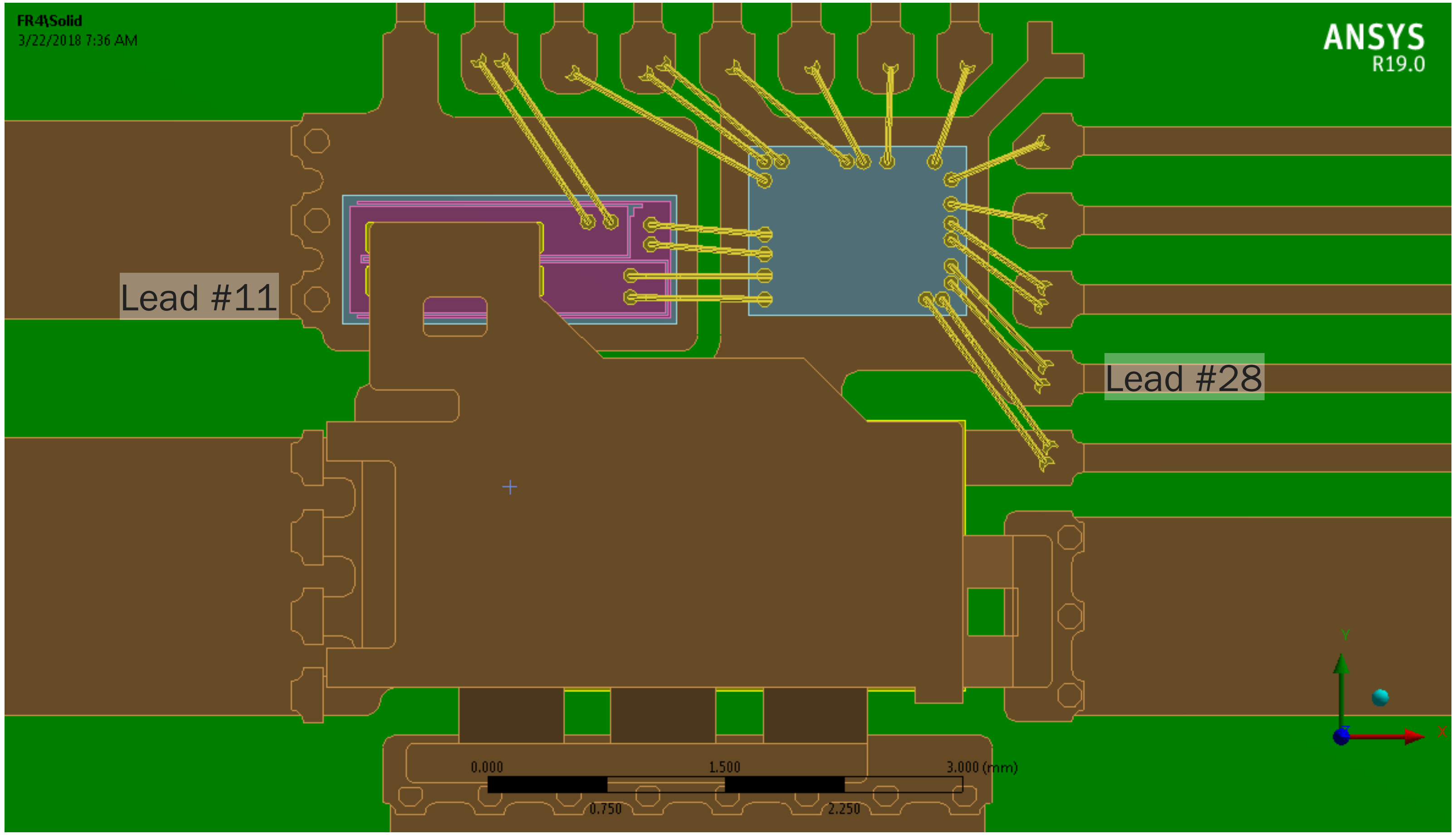
Material properties used

clip/DA solder	isotropic, constant k=81.7 W/m/°C
die	isotropic, temperature dependent
@0°C, k=170 W/m/°C	
@75°C, k=120 W/m/°C	
@150°C, k=95 W/m/°C	
wires	isotropic, k ≈ 310 W/m/°C
L/F and clip	isotropic, k=320 W/m/°C
EMC	isotropic, k=0.7 W/m/°C
FR4	orthotropic k_{xy}=1.059 W/m/°C, k_z=0.343 W/m/°C
traces	copper (annealed) isotropic, k ≈ 375 W/m/°C
board attach	isotropic, k=50.6 W/m/°C
source/gate metal	isotropic k ≈ 230 W/m/°C

FEM isometric view

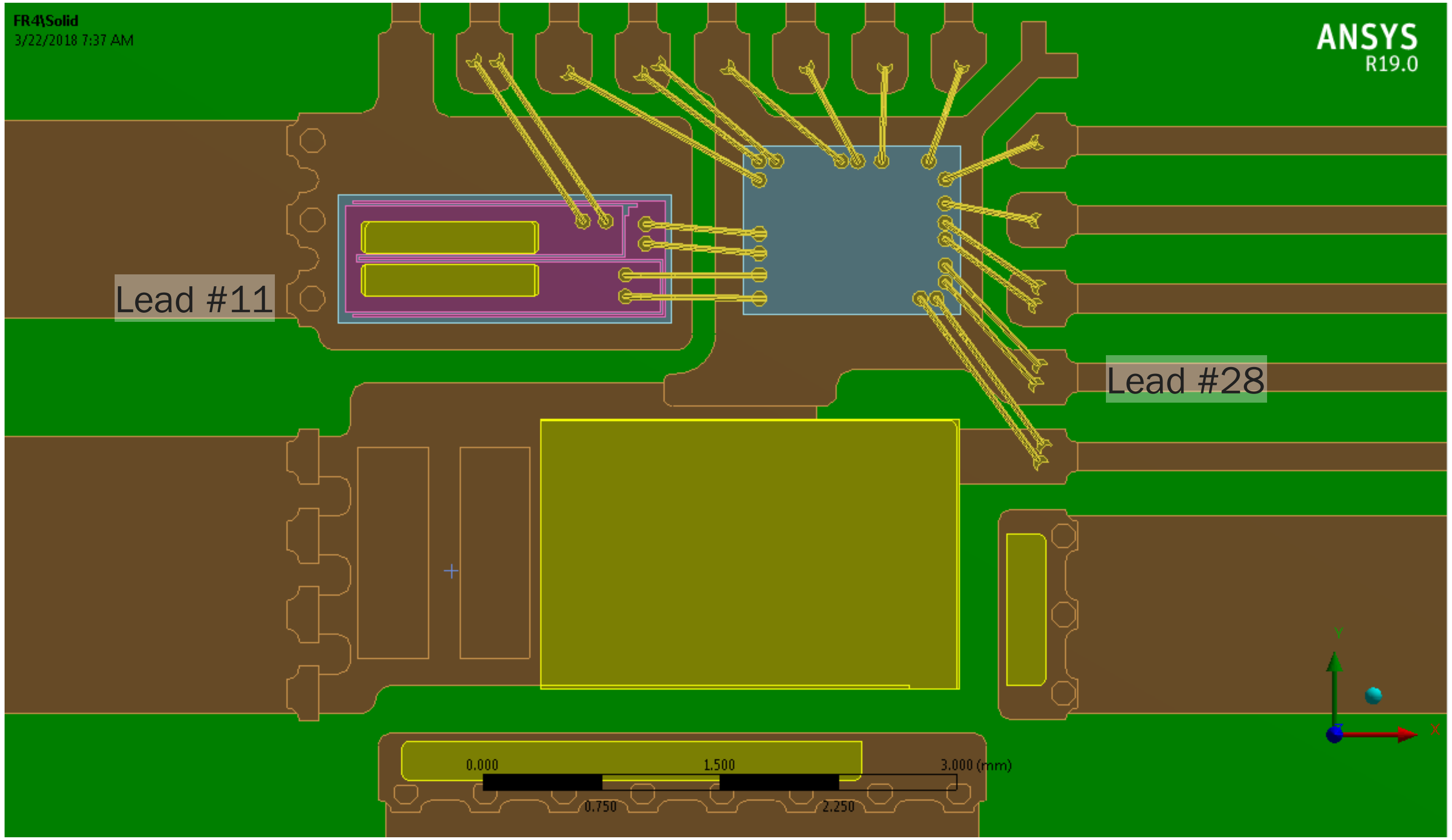


FEM top view, internal layout



Lead #19

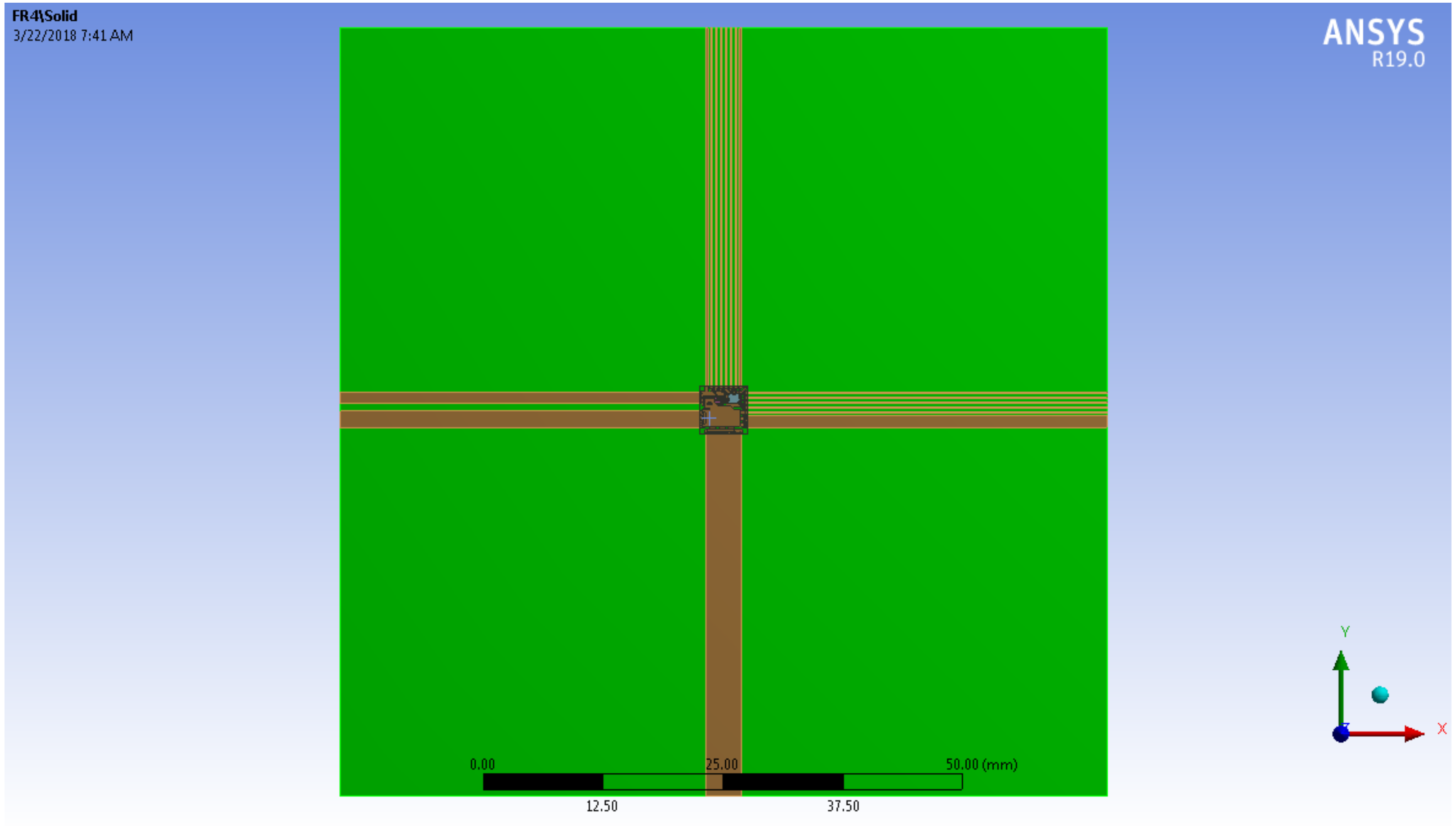
FEM top view with clip removed



Lead #19

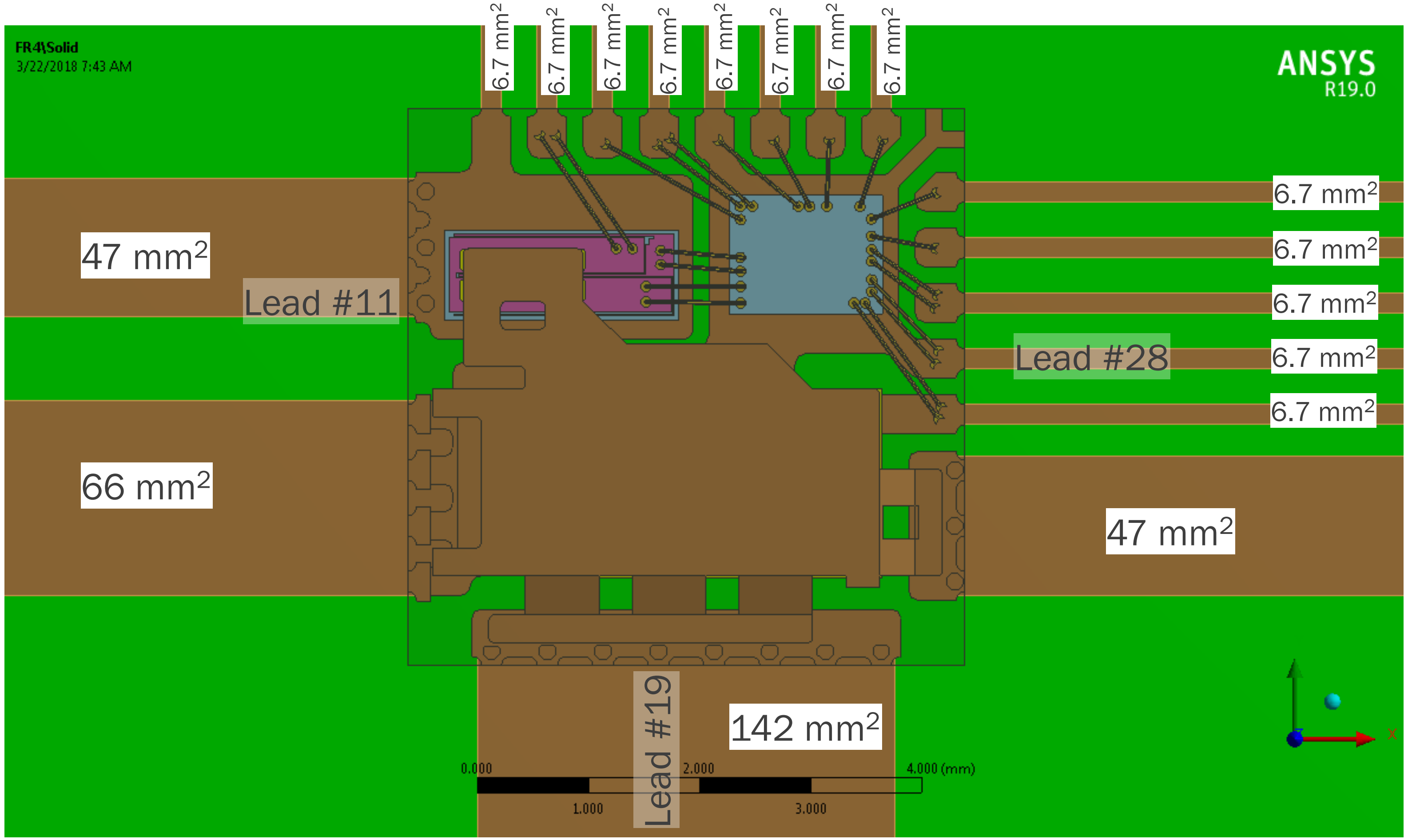
FEM, full view of 80x80 mm PCB

Total
trace/spreader
area
389 mm^2



Trace area detail

Total
trace/spreader
area
389 mm²



Linear equations derived from FEM describing three junction temperatures

These coefficients are derived from the center-of-die temperature nodes of the three die

T_LS = 6.46*Q-LS + 1.30*Q-HS + 4.05*Q-ctrl + 0.05*Tamb + 0.70*Tld-19 + 0.19*Tld-11 + 0.07*Tld-28

T_HS = 1.52*Q-LS + 6.53*Q-HS + 1.56*Q-ctrl + 0.02*Tamb + 0.18*Tld-19 + 0.78*Tld-11 + 0.02*Tld-28

T_ctrl = 3.94*Q-LS + 1.46*Q-HS + 22.67*Q-ctrl + 0.09*Tamb + 0.42*Tld-19 + 0.20*Tld-11 + 0.29*Tld-28

These coefficients are derived from the maximum temperature nodes of the three die

T_LS = 6.86*Q-LS + 1.24*Q-HS + 4.13*Q-ctrl + 0.06*Tamb + 0.69*Tld-19 + 0.18*Tld-11 + 0.07*Tld-28

T_HS = 1.51*Q-LS + 8.40*Q-HS + 2.03*Q-ctrl + 0.03*Tamb + 0.18*Tld-19 + 0.77*Tld-11 + 0.03*Tld-28

T_ctrl = 3.88*Q-LS + 1.45*Q-HS + 23.15*Q-ctrl + 0.10*Tamb + 0.42*Tld-19 + 0.19*Tld-11 + 0.29*Tld-28

Given Tamb, 3 lead temperatures, and 3 Pd values, these equations predict the junction temperatures from the original FEM with a root-mean-squared-error of only 0.5°C. Note, however, the 3x3 power coefficient sub-matrix is not exactly symmetric. If we “symmetrize” it so as to get symmetric R’s, the error increases to about 0.6°C.

Linear equations converted to resistor network

Each *power* coefficient has units of thermal resistance, but is not actually a thermal resistance. To get the inter-nodal resistances, the 3x3 matrix comprised of these 9 coefficients is inverted to obtain -1/R values on the off-diagonal, for instance:

coefficient matrix

6.46	1.52	3.94
1.30	6.53	1.46
4.05	1.56	22.67

units of °C/W

inverts to:

conductance matrix

0.1798	-0.035	-0.029
-0.029	0.1612	-0.005
-0.03	-0.005	0.0497

units of W/°C

negative reciprocals:

inter-nodal R's

	LS	HS	ctrl
LS	-5.56	28.73	34.46
HS	34.54	-6.20	186.53
ctrl	33.22	203.51	-20.14

units of °C/W

Each *temperature* coefficient is a boundary "sensitivity," which can be turned into a boundary resistance by dividing into the corresponding power coefficient

$$R_{ij} = \frac{k_{ii}}{k_{ij}}$$

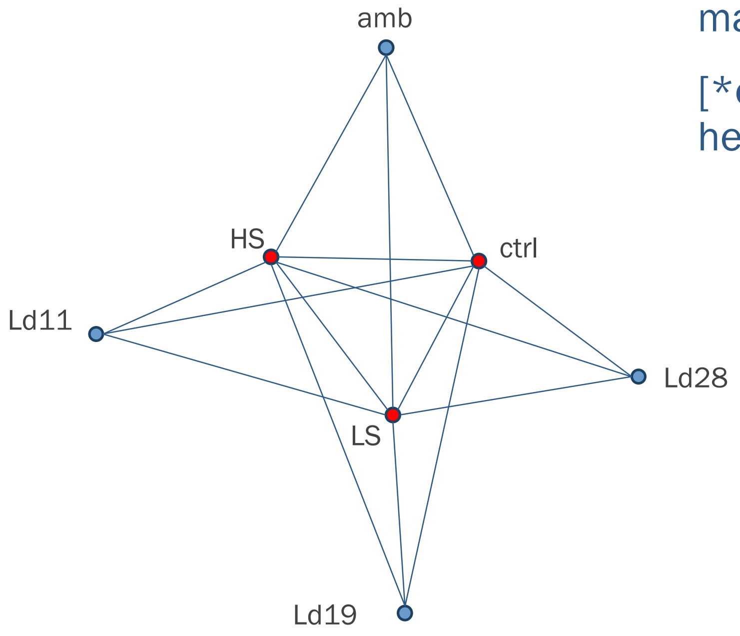
[A complete explanation of the theory and mathematics of this network analysis may be found in ON Semiconductor Application Note AND8214.]

End Result

The end result is a “mesh” network with interconnections between the three junction nodes and each of the boundary nodes:

These are the resistor values the result if the die-center temperatures are used for the model

	LS	HS	ctrl
LS	x		
HS	31.50	x	
ctrl	33.84	194.66	x
amb	130.98	294.82	147.12
Ld19	9.27	36.65	31.51
Ld11	34.55	8.41	68.15
Ld28	97.72	283.61	45.56



These are the resistor values that result if the max-temperature nodes* are used for the model

[*established for each die when it alone was heated]

	LS	HS	ctrl
LS	x		
HS	46.63	x	
ctrl	36.95	182.94	x
amb	119.10	324.58	141.15
Ld19	9.93	47.86	32.47
Ld11	38.35	10.92	69.46
Ld28	94.94	292.07	46.08

1) As mentioned on an earlier slide, in order to ensure that these network resistors are symmetric (i.e. they have the same value regardless of which direction heat flows through them), a small sacrifice in accuracy was accepted.
2) Though the “max node” predictions average slightly higher than the “die center” predictions (as they should), any particular difference is not always positive. Even so, use of the “max node” network is recommended.

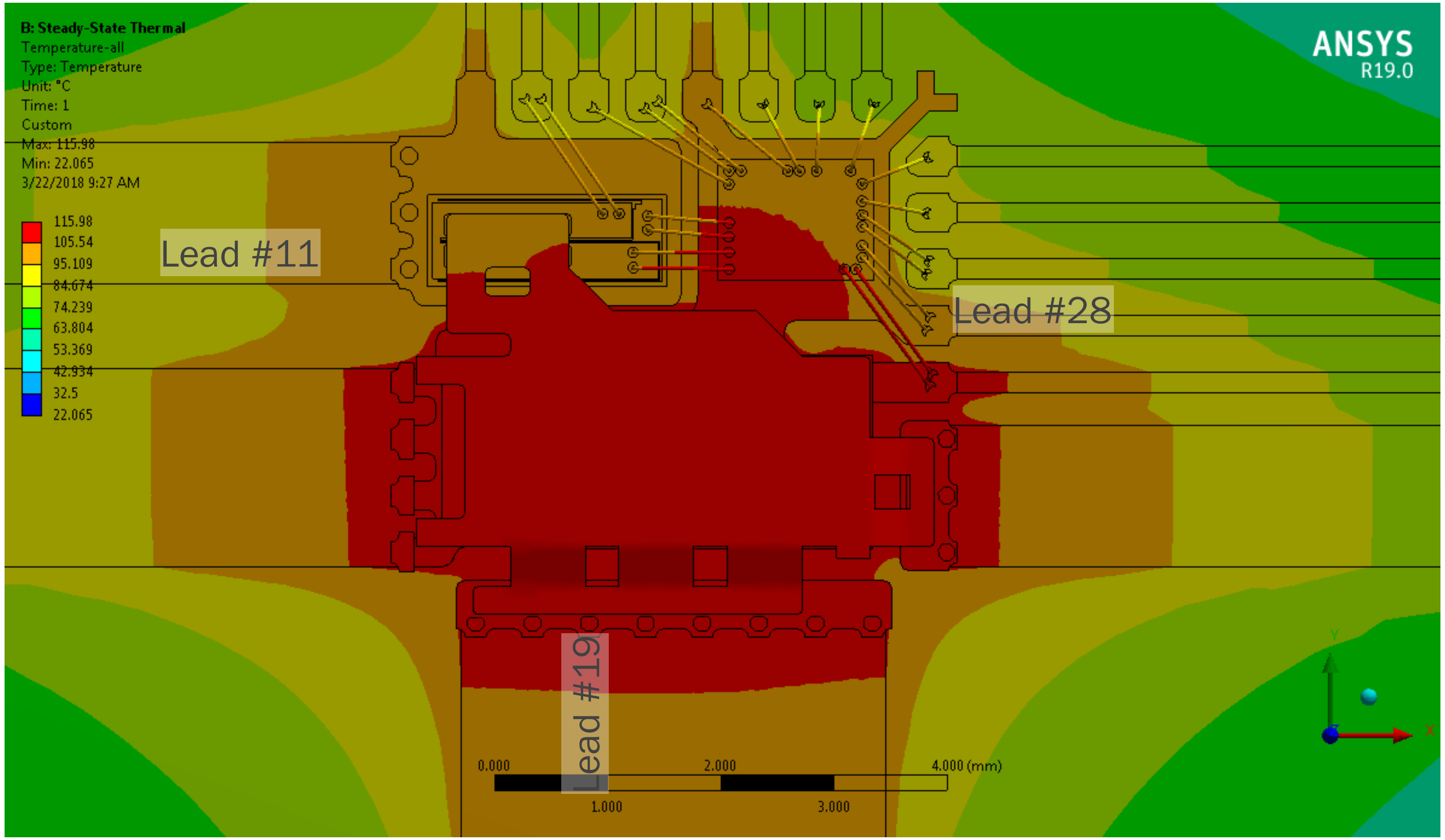
Conclusions and cautions

1) As mentioned on an earlier slide, in order to ensure that these network resistors are symmetric (i.e. they have the same value regardless of which direction heat flows through them), a small sacrifice in accuracy was accepted.
2) Though the "max node" predictions average slightly higher than the "die center" predictions (as they should), any particular difference is not always positive. Even so, use of the "max node" network is recommended.
3) The linear equations derived directly from the FEM may be convenient for estimating junction temperatures in an experimental environment where lead temperatures can be measured. The resistor network(s) are more useful as compact models to be incorporated into a larger system simulation.
4) Although it might seem that the values of the resistors connected to ambient ought to reflect the amount of metal in the PCB, the effect is weak; further, in the "self heating" simulations, heat convected directly to ambient (as opposed to being conducted through the characterized leads) was less than 5% of the total heat dissipated. In other words, even fairly significant changes to these resistor values would have a very small effect on predicted junction temperatures.

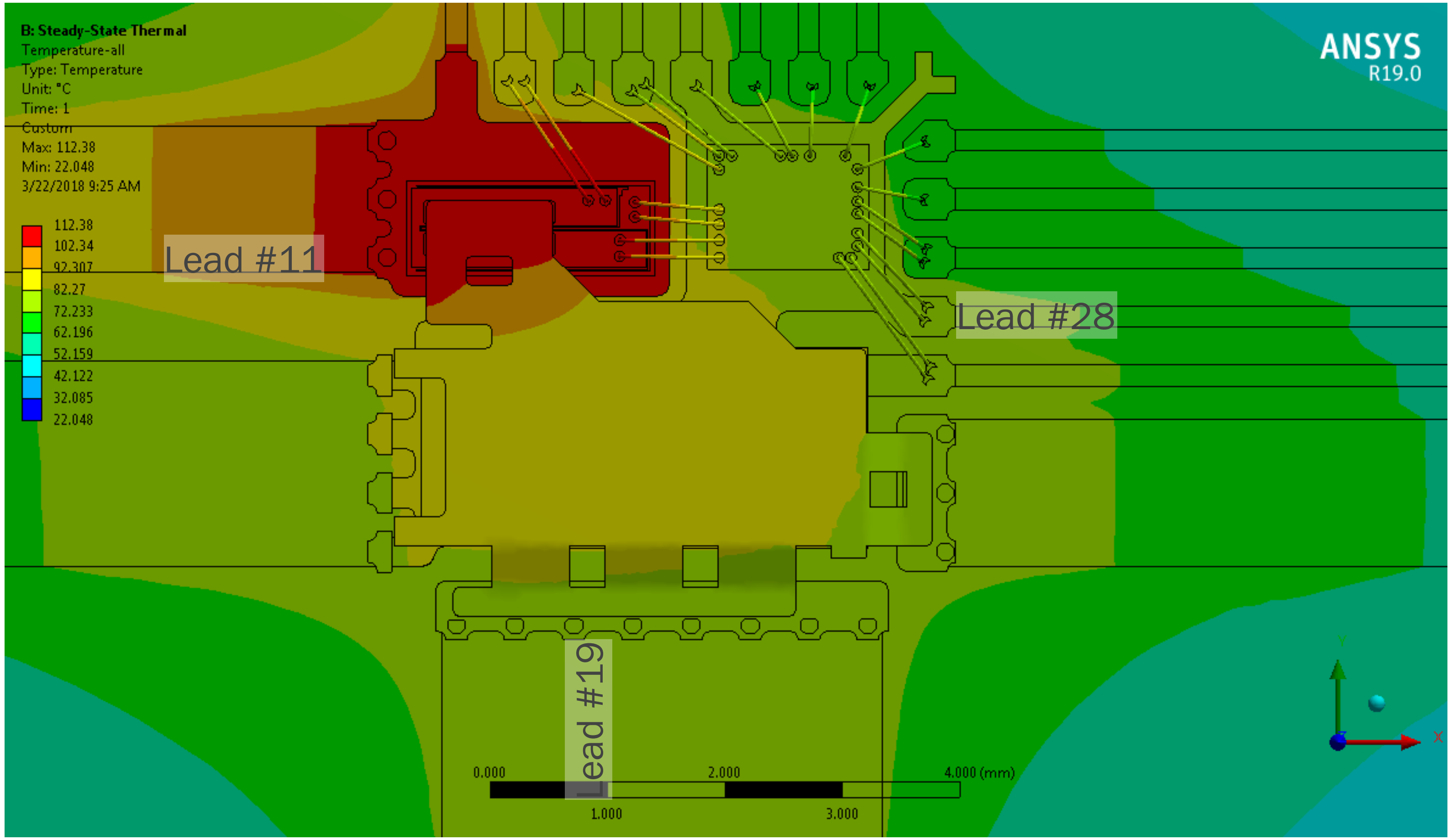
ANSYS temperature plots

(for visual reference)

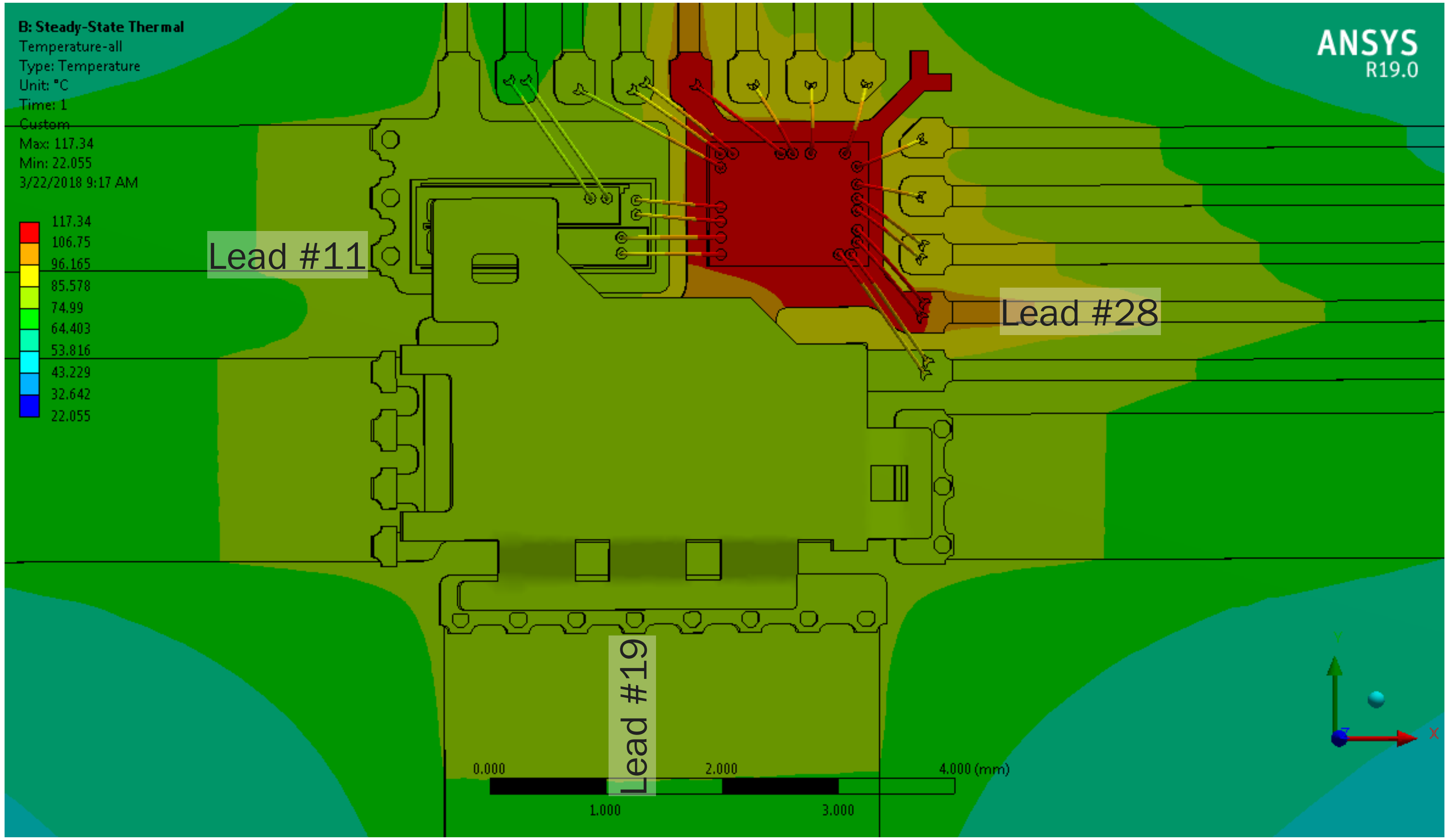
FEM, LS die only heated, 2 W



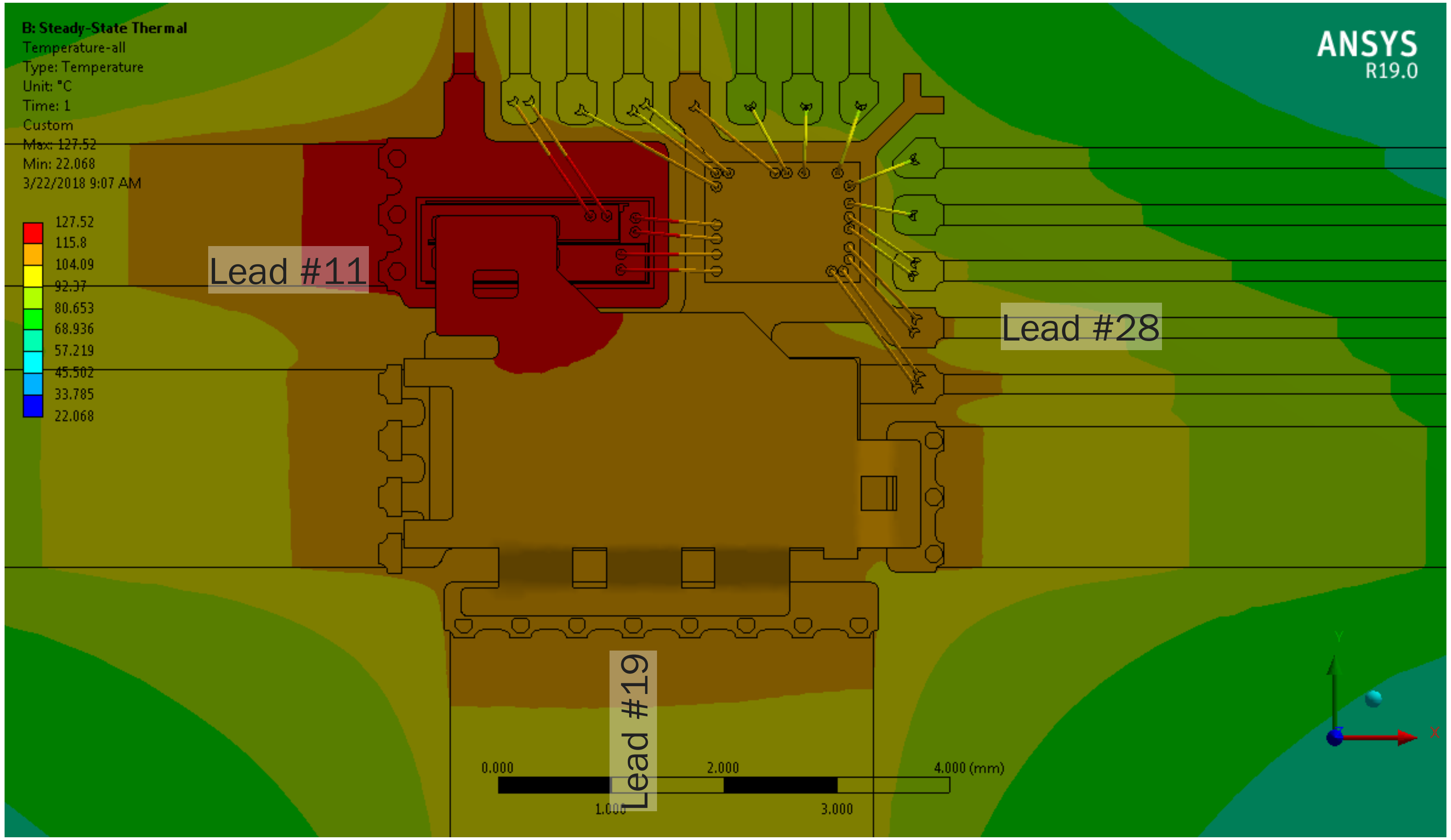
FEM, HS die only heated, 1.5 W



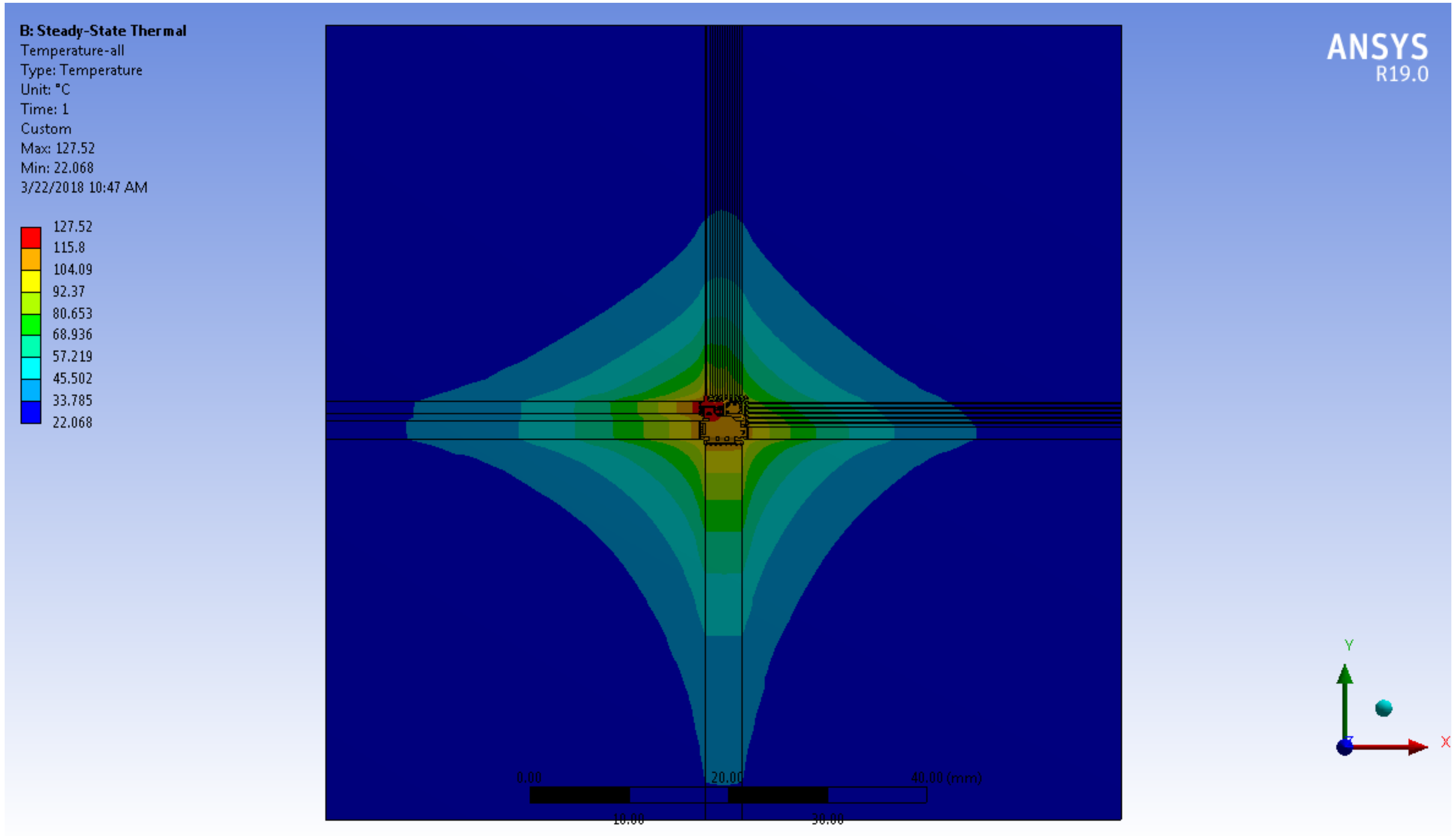
FEM, ctrl die only heated, 1.5 W



FEM all die heated, LS=1 W, HS=1 W, ctrl=0.1 W



FEM all die heated, LS=1 W, HS=1 W, ctrl=0.1 W (mold removed)



FEM all die heated, LS=1 W, HS=1 W, ctrl=0.1 W (mold shown)