

- 1 Material: Isola IS370HR, check layer stack description in this document
- 2 Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer $1 \div 4 \mu\text{m}$, gold layer $0.076 \div 0.2 \mu\text{m}$
- 3 All gerber files generated as a top view
 4. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
 5. All holes diameter refer to final diameter after eventual plating
- 6 All microvias in BGA package pads have to be filled with copper !
- 7 Two fiducials are located close to BGA package

Gerber and drill file extensions table

Gerber files	Description
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	L1_TOP - Top Layer
.G1	L2_POWER - Internal power plane layer
.G2	L3_GND - Internal ground plane
.GBL	L4_BOTTOM - Bottom Layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Bottom side silkscreen
.GM1	Board outline
Drill files	
.TXT	Layer pair L1_TOP to L4_BOTTOM - PTH holes
.TX2	Layer pair L3_GND to L4_BOTTOM - microvias

SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
PCB fabrication notes and requirements		Fabrication document	Sheet 1 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			

1

2

3

4

5

Layer Stack

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
	Surface Material	0.0150mm(0.591mil)	Solder Resist	Solder Mask	GTS
	Nickel, Gold	0.0050mm(0.197mil)		Surface Finish	
	Copper foil	0.0340mm(1.339mil)		Signal	GTL
	Prepreg	0.0800mm(3.150mil)	Isola 370HR: 1 x 1080-68	Dielectric	
	Copper foil	0.0180mm(0.709mil)		Signal	G1
	Core	1.0000mm(39.370mil)	Isola 370HR: 6 x 7628-42	Dielectric	
	Copper foil	0.0180mm(0.709mil)		Signal	G2
	Prepreg	0.0800mm(3.150mil)	Isola 370HR: 1 x 1080-68	Dielectric	
	Copper foil	0.0340mm(1.339mil)		Signal	GBL
	Nickel, Gold	0.0050mm(0.197mil)		Surface Finish	
	Surface Material	0.0150mm(0.591mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.3040mm(51.339mil)					

SECO-RANGEFINDER-GEVK

Revision:
1.0State:
released

Layer stack details

Engineer: Stefan Kosterec

Date: 01.Jun 2020 20:15

Fabrication
documentSheet
2 / 15

PCB File: Lidar_board.PcbDoc

Repository revision: 1968

ON Semiconductor
Solution Engineering Center
Piestany

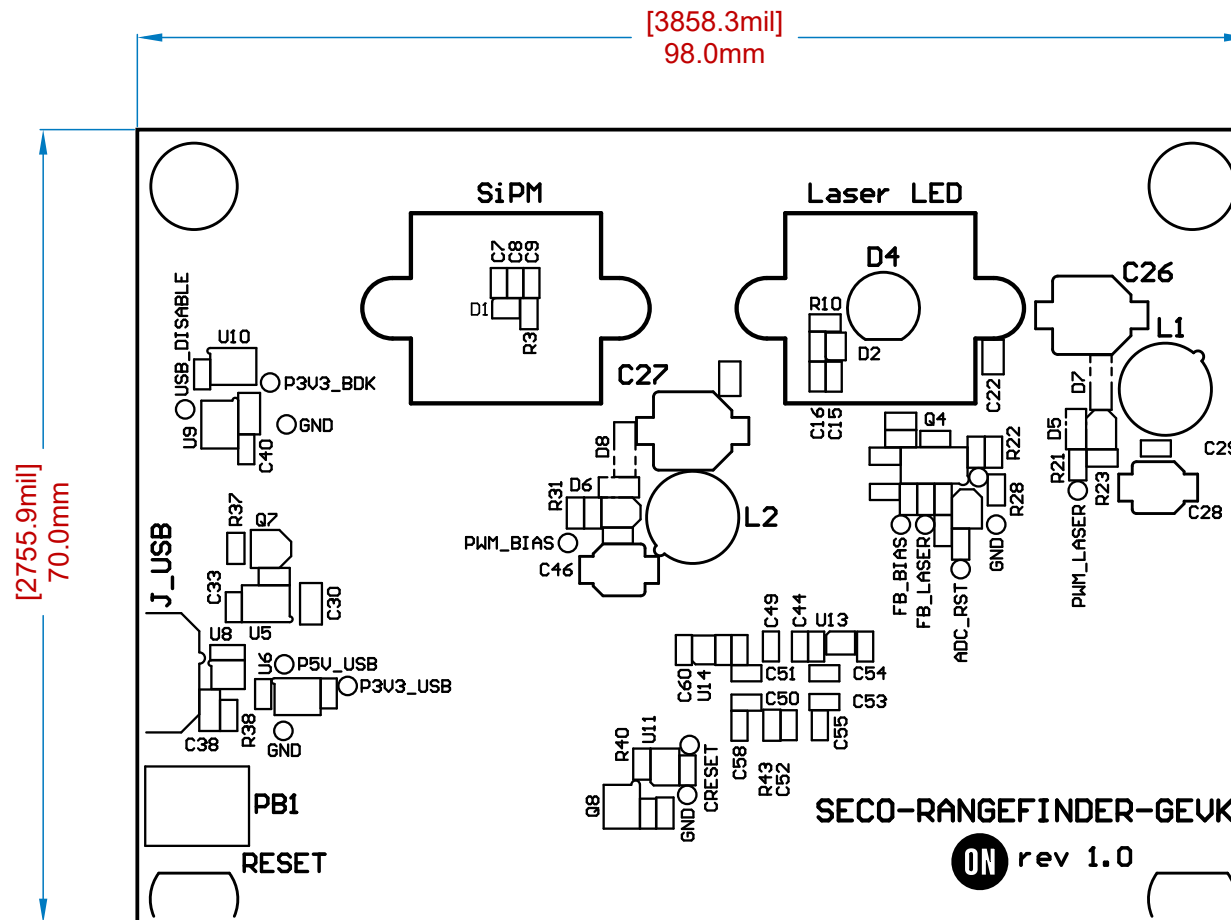
1

2

3

4

5



SECO-RANGEFINDER-GEVK

Board outline definition - top view 3:2

Engineer: Stefan Kosterec

Date: 01.Jun 2020 20:15

PCB File: Lidar_board.PcbDoc

Repository revision: 1968

Revision:
1.0

State:
released

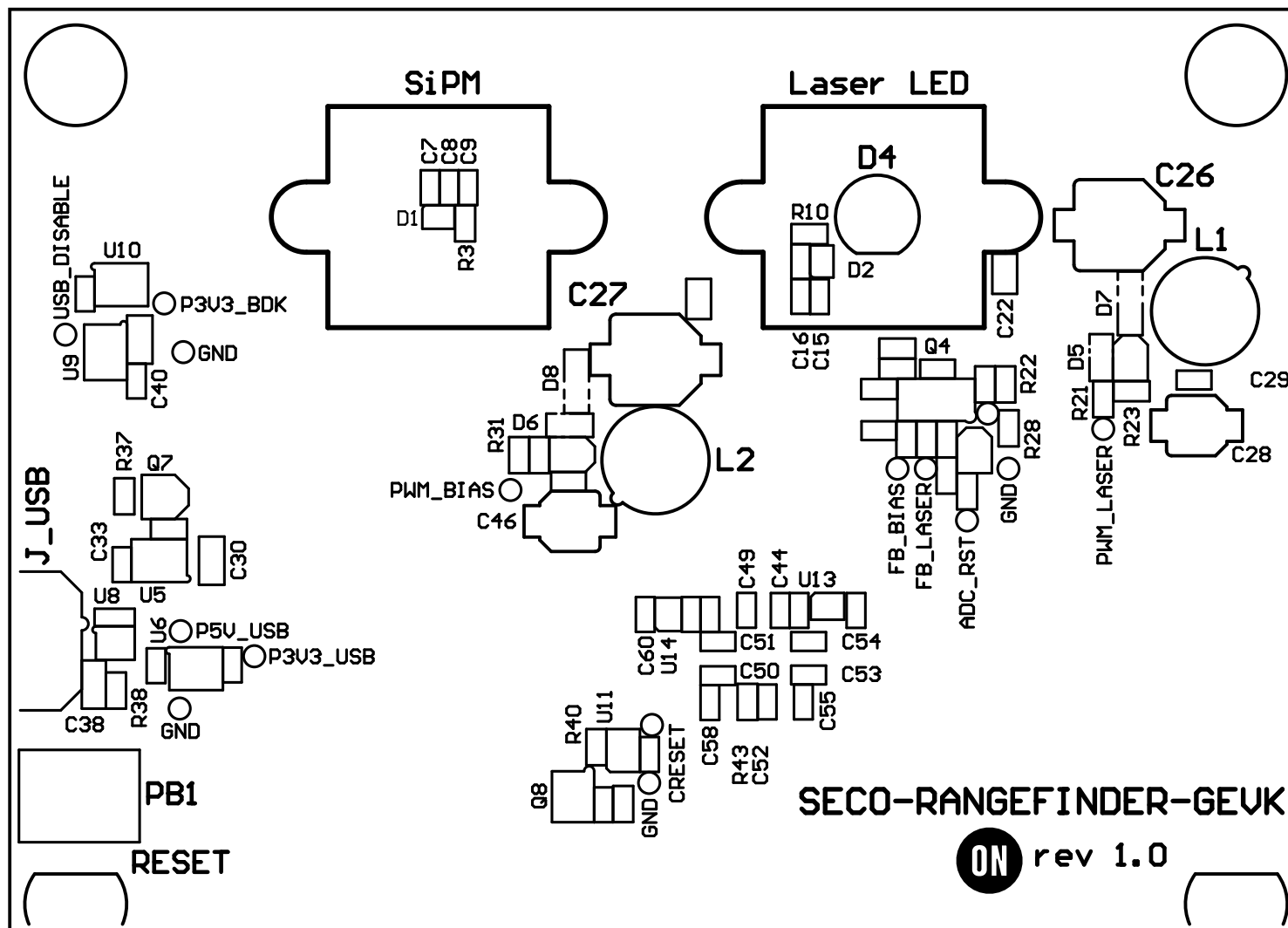
Fabrication
document

Sheet
3 / 15

ON Semiconductor
Solution Engineering Center
Piestany



Top Overlay (Scale 2:1)



SECO-RANGEFINDER-GEVK

Revision:
1.0

State:
released

Top side silkscreen - top view

Engineer: Stefan Kosterec

Date: 01.Jun 2020 20:15

Fabrication
document

Sheet
4 / 15

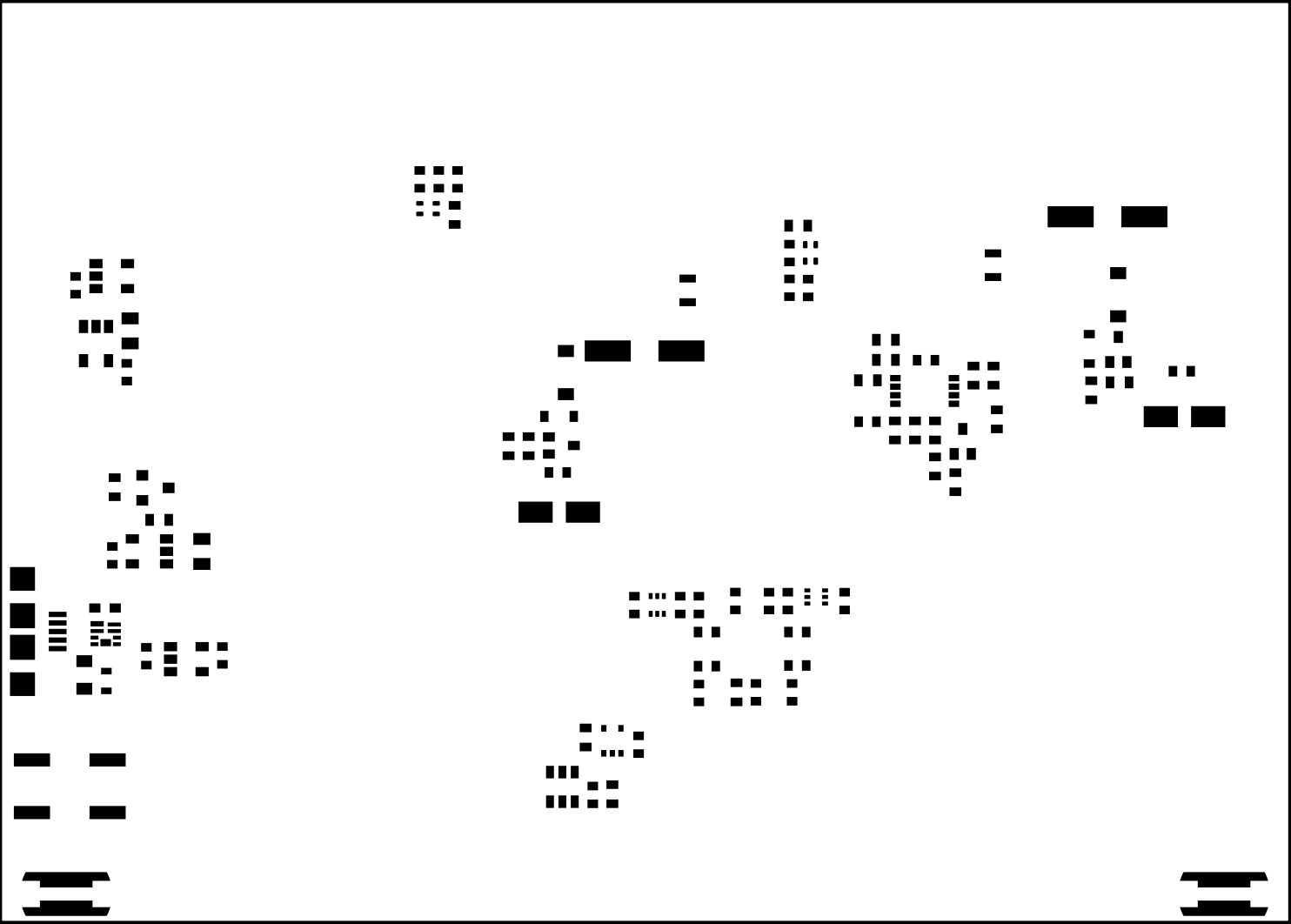
PCB File: Lidar_board.PcbDoc

Repository revision: 1968

ON Semiconductor
Solution Engineering Center
Piestany



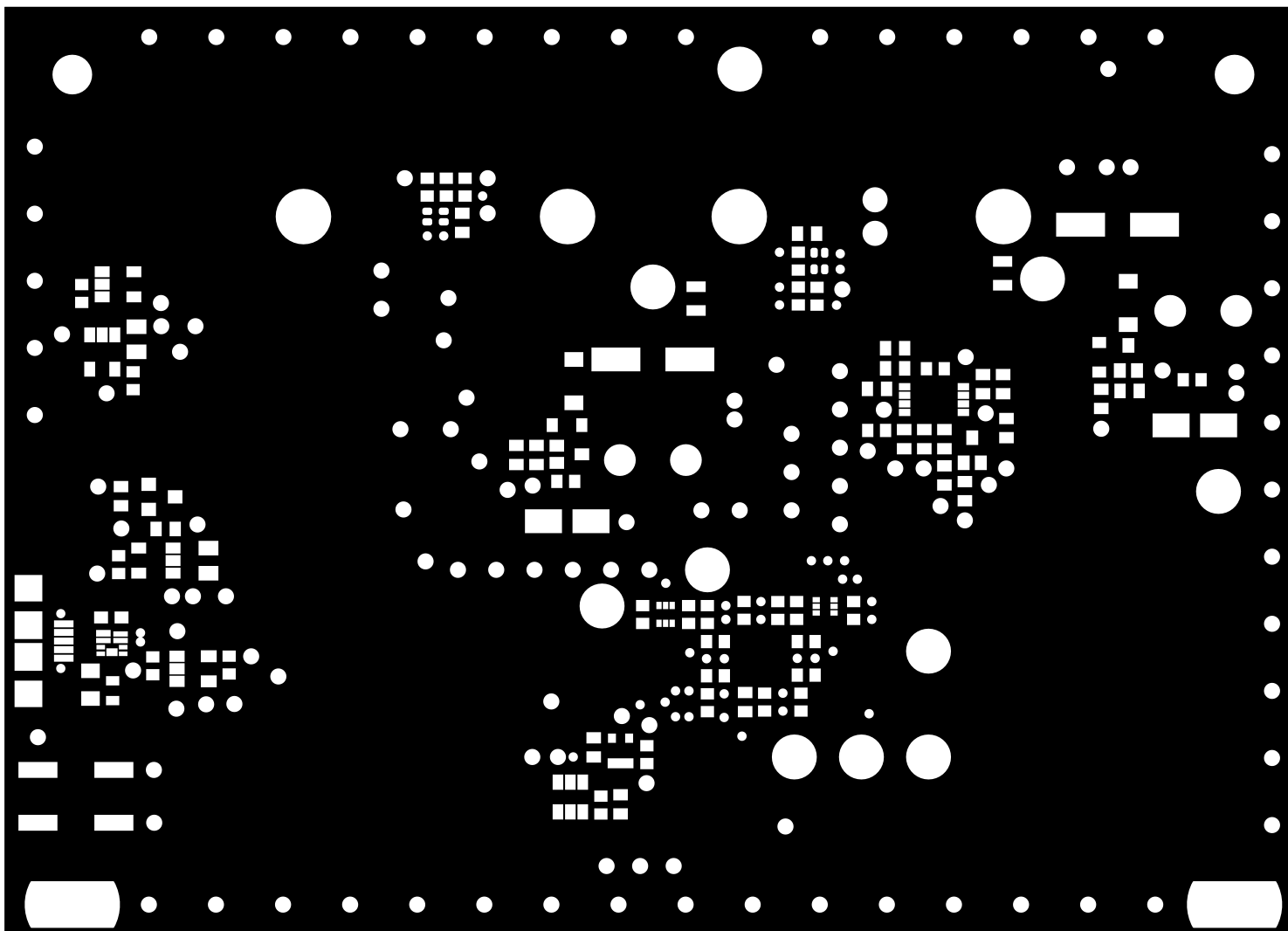
Top Paste (Scale 2:1)



SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
<i>Top side solder paste - top view</i>		Fabrication document	Sheet 5 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



Top Solder (Scale 2:1)



SECO-RANGEFINDER-GEVK

Revision:
1.0

State:
released

Top side solder mask - top view

Fabrication
document

Sheet
6 / 15

Engineer: Stefan Kosterec

Date: 01.Jun 2020 20:15

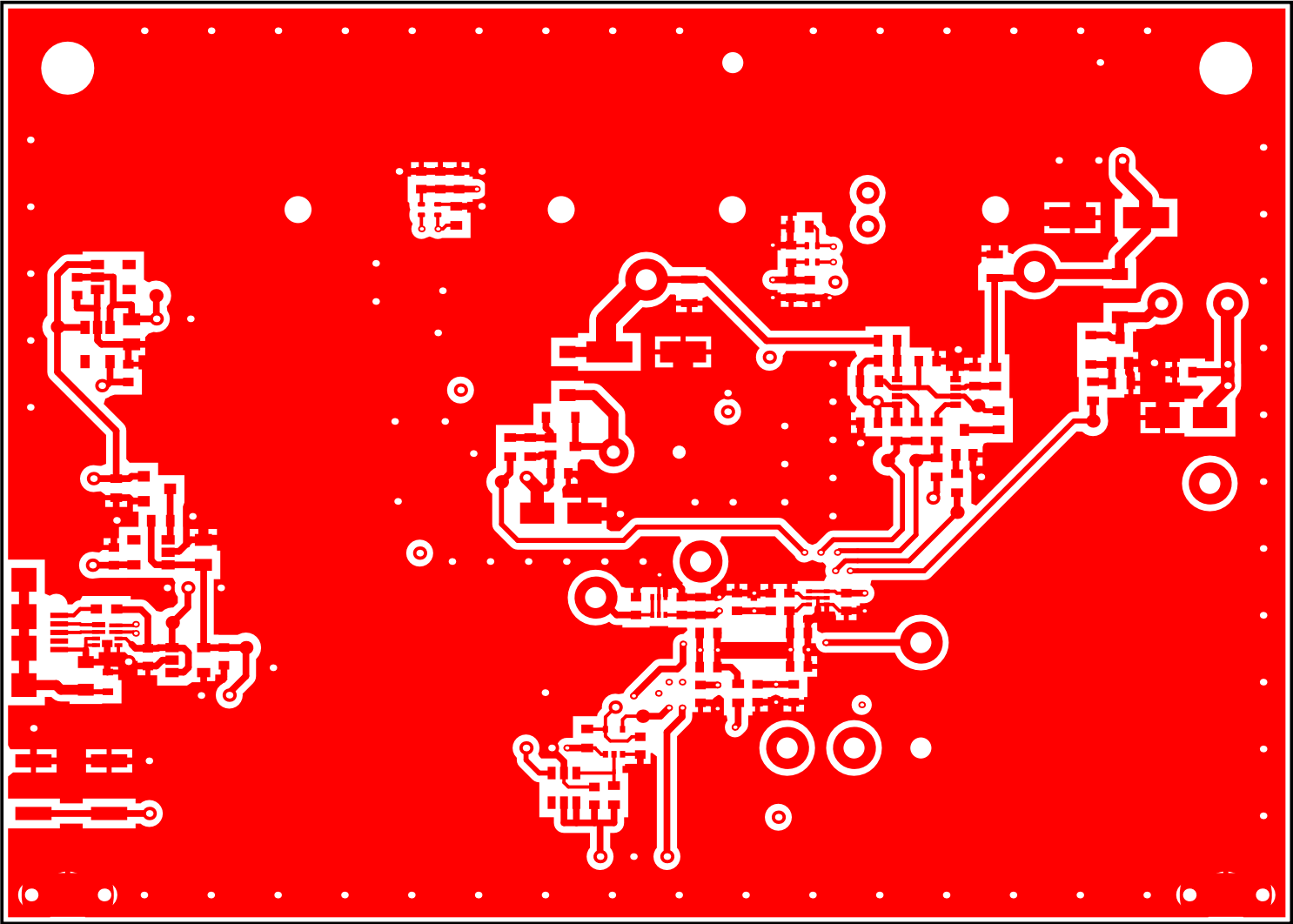
PCB File: Lidar_board.PcbDoc


Repository revision: 1968

ON Semiconductor
Solution Engineering Center
Piestany



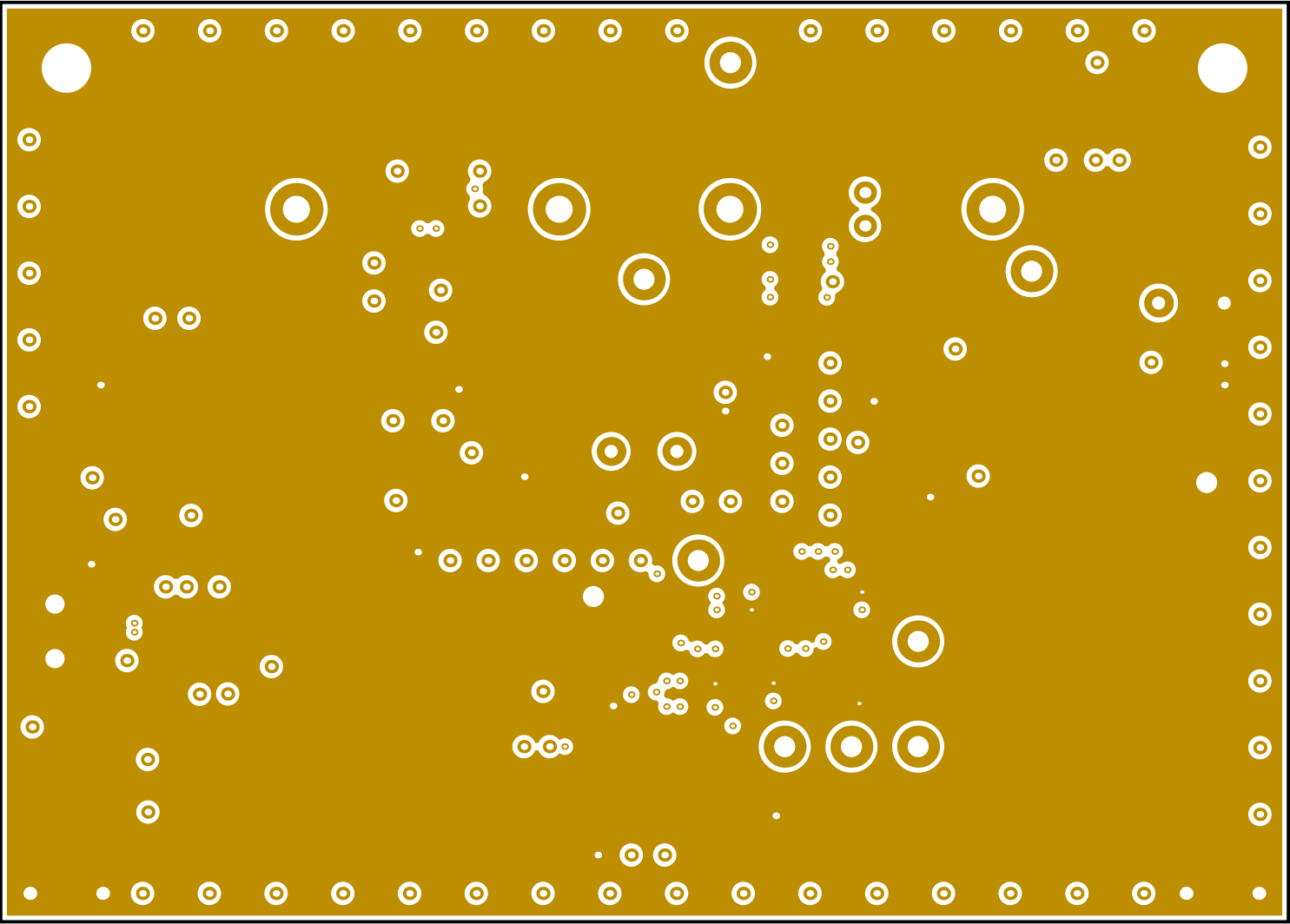
L1_TOP (Scale 2:1)




SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
Top Layer - top view		Fabrication document	Sheet 7 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



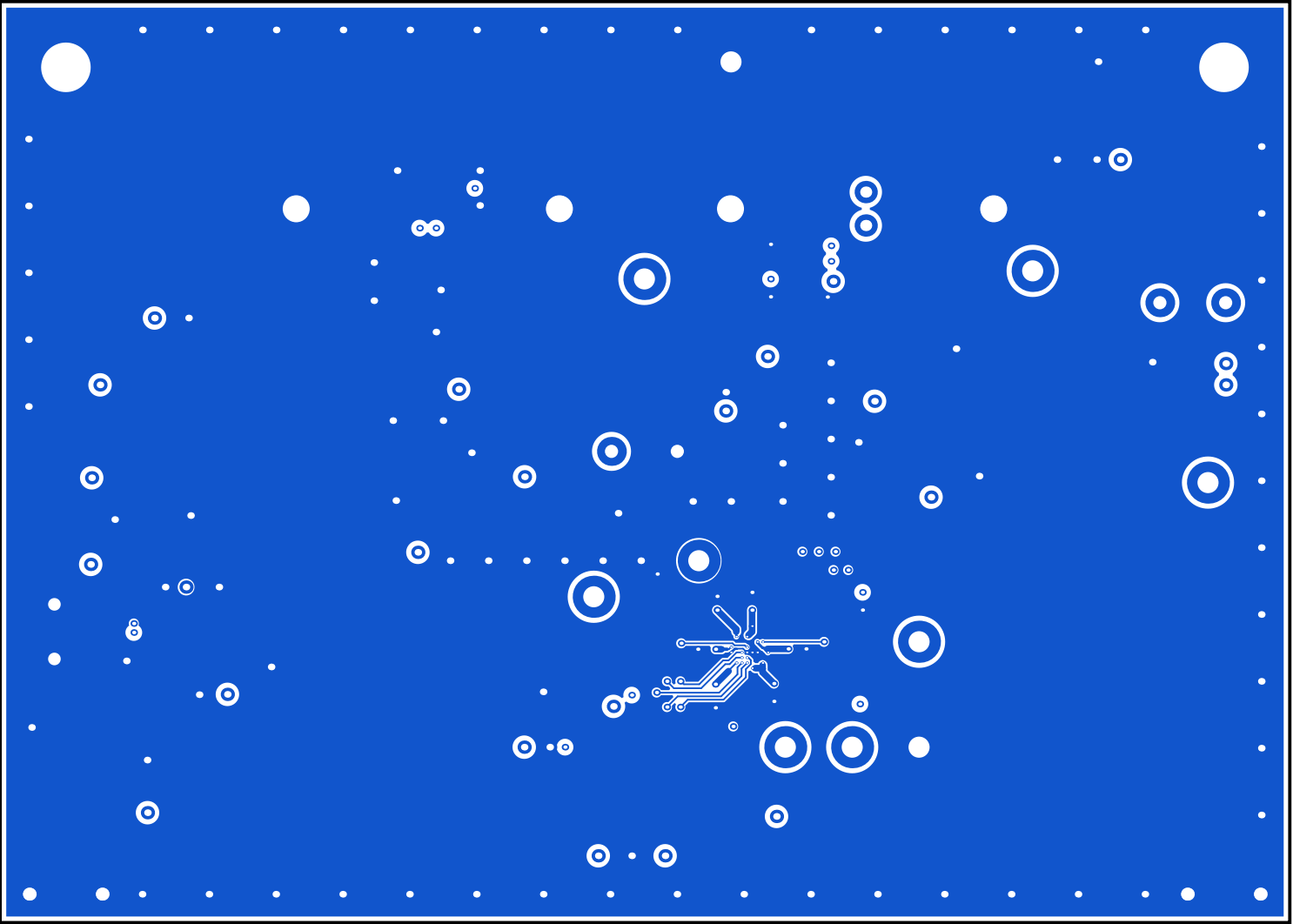
L2_POWER (Scale 2:1)




SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
<i>L2_POWER - internal power plane - top view</i>		Fabrication document	Sheet 8 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



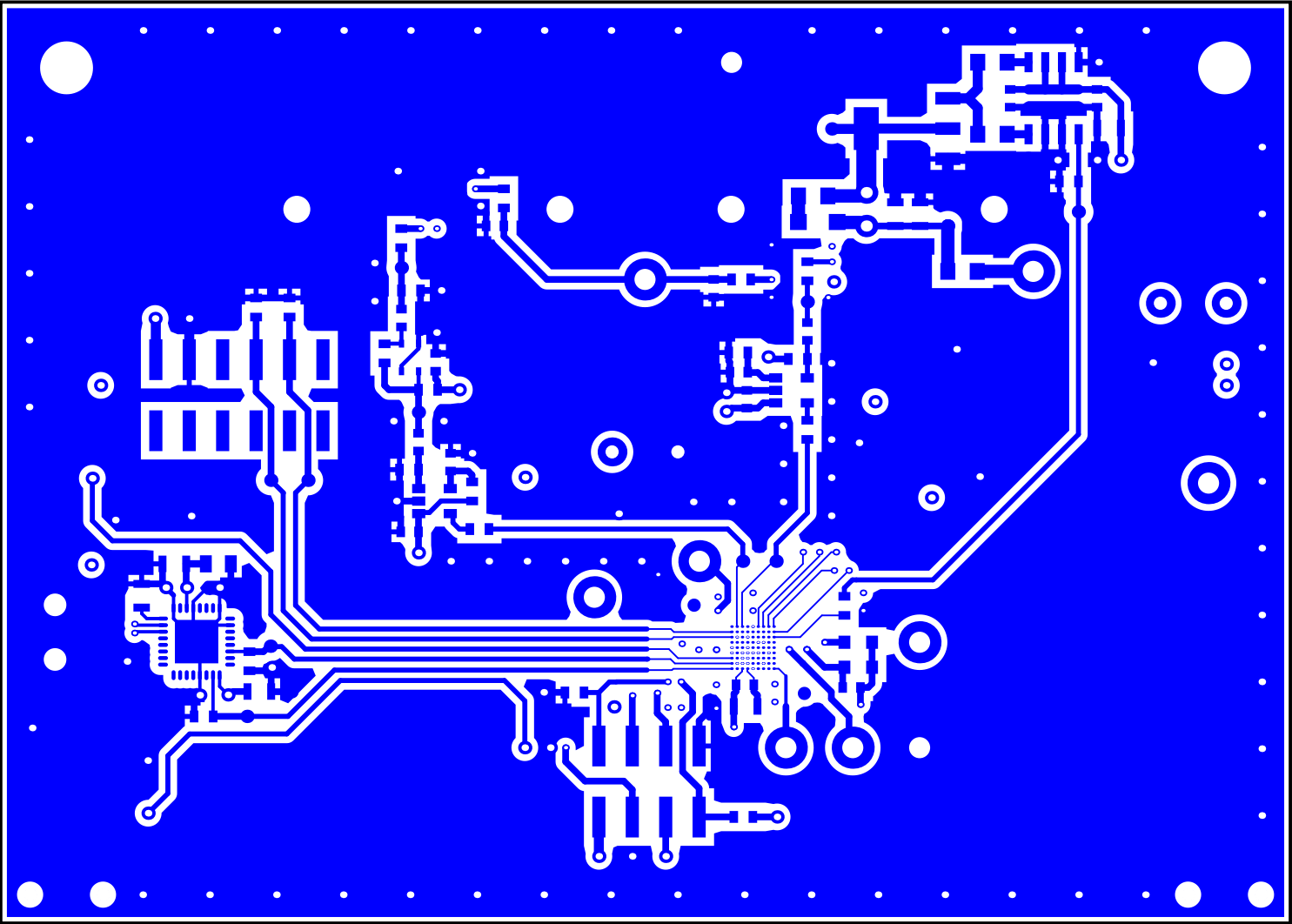
L3_GND (Scale 2:1)




SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
<i>L3_GND - internal ground plane - top view</i>		Fabrication document	Sheet 9 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



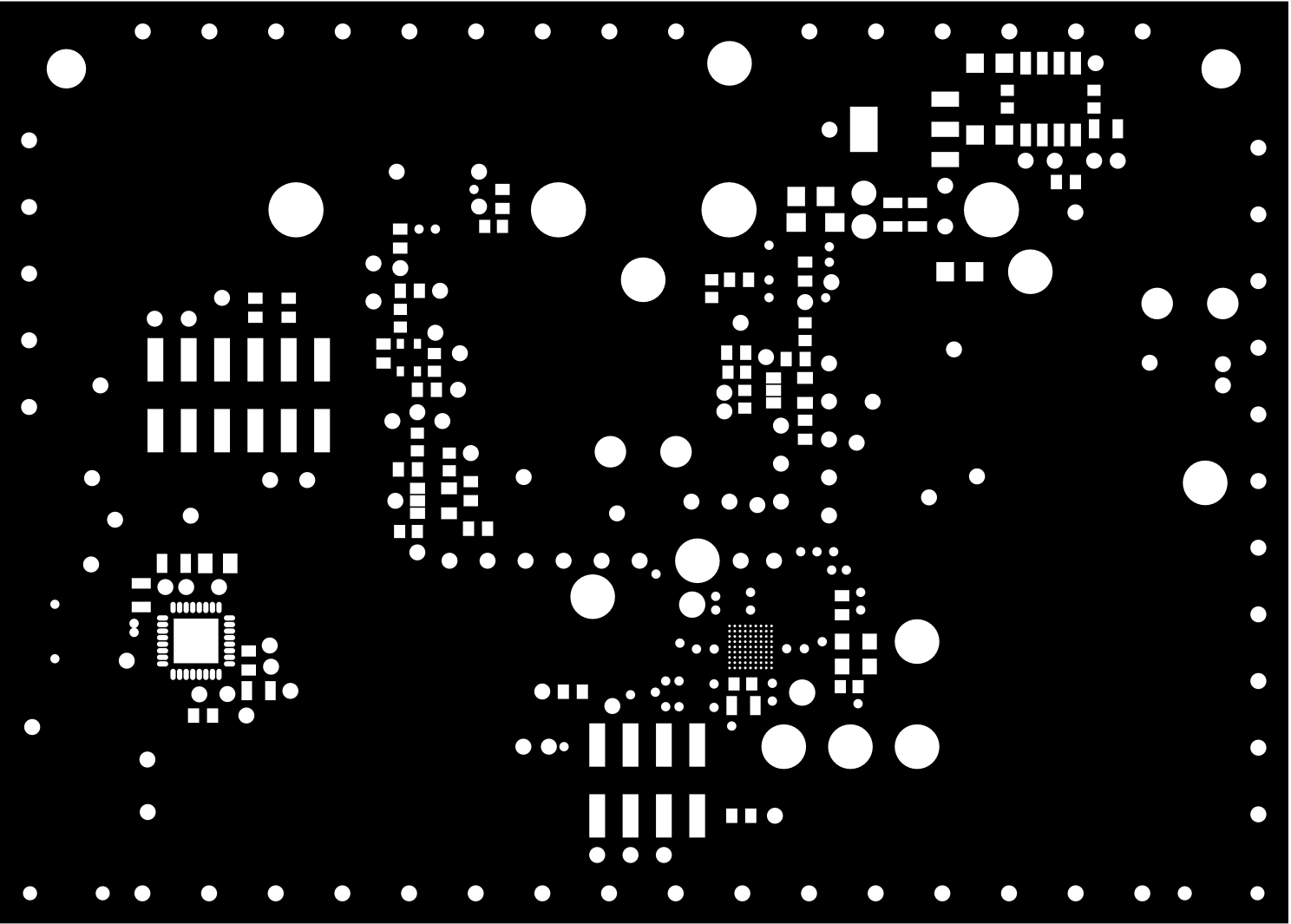
L4_BOTTOM (Scale 2:1)




SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
<i>L4_BOTTOM Layer - top view</i>		Fabrication document	Sheet 10 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



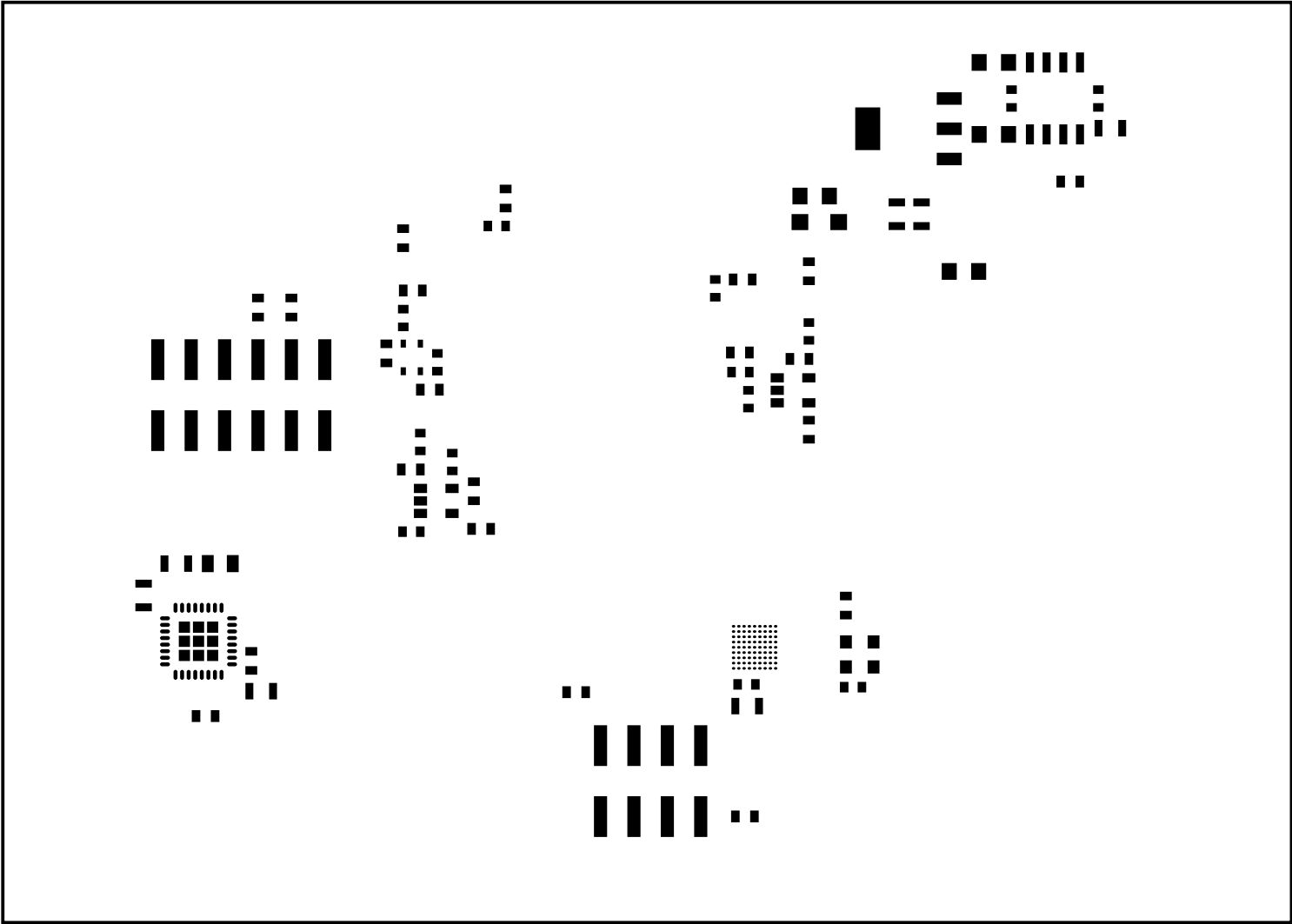
Bottom Solder (Scale 2:1)




SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
Bottom side solder mask - top view		Fabrication document	Sheet 11 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



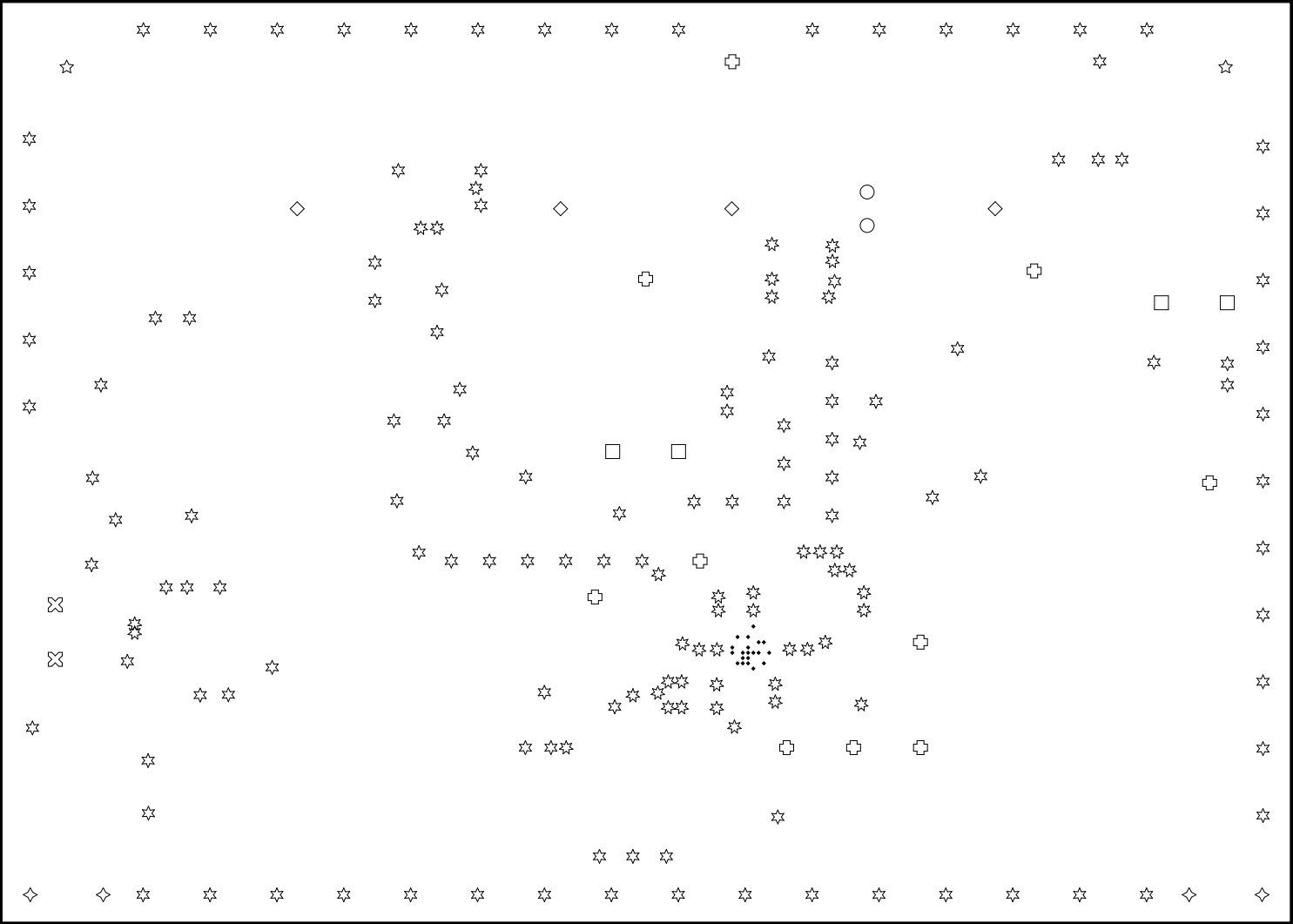
Bottom Paste (Scale 2:1)



SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
Bottom side solder paste - top view		Fabrication document	Sheet 12 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



Drill Drawing View (Scale 2:1)



8 Related drill table can be found on page 15

SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
Drill drawing		Fabrication document	Sheet 14 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
•	20	0.100mm(3.9mil)	Plated	[UVIA] L3_GND - L4_BOTTOM	Via	vialnBGApad
☆	42	0.254mm(10.0mil)	Plated	L1_TOP - L4_BOTTOM	Via	thru_small
☆	119	0.508mm(20.0mil)	Plated	L1_TOP - L4_BOTTOM	Via	thru_middle
⊗	2	0.700mm(27.6mil)	Non-Plated	L1_TOP - L4_BOTTOM	Pad	c0hn70
○	2	0.850mm(33.5mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c170h85
◇	4	0.970mm(38.2mil)	Non-Plated	L1_TOP - L4_BOTTOM	Pad	c87hn97(Tol20-0)
□	4	1.000mm(39.4mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c220h100
⊕	10	1.600mm(63.0mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c320h160
◇	4	2.050mm(80.7mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c400h205
☆	2	3.000mm(118.1mil)	Non-Plated	L1_TOP - L4_BOTTOM	Pad	c280hn300
	209 Total					

⑨ Related drill drawing can be found on page 14

SECO-RANGEFINDER-GEVK		Revision: 1.0	State: released
<i>Drill table</i>		Fabrication document	Sheet 15 / 15
Engineer: Stefan Kosterec	Date: 01.Jun 2020 20:15		
PCB File: Lidar_board.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: 1968			