SCV2951

100 mA, Low Power Low Dropout Voltage Regulator

The SCV2951 is a micropower voltage regulator that is specifically designed to maintain proper regulation with an extremely low input−to−output voltage differential. This device features a very low quiescent bias current of 75 μA and is capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The SCV2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power−on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn−off or turn−on the regulator output.

Due to the low input−to−output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The SCV2951 is available in the eight pin SOIC−8 package. The device features an initial output voltage tolerance ±0.5%.

Features

- Low Quiescent Bias Current of 75 μA
- Low Input−to−Output Voltage Differential of 50 mV at 100 μA and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V ±0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 μF Output Capacitor for Stability
- Internal Current and Thermal Limiting
- Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable; Device Temperature Grade 0: −40°C to +150°C Ambient Operating Temperature Range
- These Devices are Pb−Free and RoHS Compliant
- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

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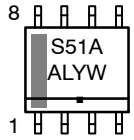
SOIC−8
CASE 751

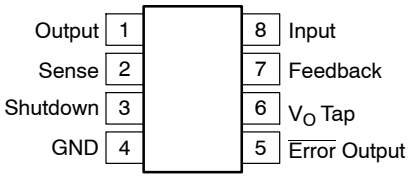
MARKING DIAGRAM



S51A	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING & MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

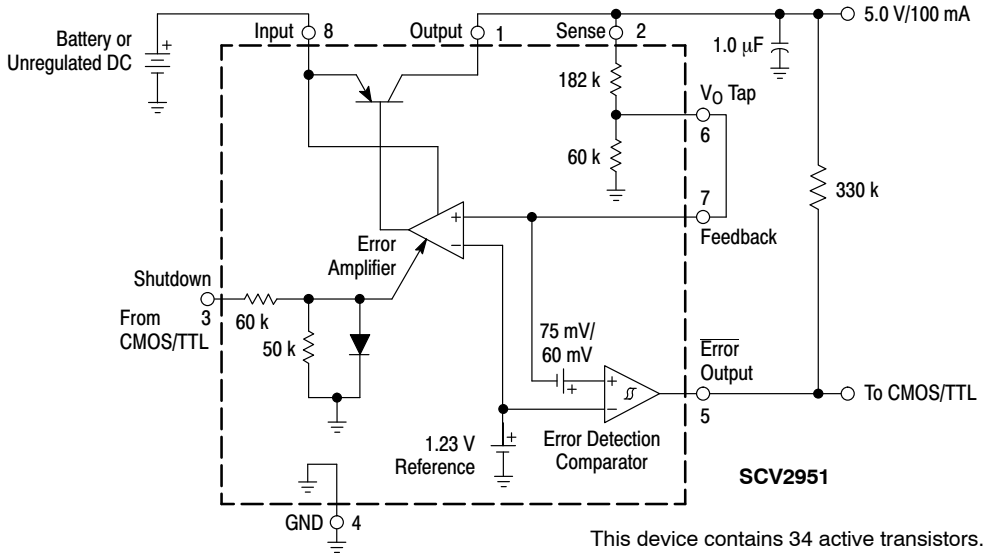


Figure 1. Representative Block Diagrams

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	30	Vdc
Peak Transient Input Voltage (t < 300 ms)	V_{CC}	32	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	Internally Limited	W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Feedback Input Voltage	V_{fb}	−1.5 to +30	Vdc
Shutdown Input Voltage	V_{sd}	−0.3 to +30	Vdc
Error Comparator Output Voltage	V_{err}	−0.3 to +30	Vdc
Operating Ambient Temperature Range	T_A	−40 to +150	°C
Maximum Die Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002
2. Latch−up Current Maximum Rating tested per AEC−Q100−004 standard:
   − Inputs Low: passing positive current 100 mA and negative current −100 mA
   − Inputs High: passing positive current 100 mA and negative current −10 mA.

ELECTRICAL CHARACTERISTICS

(V_{in} = V_O + 1.0 V, I_O = 100 μA, C_O = 1.0 μF, T_A = 25°C [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions	V_O				V
V_{in} = 6.0 V, I_O = 100 μA, T_J = 25°C		4.975	5.000	5.025	
V_{in} = 6.0 to 30 V, I_O = 100 μA to 100 mA, T_J = −40 to +150°C		4.9	–	5.1	
Line Regulation (V_{in} = $V_{O(nom)}$ +1.0 V to 30 V)	Reg_{line}	–	0.04	0.10	%
Load Regulation (I_O = 100 μA to 100 mA)	Reg_{load}	–	0.05	0.10	%
Dropout Voltage	$V_I - V_O$				mV
I_O = 100 μA		–	30	80	
I_O = 100 mA		–	350	450	
Supply Bias Current	I_{CC}				
I_O = 100 μA		–	93	120	μA
I_O = 100 mA		–	4.0	12	mA
Dropout Supply Bias Current (V_{in} = $V_{O(nom)}$ − 0.5 V, I_O = 100 μA)	$I_{CCdropout}$	–	110	170	μA
Current Limit (V_O Shorted to Ground)	I_{Limit}	–	220	300	mA
Thermal Regulation	$Reg_{thermal}$	–	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) (Note 4)	V_n				μVrms
C_L = 1.0 μF		–	126	–	
C_L = 100 μF		–	56	–	
Reference Voltage (T_A = 25°C)	V_{ref}	1.220	1.235	1.250	V
Reference Voltage (T_A = −40 to +150°C)	V_{ref}	1.200	–	1.260	V
Reference Voltage (T_A = −40 to +150°C)	V_{ref}				V
I_O = 100 μA to 100 mA, V_{in} = 23 to 30 V		1.190	–	1.270	
Feedback Pin Bias Current	I_{FB}	–	15	40	nA
ERROR COMPARATOR					
Output Leakage Current (V_{OH} = 30 V)	I_{lkg}	–	0.01	1.0	μA
Output Low Voltage (V_{in} = 4.5 V, I_{OL} = 400 μA)	V_{OL}	–	150	250	mV
Upper Threshold Voltage (V_{in} = 6.0 V)	V_{thu}	40	45	–	mV
Lower Threshold Voltage (V_{in} = 6.0 V)	V_{thl}	–	60	95	mV
Hysteresis (V_{in} = 6.0 V)	V_{hy}	–	15	–	mV
SHUTDOWN INPUT					
Input Logic Voltage	V_{shtdn}				V
Logic “0” (Regulator “On”)		0	–	0.7	
Logic “1” (Regulator “Off”)		2.0	–	30	
Shutdown Pin Input Current	I_{shtdn}				μA
V_{shtdn} = 2.4 V		–	35	50	
V_{shtdn} = 30 V		–	450	600	
Regulator Output Current in Shutdown Mode (V_{in} = 30 V, V_{shtdn} = 2.0 V, V_O = 0, Pin 6 Connected to Pin 7)	I_{off}	–	3.0	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. Noise tests on the SCV2951 are made with a 0.01 μF capacitor connected across Pins 7 and 1.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The RMS ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Leakage Current – Current drawn through a bipolar transistor collector−base junction, under a specified collector voltage, when the transistor is “off”.

Upper Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “0” to “1”.

Lower Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “1” to “0”.

Hysteresis – The difference between Lower Threshold voltage and Upper Threshold voltage.

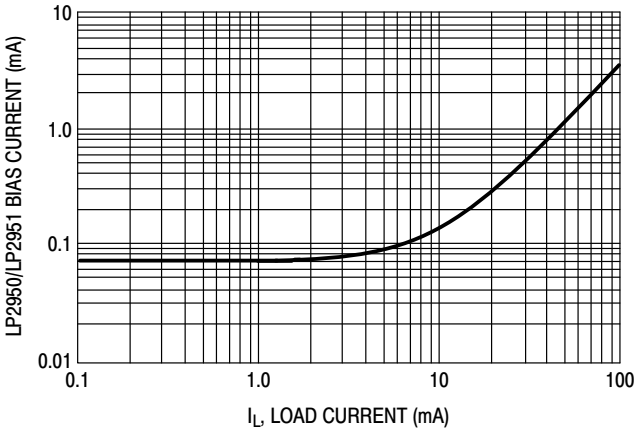


Figure 2. Quiescent Current

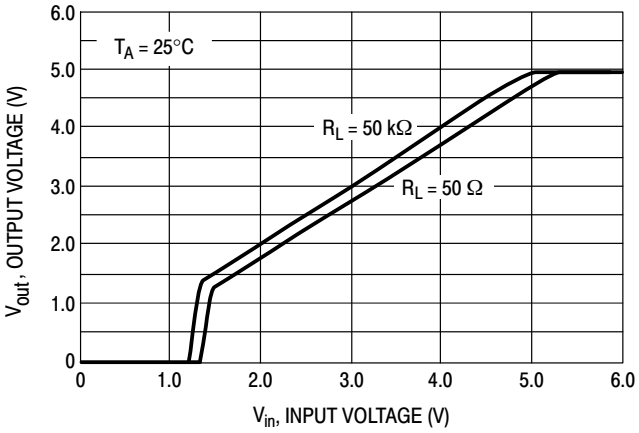


Figure 3. 5.0 V Dropout Characteristics over Load

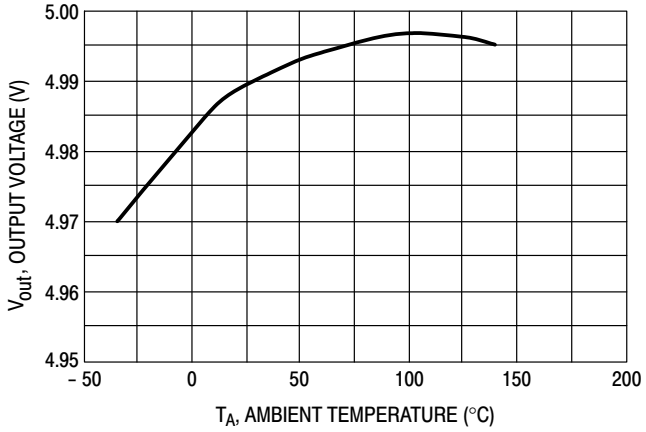


Figure 4. Output Voltage versus Temperature

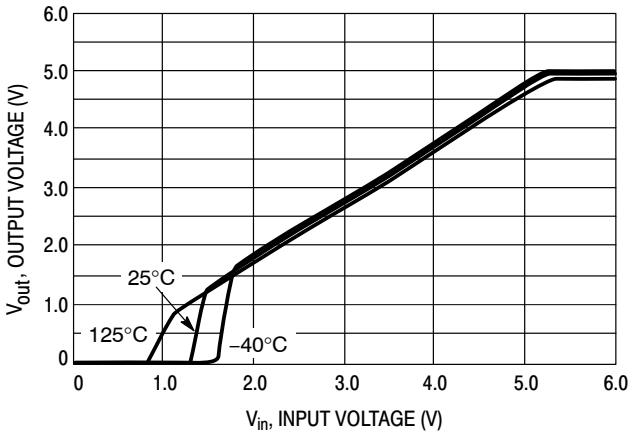


Figure 5. 5.0 V Dropout Characteristics with R_L = 50 Ω

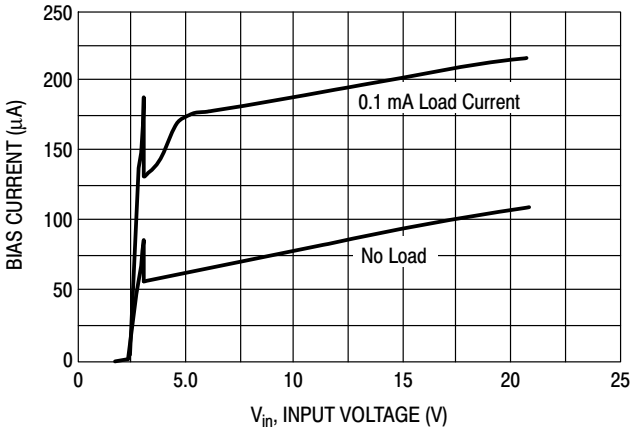


Figure 6. Input Current

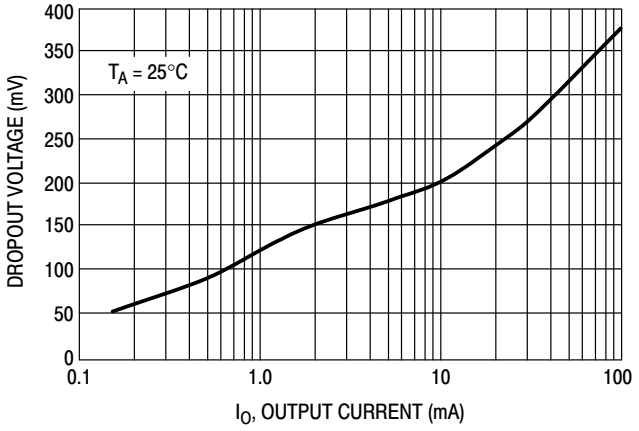


Figure 7. Dropout Voltage versus Output Current

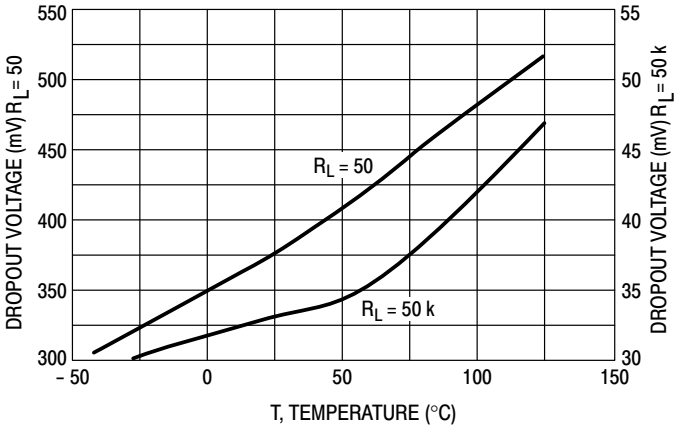


Figure 8. Dropout Voltage versus Temperature

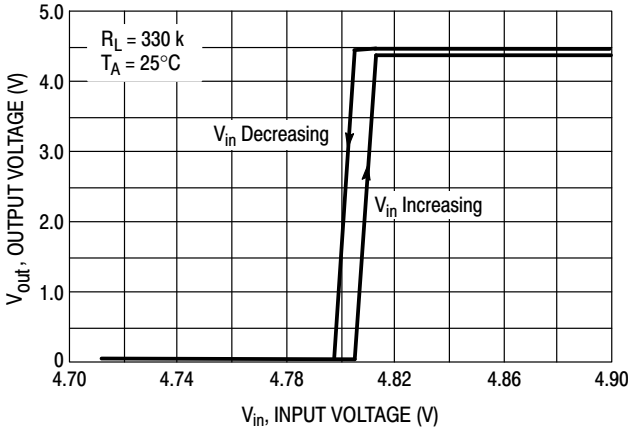


Figure 9. Error Comparator Output

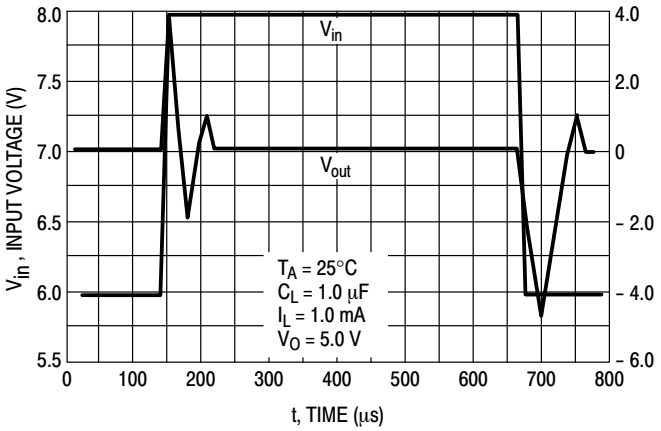


Figure 10. Line Transient Response

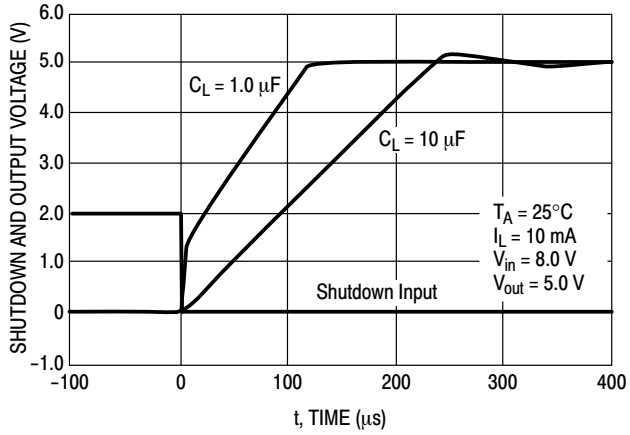


Figure 11. SCV2951 Enable Transient

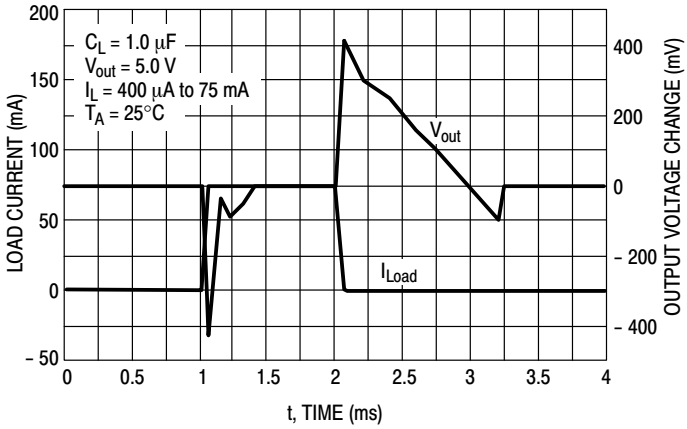


Figure 12. Load Transient Response

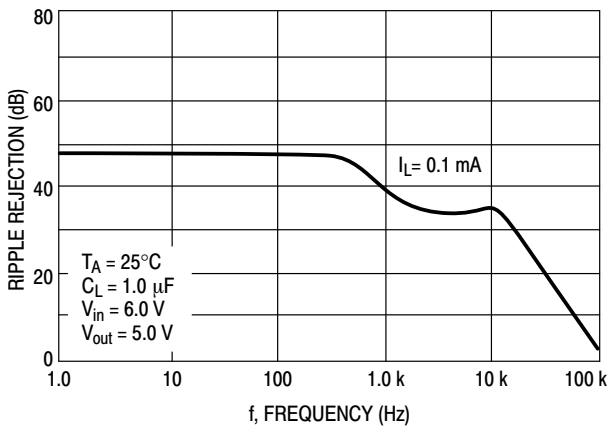


Figure 13. Ripple Rejection

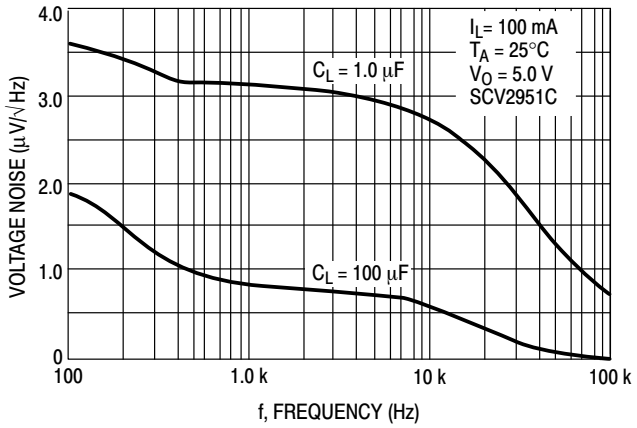


Figure 14. Output Noise

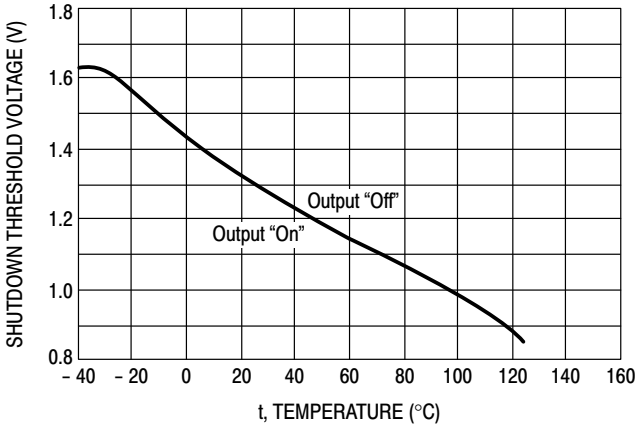


Figure 15. Shutdown Threshold Voltage versus Temperature

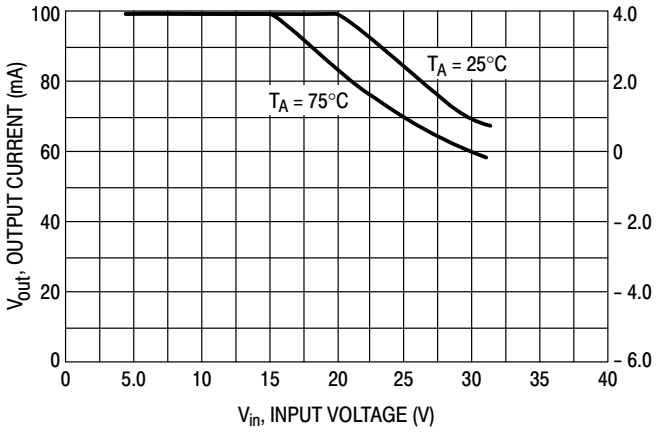


Figure 16. Maximum Rated Output Current

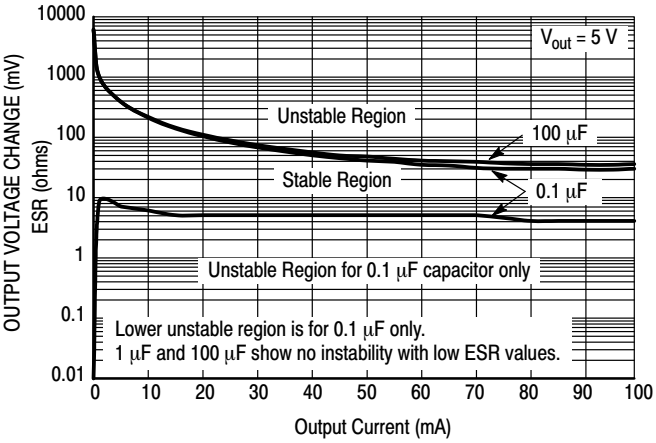


Figure 17. Output Stability versus Output Capacitor Change

APPLICATIONS INFORMATION

Introduction

The SCV2951 regulator is designed with internal current limiting and thermal shutdown making them user−friendly. Typical application circuits for the SCV2951 are shown in Figures 20 through 28.

This regulator is not internally compensated and thus require a 1.0 μF (or greater) capacitance between the SCV2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33 μF for currents less than 10 mA, or 0.1 μF for currents below 1.0 mA. Using the 8 pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (output Pin 1 connected to the feedback Pin 7) a minimum capacitance of 3.3 μF is recommended.

When setting the output voltage of the SCV2951 with external resistors, the resistance values should be chosen to draw a minimum of 1.0 μA.

A bypass capacitor is recommended across the SCV2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor.

Input capacitance at the SCV2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least 3.3 μF will stabilize the feedback loop.

Error Detection Comparator

The comparator switches to a positive logic low whenever the SCV2951 output voltage falls more than approximately 5.0% out of regulation. This value is the comparator's designed−in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains 5.0% below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

Figure 2 is a timing diagram which shows the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the input voltage to the SCV2951 is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V (V_{out} exceeds about 4.75 V). Since the SCV2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.

The error comparator output is an open collector which requires an external pullup resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the 400 μA sink capability of the error comparator. A value between 100 kΩ and 1.0 MΩ is suggested. No pullup resistance is required if this output is unused.

When operated in the power down mode (V_{in} = 0 V), the error comparator output will go high if it has been pulled up to an external supply (the output transistor is in high impedance state). To avoid this invalid response, the error comparator output should be pulled up to V_{out} (see Figure 18).

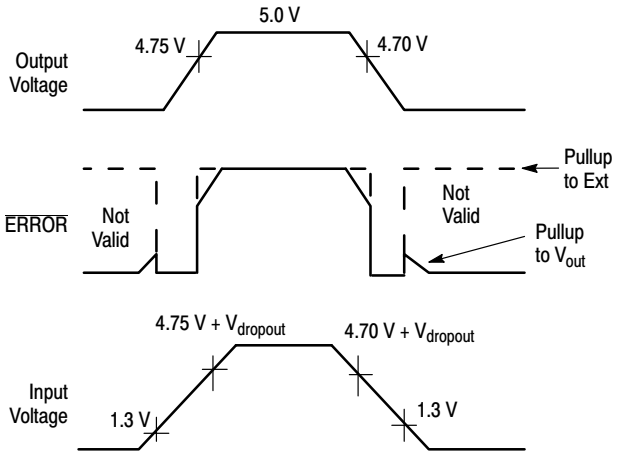


Figure 18. $\overline{\text{ERROR}}$ Output Timing

Programming the Output Voltage

The SCV2951 may be pin−strapped for the nominal fixed output voltage using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 19.

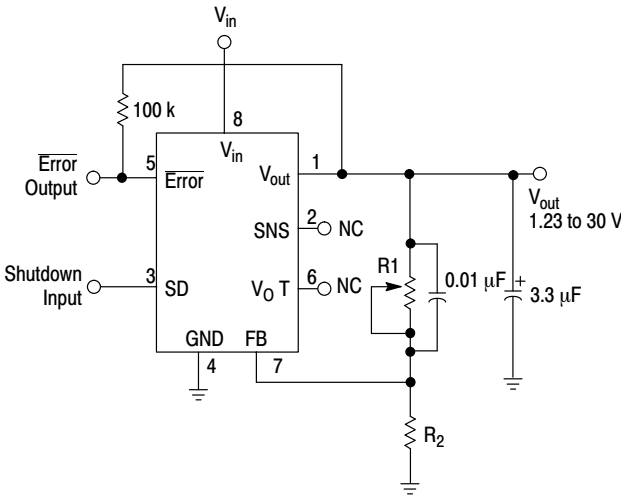


Figure 19. Adjustable Regulator

The complete equation for the output voltage is:

$$V_{out} = V_{ref}(1 + R1/R2) + I_{FB} R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1.0 μA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the SCV2951 typically draws 75 μA at no load with Pin 2 open circuited, the extra 12 μA of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise on the 3 lead LP2950. However, increasing the capacitor from 1.0 μF to 220 μF only decreases the noise from 430 μV to 160 μVrms for a 100 kHz bandwidth at the 5.0 V output.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{Bypass} \approx \frac{1}{2\pi R1 \times 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 126 μVrms for a 100 kHz bandwidth at 5.0 V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

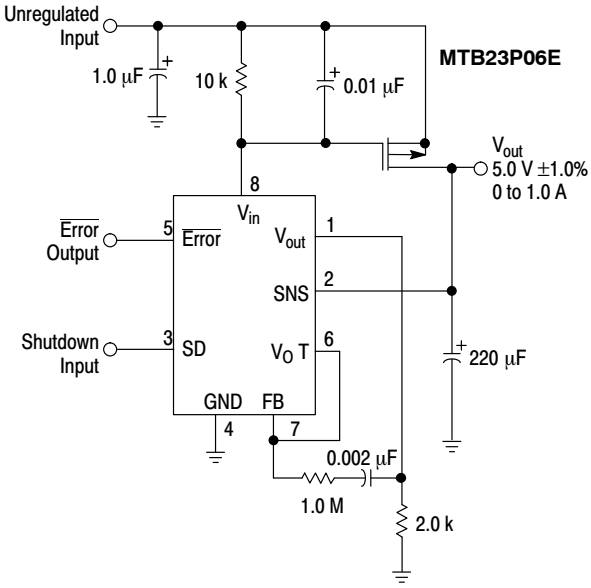


Figure 20. 1.0 A Regulator with 1.2 V Dropout

TYPICAL APPLICATIONS

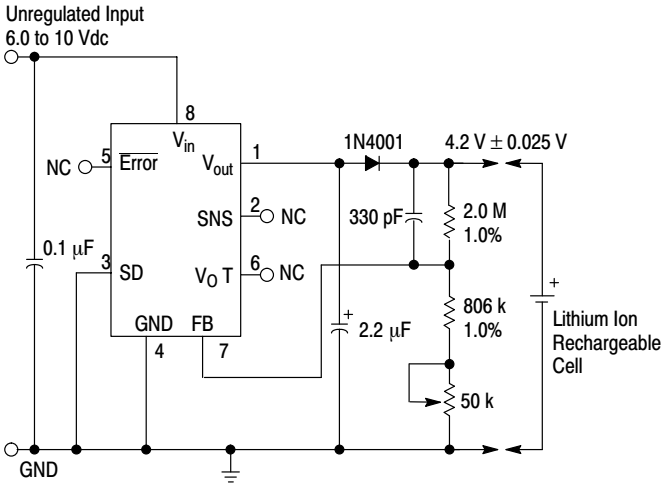


Figure 21. Lithium Ion Battery Cell Charger

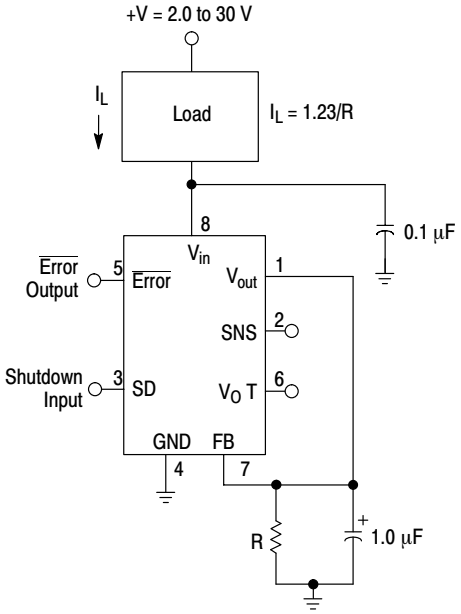
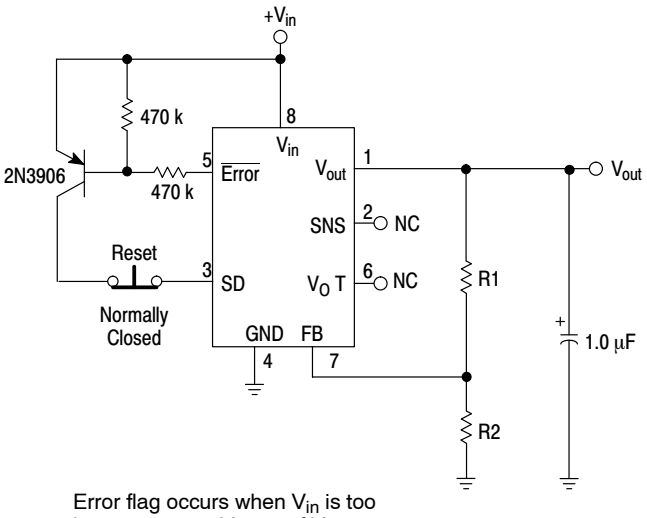


Figure 22. Low Drift Current Sink



Error flag occurs when V_{in} is too low to maintain V_{out}, or if V_{out} is reduced by excessive load current.

Figure 23. Latch Off When Error Flag Occurs

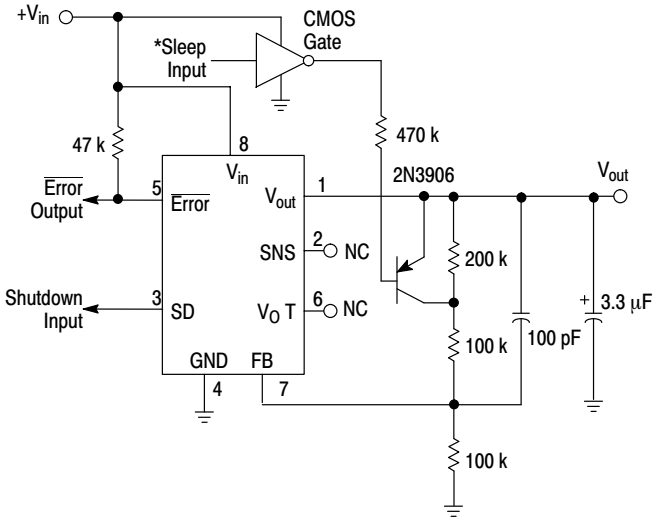
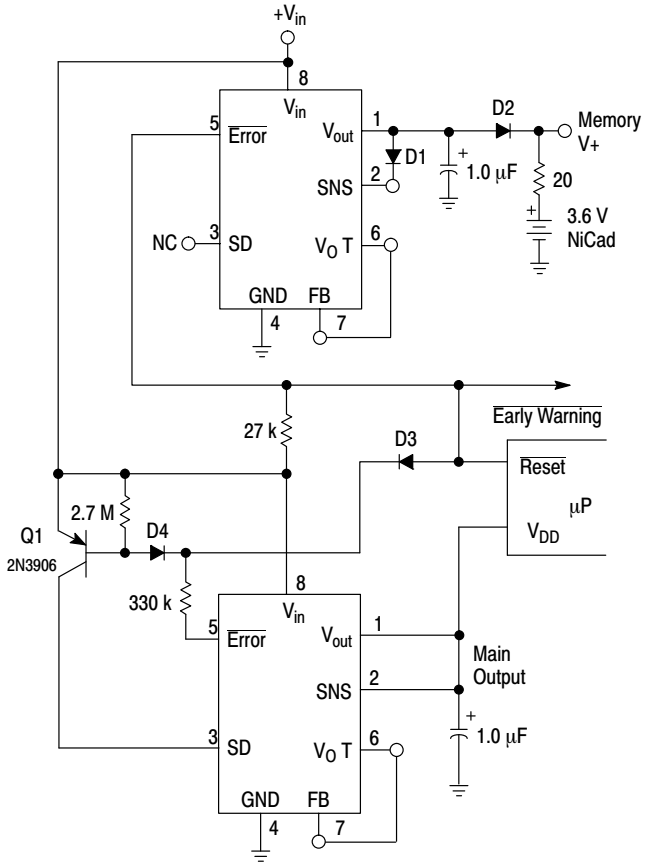


Figure 24. 5.0 V Regulator with 2.5 V Sleep Function



All diodes are 1N4148.

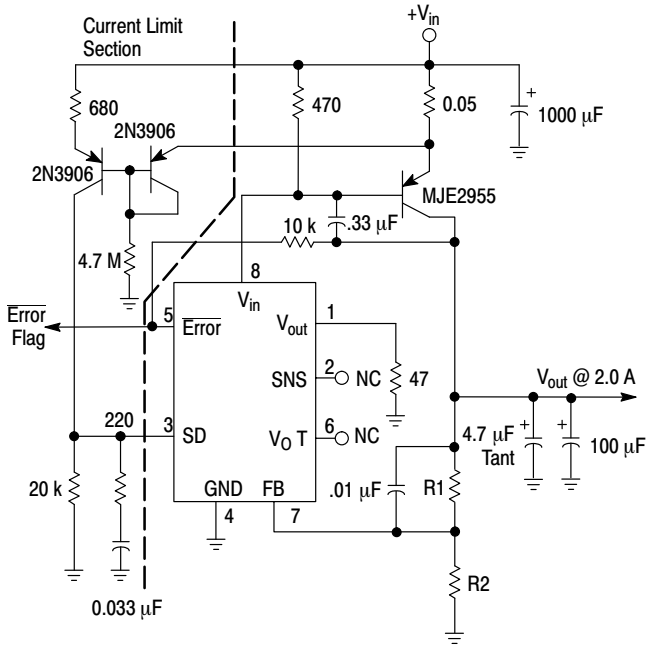
Early Warning flag on low input voltage.

Main output latches off at lower input voltages.

Battery backup on auxiliary output.

Operation: Regulator #1's V_{out} is programmed one diode drop above 5.0 V. Its error flag becomes active when $V_{in} \leq 5.7$ V. When V_{in} drops below 5.3 V, the error flag of regulator #2 becomes active and via Q1 latches the main output "off". When V_{in} again exceeds 5.7 V, regulator #1 is back in regulation and the early warning signal rises, unlatching regulator #2 via D3.

Figure 25. Regulator with Early Warning and Auxiliary Output



V_{out} = 1.25V (1.0 + R1/R2)

For 5.0 V output, use internal resistors. Wire Pin 6 to 7, and wire Pin 2 to +V_{out} Bus.

Figure 26. 2.0 A Low Dropout Regulator

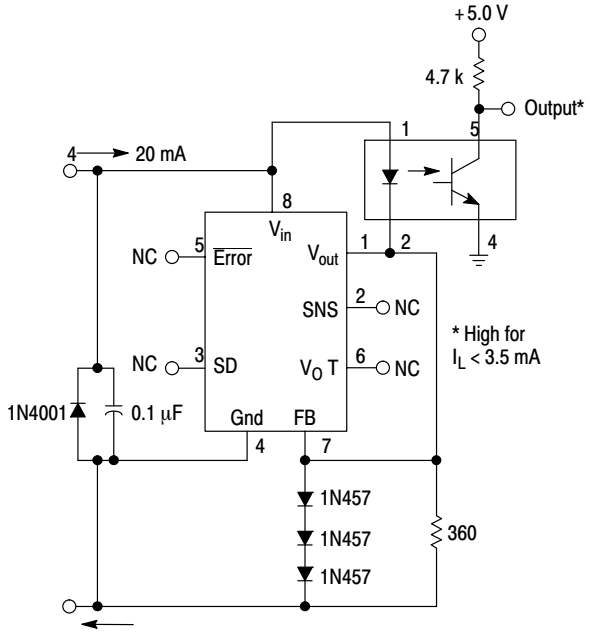


Figure 27. Open Circuit Detector for 4.0 to 20 mA Current Loop

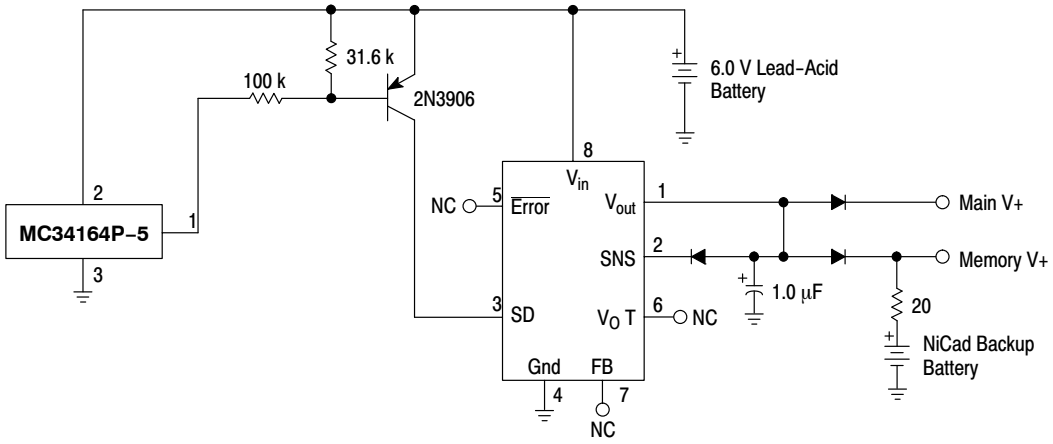


Figure 28. Low Battery Disconnect

ORDERING INFORMATION

Part Number	Output Voltage (V)	Tolerance (%)	Package	Shipping†
SCV2951ACDR2G	5.0 or Adj.	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

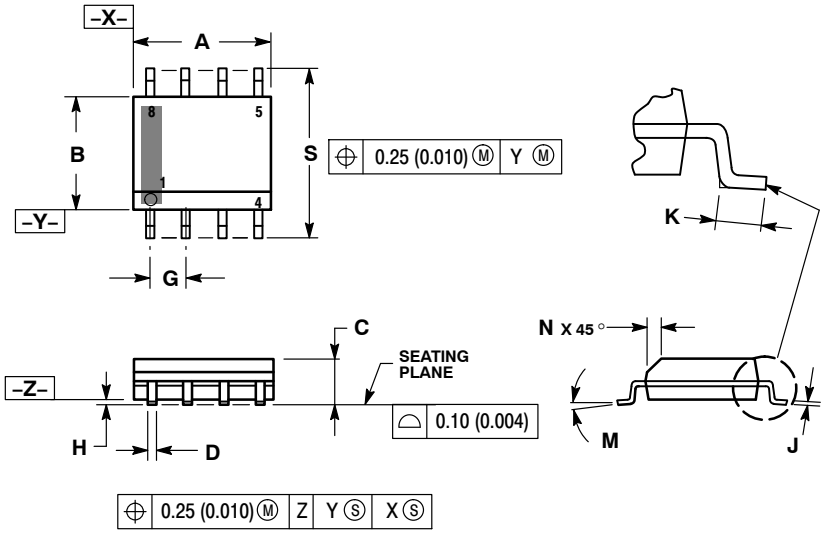
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

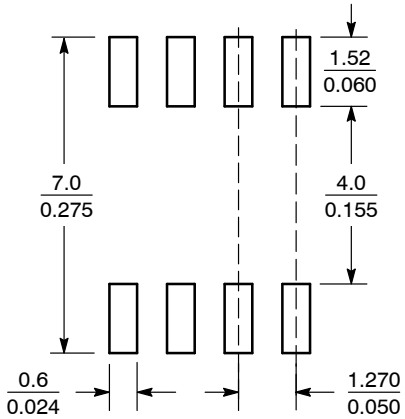
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

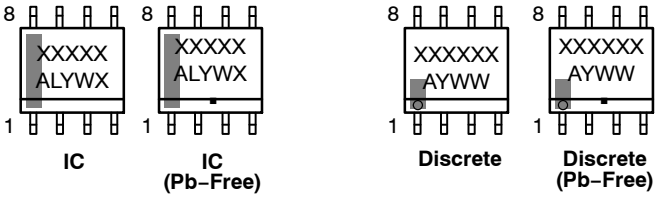
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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