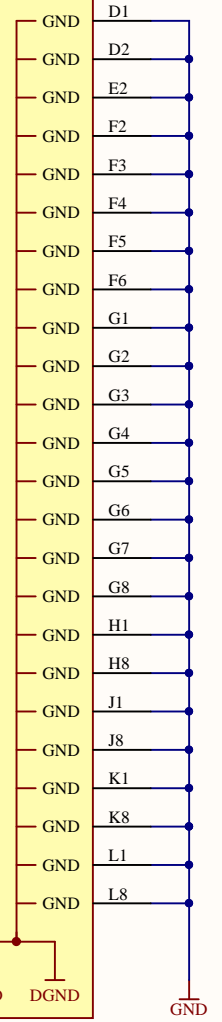
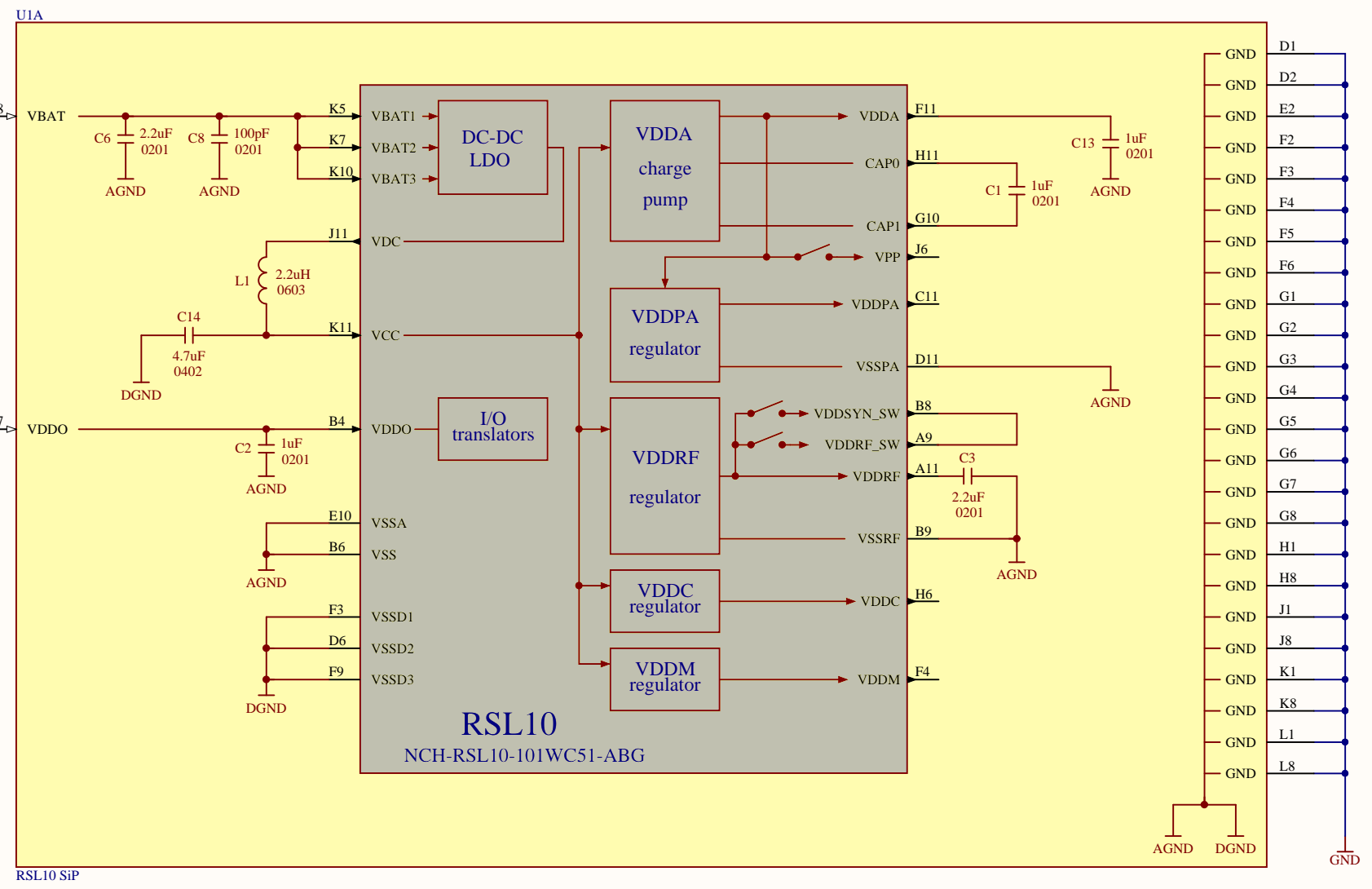
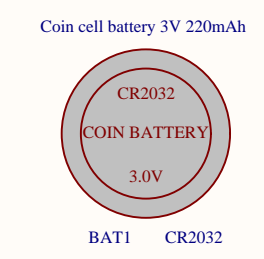
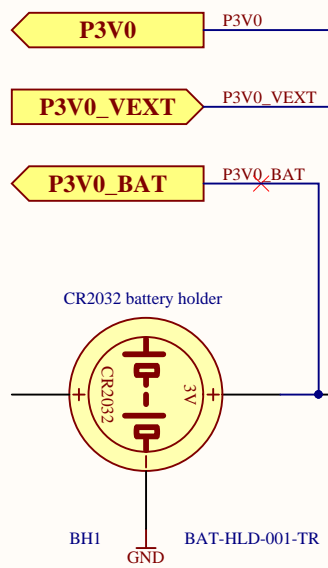


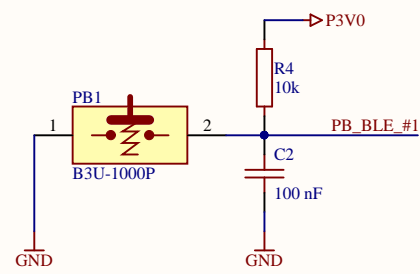
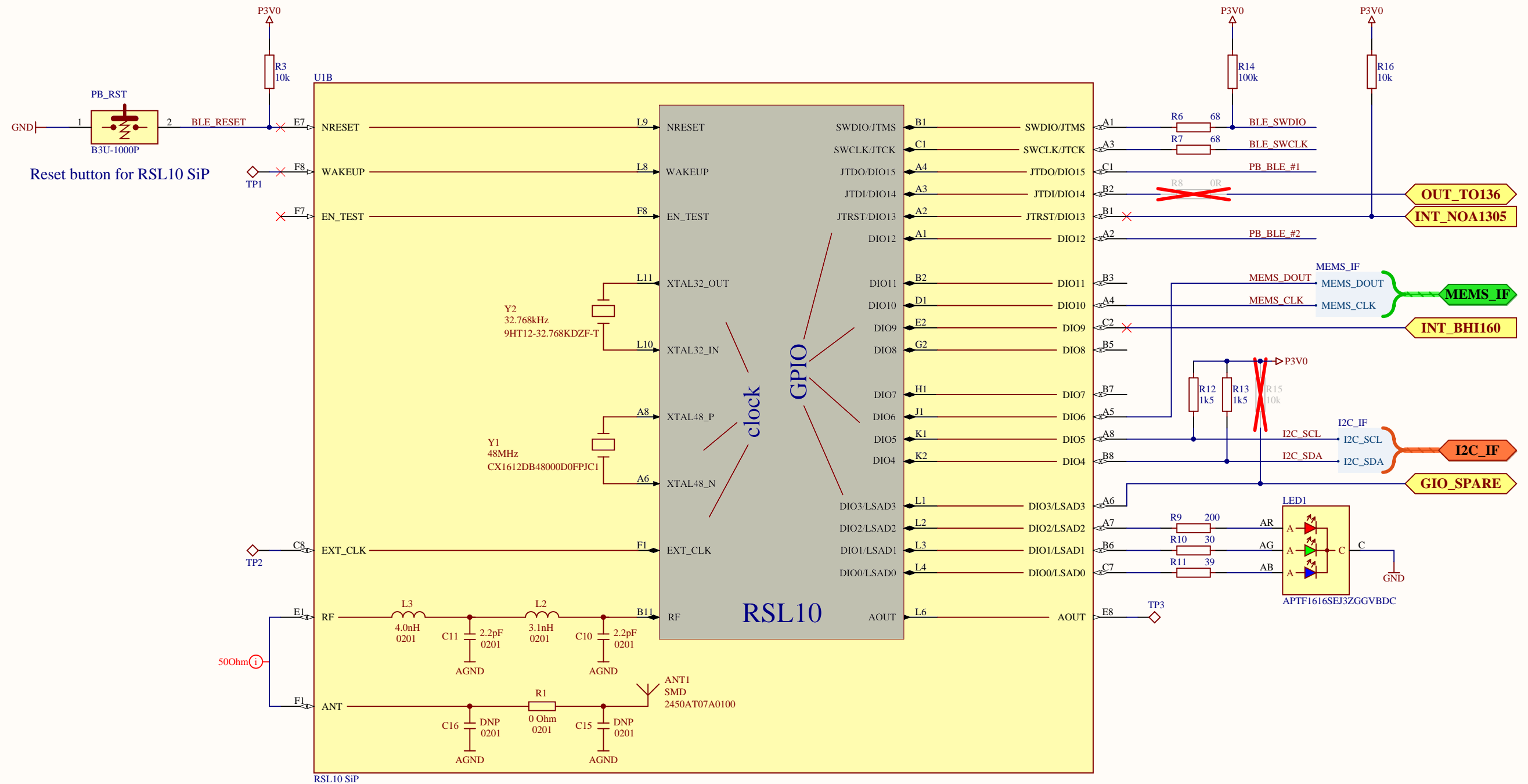
RSL10-SENSE-DB-GEVB		Assembly variant:	State:
<i>Top level block diagram</i>		<i>standard_board</i>	<i>released</i>
Revision: 1.1	Repository revision: TBD		ON Semiconductor Solution Engineering Center Piešťany
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SENSE_DB_GEV.B.SchDoc	1/4		



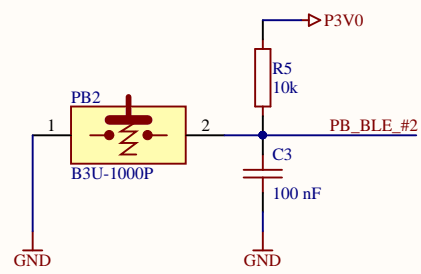


RSL10-SENSE-DB-GEVB		Assembly variant:	State:
<i>RSL10 SiP power management</i>		<i>standard_board</i>	<i>released</i>
Revision: 1.1	Repository revision: TBD		ON Semiconductor Solution Engineering Center Piešťany
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SiP_power.SchDoc	2/4		

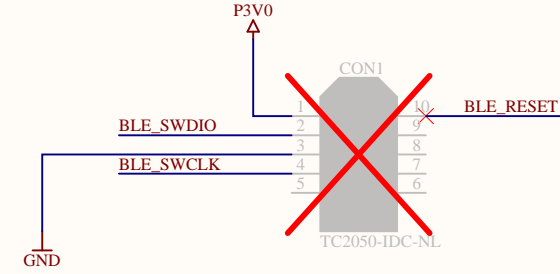




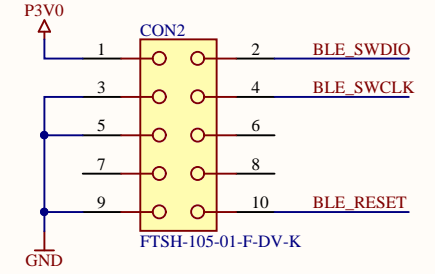
Programmable button #1



Programmable button #2

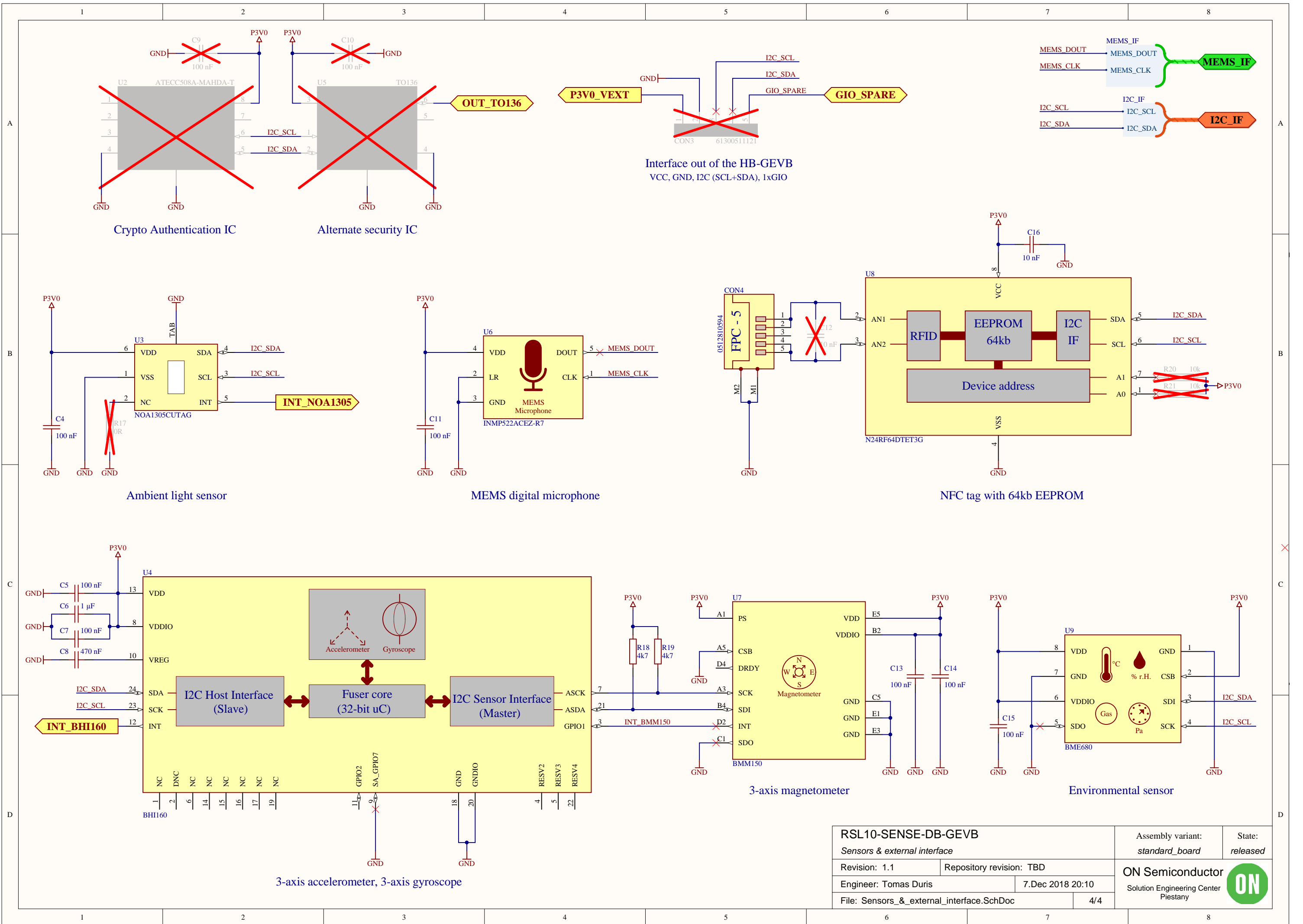


RSL10 SiP SW Debug & Programming



RSL10 SiP SW Debug

RSL10-SENSE-DB-GEVB		Assembly variant:	State:
RSL 10 SiP signals		standard_board	released
Revision: 1.1	Repository revision: TBD	ON Semiconductor Solution Engineering Center Piestany	
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SiP_signals.SchDoc	3/4		



RSL10-SENSE-DB-GEVB		Assembly variant:	State:
Sensors & external interface		standard_board	released
Revision: 1.1	Repository revision: TBD	ON Semiconductor Solution Engineering Center Piešťany	
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: Sensors_&_external_interface.SchDoc	4/4		