MOSFET – Power, N-Channel

60 V, 50 A, 22 mΩ

RFP50N06

These N−Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developed type TA49018.

Features

- 50 A, 60 V
- $r_{DS(ON)} = 0.022\ \Omega$
- Temperature Compensating PSPICE™ Model
- Peak Current vs. Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- This Device is Pb−Free and is RoHS Compliant

Specifications

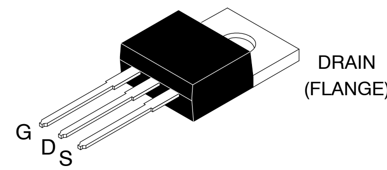
ABSOLUTE MAXIMUM RATINGS

(T_C = 25°C, unless otherwise specifieded)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain to Source Voltage (Note 1)		60	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20 kΩ) (Note 1)		60	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (Figure 2)	50	A
I_{DM}		Pulsed	(Figure 5)	
E_{AS}	Pulsed Avalanche Rating		(Figure 6)	
P_D	Power Dissipation Linear Derating Factor		131 0.877	W W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 175	°C
T_L	Maximum Temperature for Soldering Leads at 0.063 inch (1.6 mm) from Case for 10 s		300	°C
T_{pkg}	Maximum Temperature for Soldering Package Body for 10 s, see Techbrief 334		260	°C

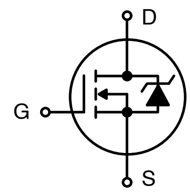
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. T_J = 25°C to 150°C

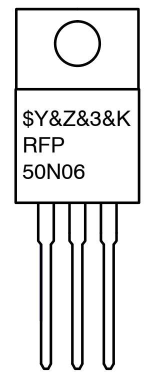


TO−220−3LD
CASE 340AT

SYMBOL



MARKING DIAGRAM



$Y	=	**onsemi** Logo
&Z	=	Assembly Plant Code
&3	=	Date Code (Year & Week)
&K	=	Lot
RFP50N06	=	Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
RFP50N06	TO−220−3LD (Pb−Free)	800 units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250 μA, V_{GS} = 0 V (Figure 11)		60	–	–	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA (Figure 10)		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	T_C = 25°C	–	–	1	μA
			T_C = 150°C	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		–	–	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 50 A, V_{GS} = 10 V (Figure 9)		–	–	0.022	Ω
Turn−On Time	t_{ON}	V_{DD} = 30 V, I_D = 50 A R_L = 0.6 Ω, V_{GS} = 10 V R_{GS} = 3.6 Ω (Figure 13)		–	–	95	ns
Turn−On Delay Time	$t_{d(ON)}$			–	12	–	ns
Rise Time	t_r			–	55	–	ns
Turn−Off Delay Time	$t_{d(OFF)}$			–	37	–	ns
Fall Time	t_f			–	13	–	ns
Turn−Off Time	t_{OFF}			–	–	75	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to 20 V	V_{DD} = 48 V, I_D = 50 A, R_L = 0.96 Ω $I_{g(REF)}$ = 1.45 mA (Figure 13)	–	125	150	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 to 10 V		–	67	80	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to 2 V		–	3.7	4.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz (Figure 12)		–	2020	–	pF
Output Capacitance	C_{OSS}			–	600	–	pF
Reverse Transfer Capacitance	C_{RSS}			–	200	–	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		–	–	1.14	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO−220		–	–	62	°C/W

SOURCE TO DRAIN DIODE CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 50 A	–	–	1.5	V
Output Capacitance	t_{rr}	I_{SD} = 50 A, dI_{SD}/dt = 100 A/μs	–	–	125	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified)

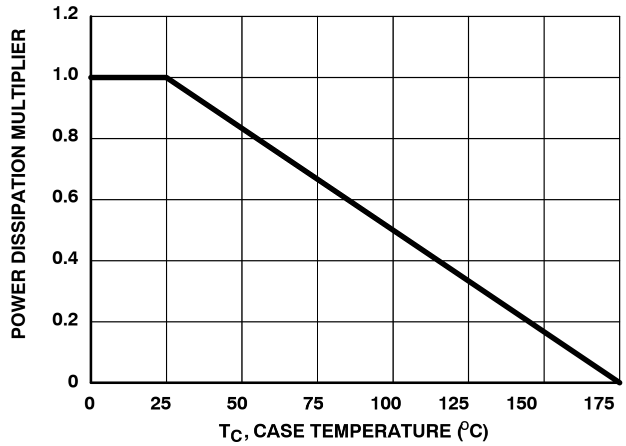


Figure 1. Normalized Power Dissipation vs. Case Temperature

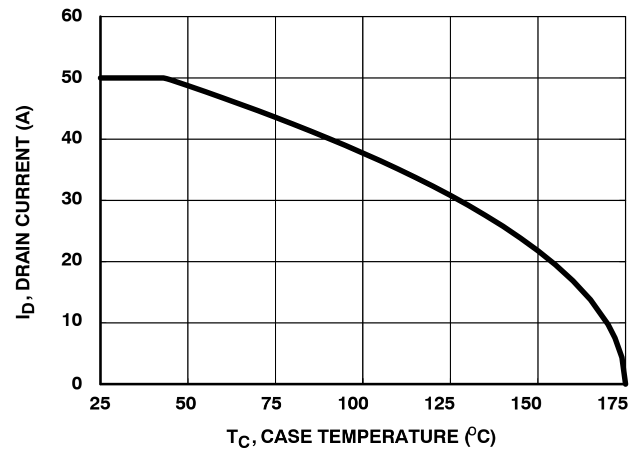


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

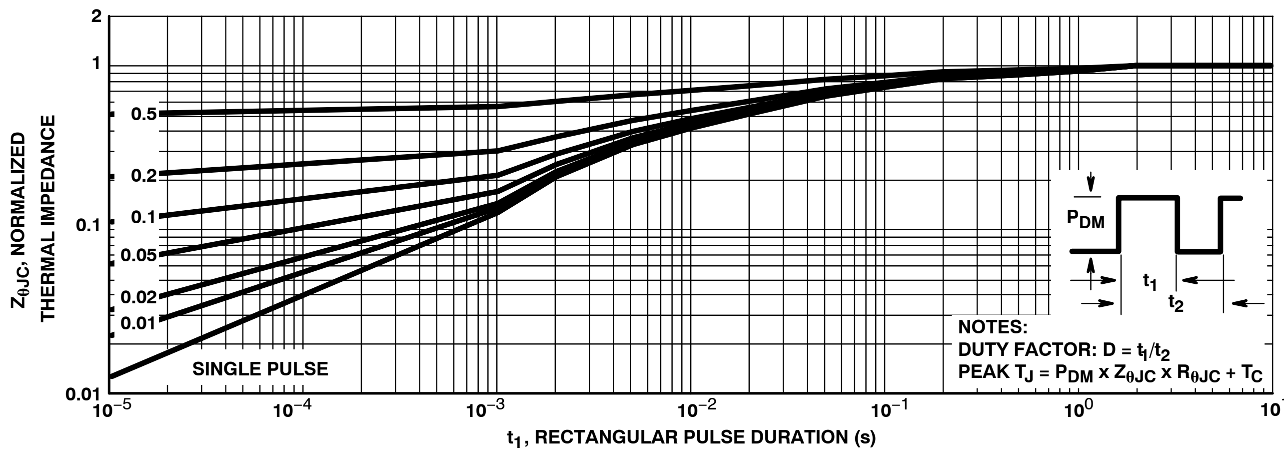


Figure 3. Normalized Maximum Transient Thermal Impedance

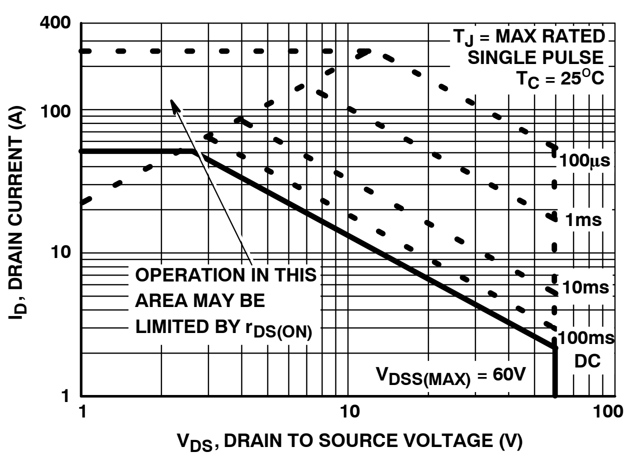


Figure 4. Forward Bias Safe Operating Area

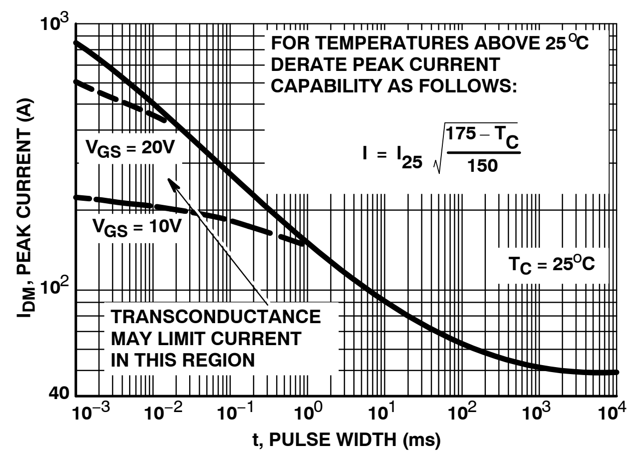


Figure 5. Peak Current Capability

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified) (continued)

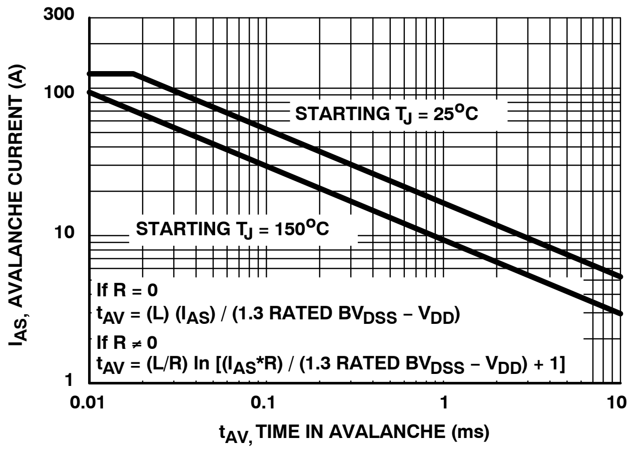


Figure 6. Unclamped Inductive Switching Capability

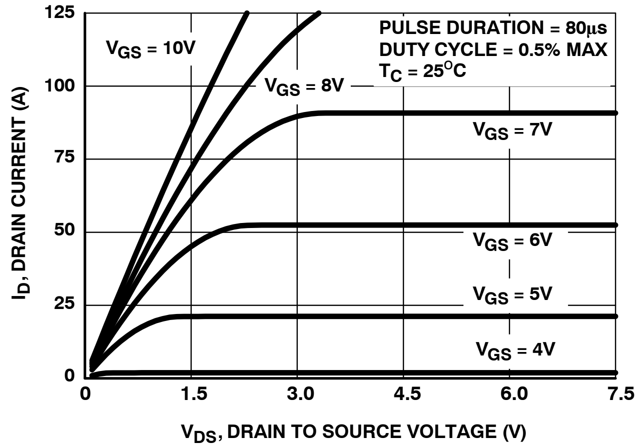


Figure 7. Saturation Characteristics

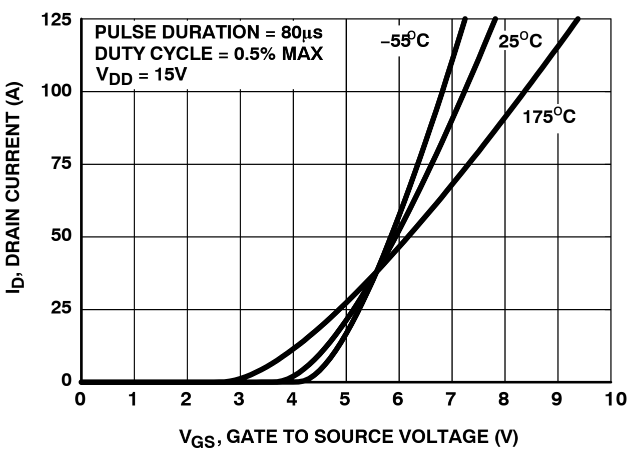


Figure 8. Transfer Characteristics

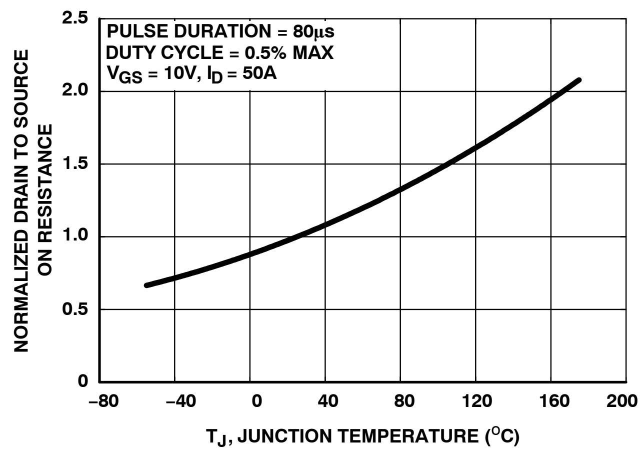


Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature

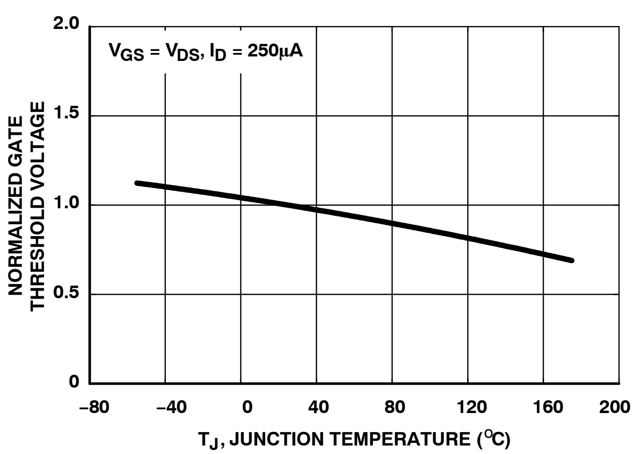


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

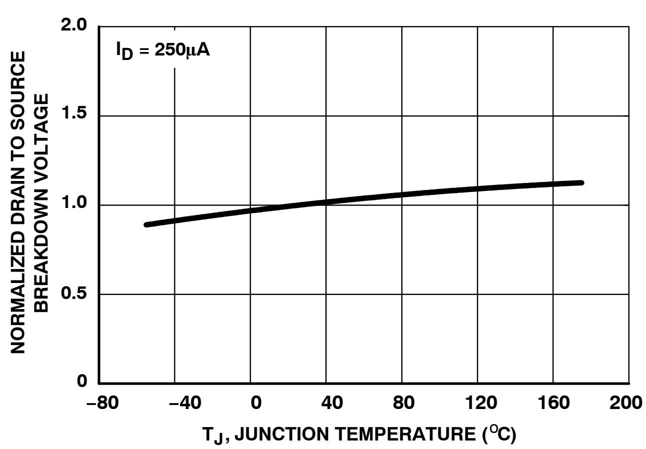


Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified) (continued)

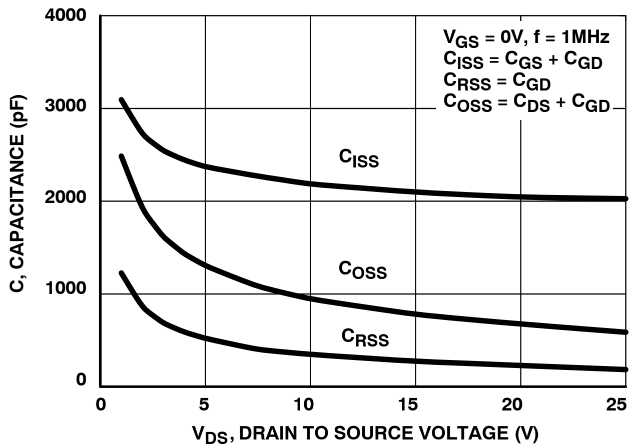


Figure 12. Capacitance vs. Drain to Source Voltage

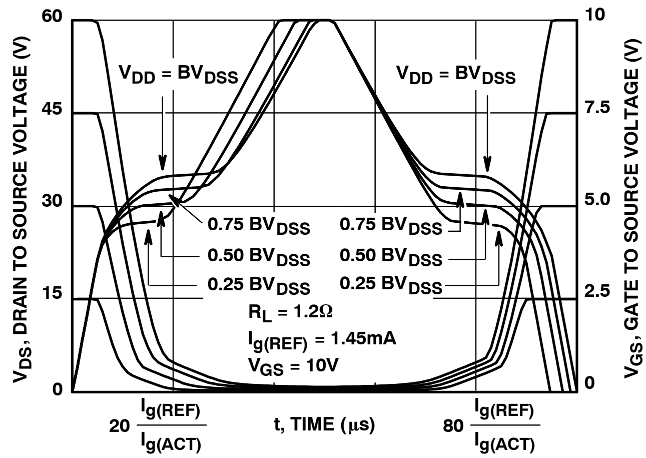


Figure 13. Normalized Switching Waveforms for Constant Gate Current

TEST CIRCUITS AND WAVEFORMS

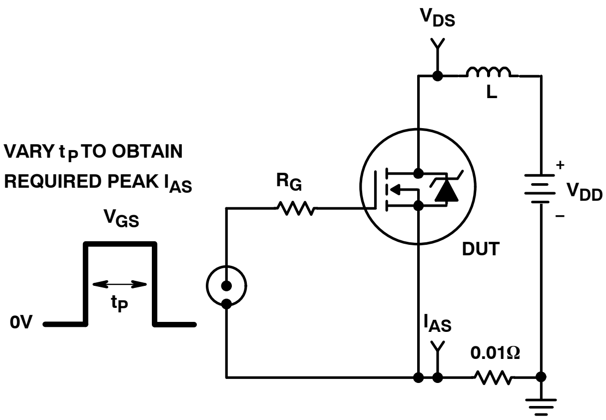


Figure 14. Unclamped Energy Test Circuit

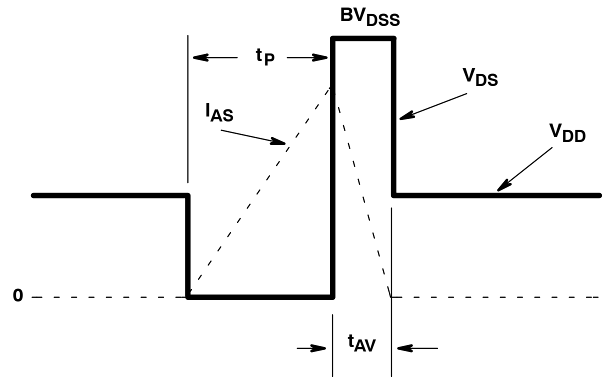


Figure 15. Unclamped Energy Waveforms

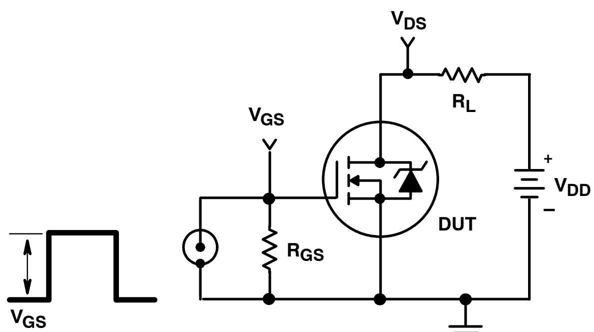


Figure 16. Switching Time Test Circuit

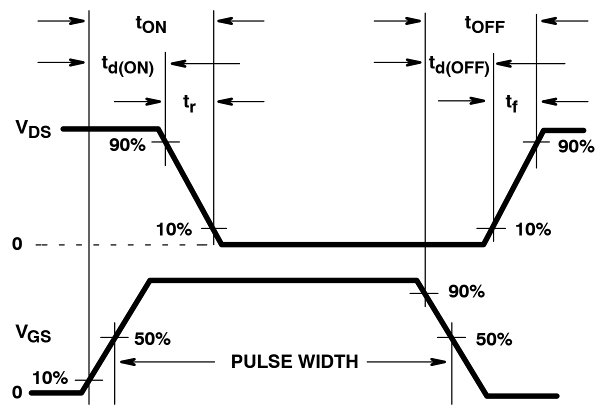


Figure 17. Switching Waveforms

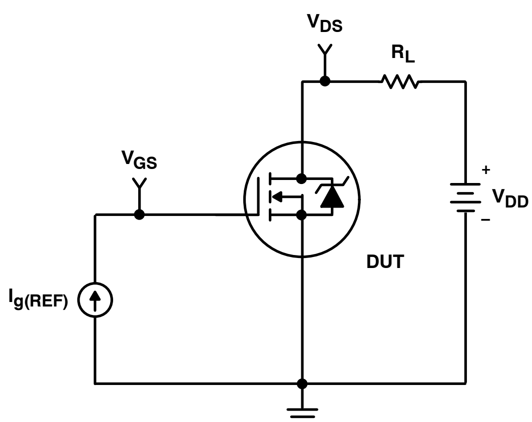


Figure 18. Gate Charge Test Circuit

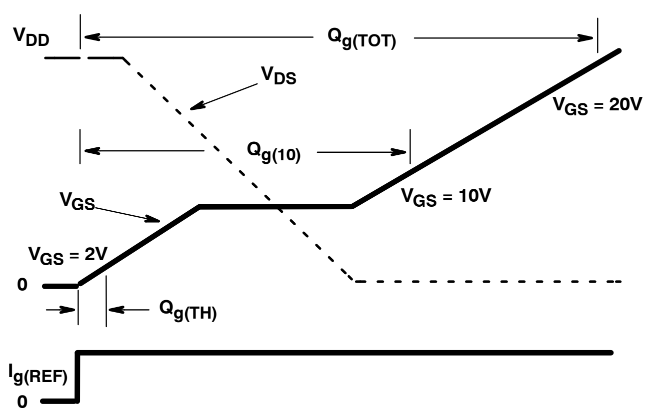


Figure 19. Gate Charge Waveforms

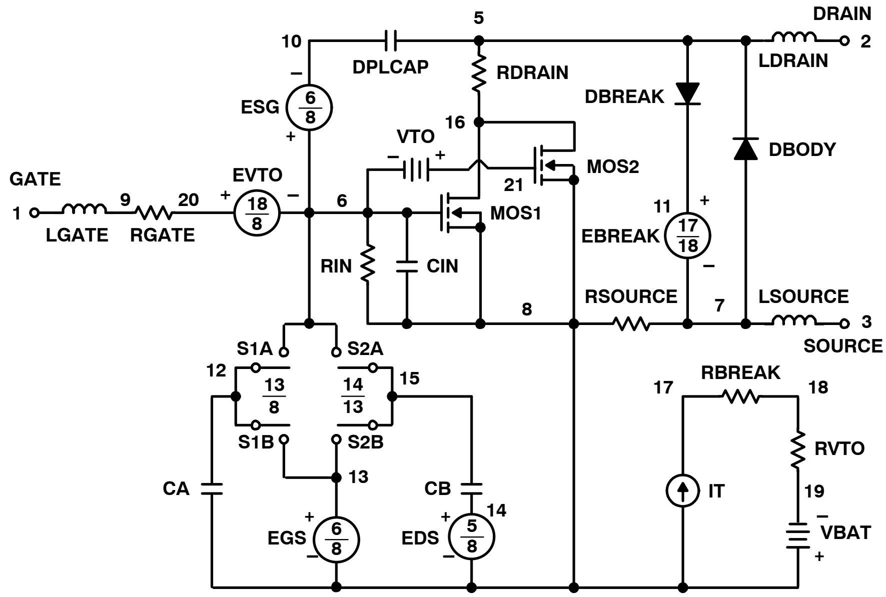
PSPICE ELECTRICAL MODEL

.SUBCKT RFP50N06213

REV 2/22/93

*NOM TEMP = 25°C

CA 12 8 3.68e–9
CB 15 14 3.625e–9
CIN 6 8 1.98e–9



DBODY 7 5 DBDMOD
DBREAK 5 11DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e–9
LGATE 1 9 5.65e–9
LSOURCE 3 7 4.13e–9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e–4
RGATE 9 20 0.690
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 12e–3
RVTO 18 19 RVTOMOD 1

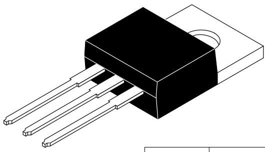
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.678

.MODEL DBDMOD D (IS=9.85e–13 RS=4.91e–3 TRS1=2.07e–3 TRS2=2.51e–7 CJO=2.05e–9 TT=4.33e–8)
.MODEL DBKMOD D (RS=1.98e–1 TRS1=2.35E–4 TRS2=–3.83e–6)
.MODEL DPLCAPMOD D (CJO=1.42e–9 IS=1e–30 N=10)
.MODEL MOSMOD NMOS (VTO=3.65 KP=35 IS=1e–30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.23e–3 TC2=–2.34e–7)
.MODEL RDSMOD RES (TC1=5.01e–3 TC2=1.49e–5)
.MODEL RVTOMOD RES (TC1=–5.03e–3 TC2=–5.16e–6)
.MODEL S1AMOD VSWITCH (RON=1e–5 ROFF=0.1 VON=–6.75 VOFF=–2.5)
.MODEL S1BMOD VSWITCH (RON=1e–5 ROFF=0.1 VON=–2.5 VOFF=–6.75)
.MODEL S2AMOD VSWITCH (RON=1e–5 ROFF=0.1 VON=–2.7 VOFF=2.3)
.MODEL S2BMOD VSWITCH (RON=1e–5 ROFF=0.1 VON=2.3 VOFF=–2.7)

.ENDS

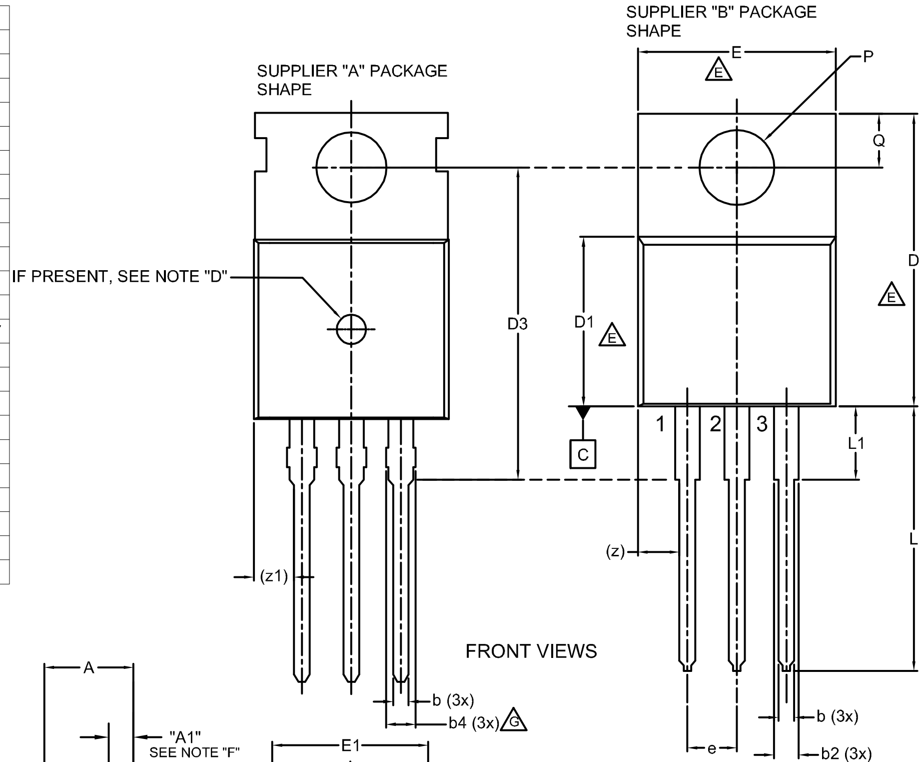
NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub–Circuit for the Power MOSFET Featuring Global Temperature Options;** authors, William J. Hepp and C. Frank Wheatley.



TO−220−3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
Θ	3°	--	5°



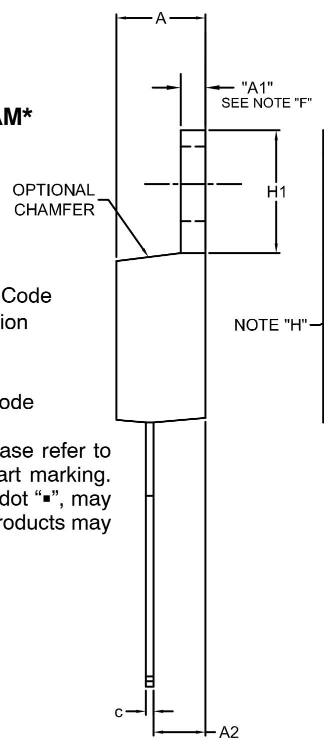
FRONT VIEWS

GENERIC MARKING DIAGRAM*

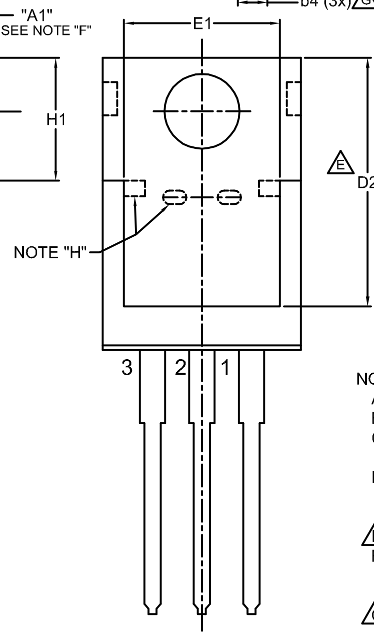
XXXXX
XXXXX
AYWWZZ

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

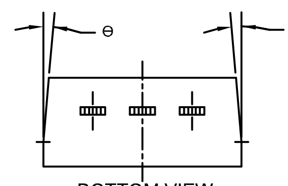
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



SIDE VIEW



BACK VIEW



BOTTOM VIEW

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	TO−220−3LD	PAGE 1 OF 1

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