

# PCGA200T65NF8M1

## 650 V, 200 A Field Stop Trench IGBT with Solderable Top Metal



ON Semiconductor®

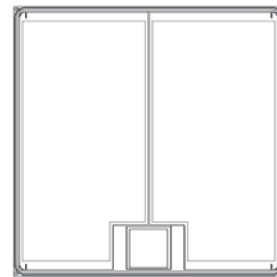
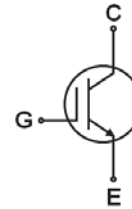
[www.onsemi.com](http://www.onsemi.com)

### Features

- AEC-Q101 Qualified
- Maximum Junction Temperature 175°C
- Positive Temperature Coefficient
- Easy Paralleling
- Short Circuit Rated
- Very Low Saturation Voltage:  $V_{CE(SAT)} = 1.53 \text{ V(Typ.) @ } I_C = 200 \text{ A}$
- Optimized for Motor Control Applications
- Emitter Pad Covered with Solderable Metal Layer

### Applications

- Automotive Traction Modules
- General Power Modules



### ORDERING INFORMATION

Part Number	PCGA200T65NF8M1	
Packing	Water (sawn on foil)	
	mils	$\mu\text{m}$
Die Size	394 × 394	10,000 × 10,000
Emitter Attach Area	2 × (177 × 348)	2 × (4,493.5 × 8,832)
Gate / Sensor Pad Attach Area	55 × 55	1,408 × 1,406
Die Thickness	3	79
Top Metal	5 $\mu\text{m}$ AlSiCu + 1.15 $\mu\text{m}$ Ti/NiV/Ag (STM)	
Back Metal	0.95 $\mu\text{m}$ NiV/Ag	
Topside Passivation	Silicon Nitride plus Polyimide	
Wafer Diameter	200 mm	
Max Possible Die Per Wafer	234	

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## ABSOLUTE MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Ratings	Units
Collector–Emitter Voltage	V <sub>CES</sub>	650	V
Gate–Emitter Voltage	V <sub>GES</sub>	±20	V
DC Collector Current, limited by T <sub>J</sub> max	I <sub>C</sub>	(Note 1)	A
Pulsed Collector Current, V <sub>GE</sub> =15 V, t <sub>p</sub> limited by T <sub>J</sub> max (Note 2)	I <sub>CM</sub>	600	A
Short Circuit Withstand Time, V <sub>GE</sub> = 15 V, V <sub>CE</sub> ≤ 400 V, T <sub>J</sub> ≤ 150°C	t <sub>sc</sub>	5	μs
Operating Junction Temperature	T <sub>J</sub>	–40 to +175	°C
Storage Temperature Range	T <sub>stg</sub>	+17 to +25	°C

1. Depends on the thermal properties of assembly
2. Not subject to production test – verified by design/characterization

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
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### Static Characteristics (Tested on wafers)

Collector–Emitter Breakdown Voltage	BV <sub>CES</sub>	V <sub>GE</sub> = 0 V, I <sub>C</sub> = 1 mA	650	–	–	V
Collector–Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> = 100 A, V <sub>GE</sub> = 15 V	–	1.25	1.75	V
Gate–Emitter Threshold Voltage	V <sub>GE(th)</sub>	V <sub>GE</sub> = V <sub>CE</sub> , I <sub>C</sub> = 200 mA	4.5	5.5	6.5	V
Collector Cut–Off Current	I <sub>CES</sub>	V <sub>CE</sub> = V <sub>CES</sub> , V <sub>GE</sub> = 0 V	–	–	40	μA
Gate Leakage Current	I <sub>GES</sub>	V <sub>GE</sub> = V <sub>GES</sub> , V <sub>CE</sub> = 0 V	–	–	±400	nA

### Electrical Characteristics (Not subjected to production test – verified by design/characterization)

Collector to Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> = 200 A, V <sub>GE</sub> = 15 V	T <sub>J</sub> = 25°C	–	1.53	1.9	V
			T <sub>J</sub> = 175°C	–	2.04	–	V
Input Capacitance	C <sub>IES</sub>	V <sub>CE</sub> = 30 V, V <sub>GE</sub> = 0 V f = 1 MHz	–	9.6	–	nF	
Output Capacitance	C <sub>OES</sub>		–	445	–	pF	
Reverse Transfer Capacitance	C <sub>RES</sub>		–	78	–	pF	
Internal Gate Resistance	R <sub>G</sub>	f = 1 MHz	–	2.0	–	Ω	
Total Gate Charge	Q <sub>G(Total)</sub>	V <sub>CE</sub> = 400 V, I <sub>C</sub> = 200 A V <sub>GE</sub> = 15 V	–	229	–	nC	
Gate–to–Emitter Charge	Q <sub>GE</sub>		–	66	–	nC	
Gate–to–Collector Charge	Q <sub>GC</sub>		–	64	–	nC	
Turn–On Delay Time	t <sub>d(on)</sub>	V <sub>CE</sub> = 400 V, I <sub>C</sub> = 200 A R <sub>G</sub> = 15 Ω V <sub>GE</sub> = 15 V Inductive Load T <sub>J</sub> = 25°C	–	67	–	ns	
Rise Time	t <sub>r</sub>		–	233	–	ns	
Turn–Off Delay Time	t <sub>d(off)</sub>		–	118	–	ns	
Fall Time	t <sub>f</sub>		–	177	–	ns	
Turn–On Delay Time	t <sub>d(on)</sub>	V <sub>CE</sub> = 400 V, I <sub>C</sub> = 200 A R <sub>G</sub> = 15 Ω V <sub>GE</sub> = 15 V Inductive Load T <sub>J</sub> = 175°C	–	64	–	ns	
Rise Time	t <sub>r</sub>		–	236	–	ns	
Turn–Off Delay Time	t <sub>d(off)</sub>		–	124	–	ns	
Fall Time	t <sub>f</sub>		–	208	–	ns	

3. For ordering, technique and other information on Onsemi automotive bare die products, please contact [automotivebaredie@onsemi.com](mailto:automotivebaredie@onsemi.com)

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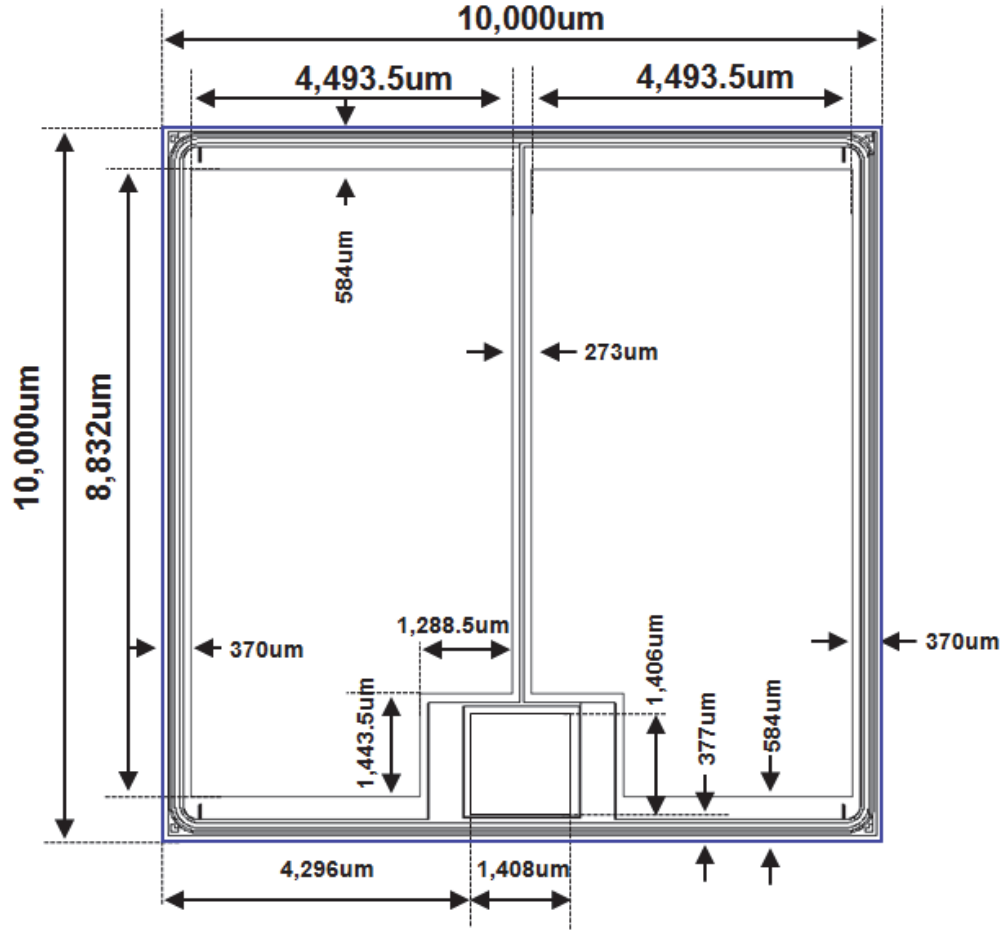



Figure 1. Dimensional Outline and Pad Layout

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