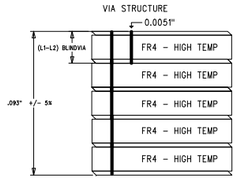
REVISIONS					
REV	ECO	DESCRIPTION	ORG	DATE	CHECK
B	N/A	INITIAL RELEASE	XX	2017-NOV-29	XX

6 LAYER LAMINATE STRUCTURE



LAYER DESCRIPTION	Cu WT OZ	SE IMP OHMS	SE Tw	REF LAYER	DIFF IMP OHMS	DIFF Tw/Ts	REF LAYER
L01-TOP (DUT) SIDE	1.00	50	0.007"	L02	90	0.0075"/0.0075"	L02
L02-GND1	1.00						
L03-PVDD_DVDD	1.00						
L04-SIGNAL	1.00	50	0.007"	L02 & L05			
L05-GND2	1.00						
L06-BOTTOM	1.00	50	0.007"	L05	90	0.0075"/0.0075"	L05

BOARD THICK: 0.093" +/-5%

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER DTS FAB SPEC & IPC-6012, CLASS 2.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSION OF CIRCUIT FEATURES IN THE PROVIDED MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES: ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.

2. DIELECTRIC MATERIAL:
   A. FR-4 HIGH TEMP
   B. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS.
   C. THICKNESS OF DIELECTRIC LAYERS IS VENDORS OPTION SEE LAYER STACK UP FOR INDICATED TRACE WIDTHS AND IMPEDANCE REQUIREMENTS.

3. DRILLING:
   A. ALL DRILLS ARE FINISHED HOLE SIZES.
   B. FILL 0.005" DRILL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATED WITH COPPER .005(.0002) MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025(.001)MAXIMUM.THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED. MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS. PLEASE SEE "D11-101605-B185" DATA.
   C. FOR L1-L2 0.0051" BLIND VIAS ARE SOLID CU FILLED. DIMPLE DEPTH IN BGA PADS SHALL BE .025 (0.001) MAXIMUM. FOR EPOXY FILL, OVERPLATE WITH COPPER, .005 (.002) MINIMUM AND THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS, NO MINIMUM MEASUREMENT REQUIRED. MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS. SEE "D11-101605-B185".
   D. THE DRILLS 0.005" & 0.0051" CAN FINISH AT 0.005".

4. SOLDERMASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR GREEN.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON U1 SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. FINAL FINISH:

   FINAL FINISH SHALL BE FLUSH GOLD.

7. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/-10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.
   C. CONTROLLED TRACES ARE LESS THAN 3 INCHES LONG ON THE TESTER SIDE. ADD A COUPON FOR IMPEDANCE VERIFICATION IF NECESSARY.

8. BOW AND TWIST SHALL BE LIMITED TO 0.005 INCH PER LINEAR INCH.

9. THIEVING (SOLID) ALLOWED ON ALL INNER LAYERS PER FAB VENDOR'S RECOMMENDATION.
   THIEVING SHAPE - SQUARE
   THIEVING SIZE - 0.030"
   THIEVING PITCH - 0.050"
   THIEVING TO ANY BOARD FEATURES - 0.050"

10. FAB VENDOR TO ADD TEAR DROP FOR ALL INTERNAL SIGNAL LAYERS.

ALL NUMBERS BELOW ARE REFERENCED TO ORIGINAL DESIGN AND ARE TO USED TO SHOW COMPLEXITY OF BOARD ONLY
ALL MEASUREMENTS ARE FROM DRILLED HOLE SIZE.
0.005" OVER NOMINAL FOR PLTD HOLES.

MIN. HOLE PITCH = 0.0157"
MIN. SMD PITCH = 0.0157"
MIN. TRACE WIDTH = 0.005"
MIN. ANNULAR RING = 0.00144"
MIN. HOLE TO COPPER = 0.00715"
MIN.AIR GAP = 0.00374"

ALL UNITS IN INCHES OTHERWISE SPECIFIED

TITLE:
FM160605C

DYNAMIC TEST SOLUTIONS
PCB DESIGN
1-408-264-8880
+65-6873-4610

FAB1	
CUSTOMER:	ON SEMI
DTS PART NO:	D11-101605-B
REV CODE:	B
DESIGNER	XXXXXXXX
DATE:	2017 NOV 29
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REVISIONS					
REV	ECO	DESCRIPTION	ORG	DATE	CHECK
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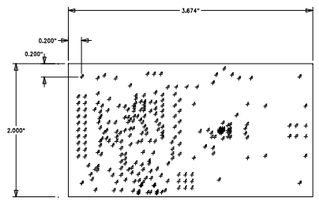
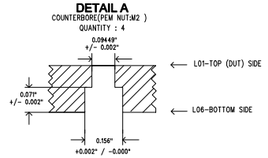


DETAIL A
COUNTERBORE(PEM NUT:M2)
QUANTITY : 4



ALL UNITS IN INCHES OTHERWISE SPECIFIED

DRILL CHART

SIZE	QTY	SYM	PLATED	TOL
0.005	14	A	YES	+0.000 / -0.005
0.0051	1	B	YES	+0.000 / -0.005
0.012	149	C	YES	+0.000 / -0.012
0.01969 x 0.04528	2	D	YES	+/-0.003
0.02165 x 0.03346	2	E	YES	+/-0.003
0.035	9	F	YES	+/-0.003
0.03988	2	G	NO	+/-0.002
0.04	59	H	YES	+/-0.003
0.063	2	I	YES	+/-0.003
0.06693	3	J	YES	+/-0.003
0.07087	4	K	YES	+/-0.003
0.09449	4	L	NO	+/-0.002
0.144	4	M	NO	+/-0.002

NOTES
SEE NOTE 3B & 3D - FILLED VIAS
SEE NOTE 3C & 3D - BLIND VIA : L01 to L02.
DETAIL A - COUNTER BORE

TITLE:
FM160605C

DYNAMIC TEST SOLUTIONS
PCB DESIGN
1-408-264-8880
+65-6873-4610

FAB2	
CUSTOMER:	ON SEMI
DTS PART NO:	D11-101605-B
REV CODE:	B
DESIGNER	XXXXXXXX
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