

MOSFET – Power, Single N-Channel

60 V, 0.91 mΩ, 376 A

NVMTS001N06C

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Plated for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	376	A
		$T_C = 100^\circ\text{C}$		266	
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	P_D	244.0	W
		$T_C = 100^\circ\text{C}$		122.0	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	53.7	A
		$T_A = 100^\circ\text{C}$		38.0	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	5.0	W
		$T_A = 100^\circ\text{C}$		2.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			I_S	203.4	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 30 \text{ A}$)			E_{AS}	887	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.614	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	30.10	

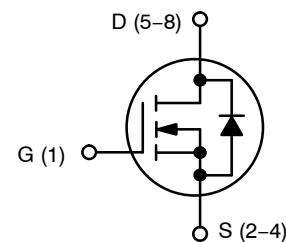
1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



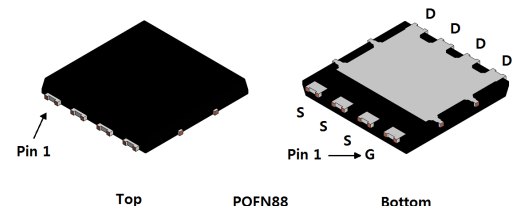
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$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	0.91 mΩ @ 10 V	376 A

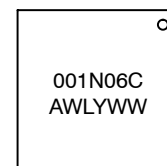


N-CHANNEL MOSFET



DFNW8
CASE 507AP

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMTS001N06C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		22		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		7.75		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.77	0.91	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		160		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.5		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 30\text{ V}$		8705		pF
Output Capacitance	C_{OSS}			6690		
Reverse Transfer Capacitance	C_{RSS}			107		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		113		nC
Threshold Gate Charge	$Q_{G(TH)}$			19.5		
Gate-to-Source Charge	Q_{GS}			31.2		
Gate-to-Drain Charge	Q_{GD}			16.3		
Voltage Plateau	V_{GP}	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$		4.01		V

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		27.4		ns
Rise Time	t_r			21.4		
Turn-Off Delay Time	$t_{d(OFF)}$			58.3		
Fall Time	t_f			14.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.78	1.2	V
			$T_J = 125^\circ\text{C}$		0.63		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$			100		ns
Charge Time	t_a				66.3		
Discharge Time	t_b				43.7		
Reverse Recovery Charge	Q_{RR}				236		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

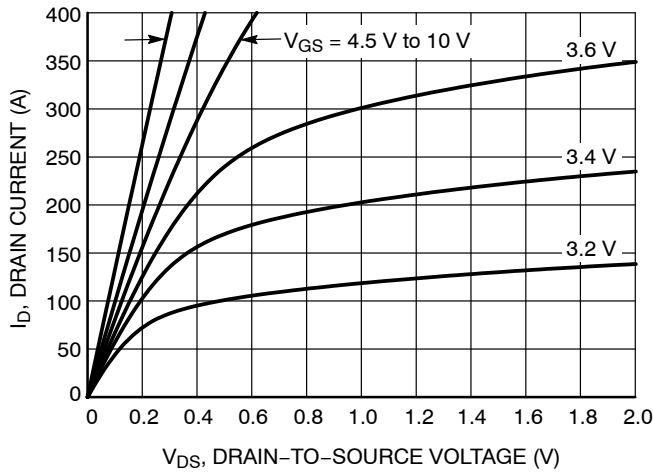


Figure 1. On-Region Characteristics

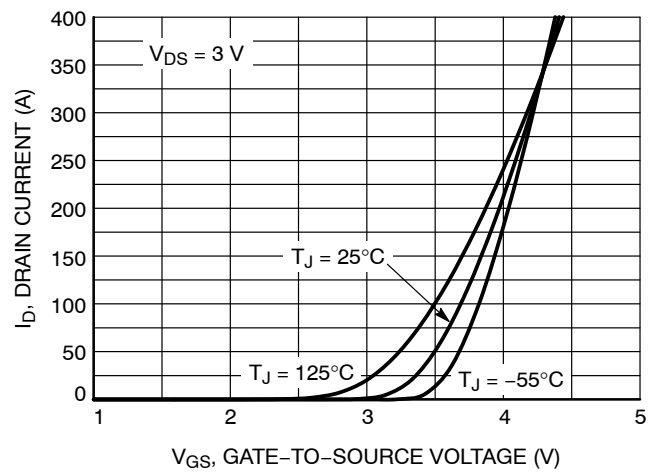


Figure 2. Transfer Characteristics

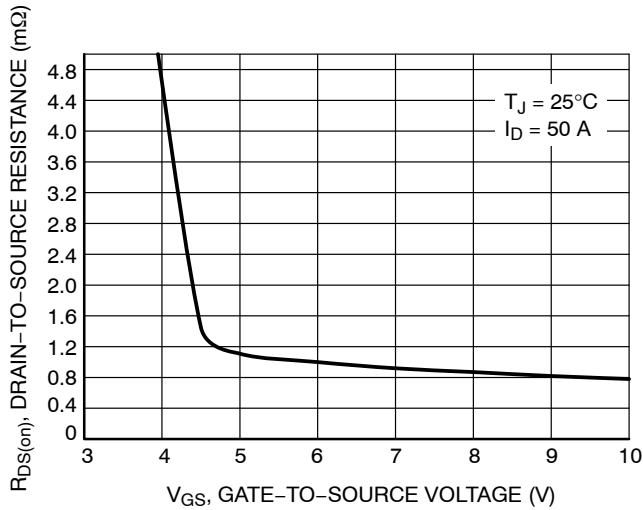


Figure 3. On-Resistance vs. Gate-to-Source Voltage

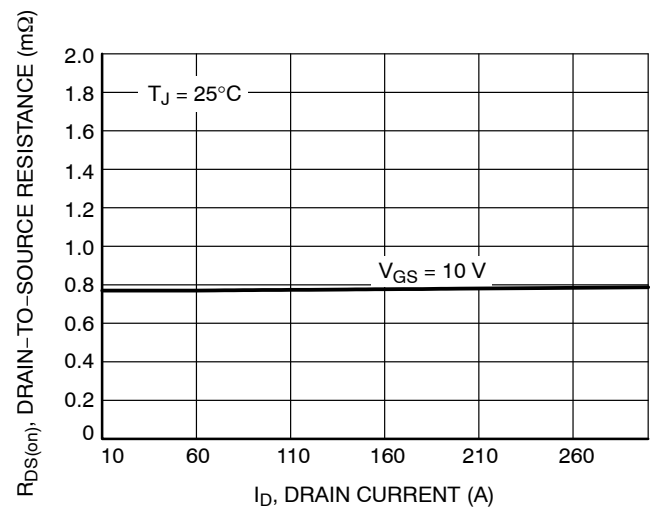


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

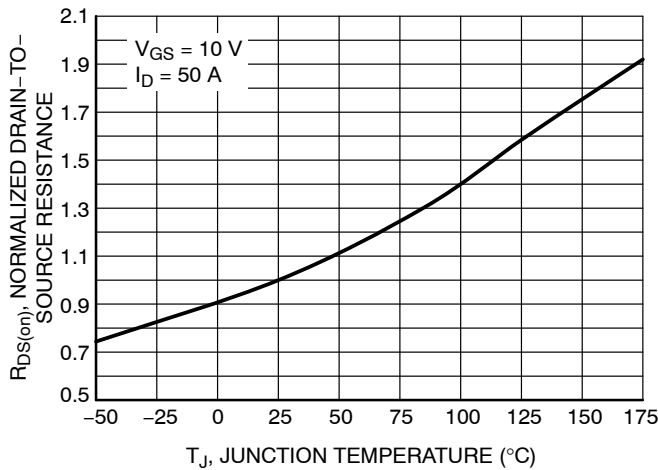


Figure 5. On-Resistance Variation with Temperature

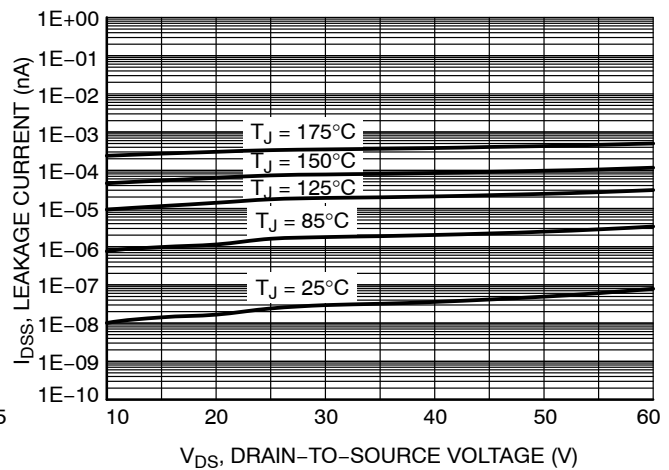


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

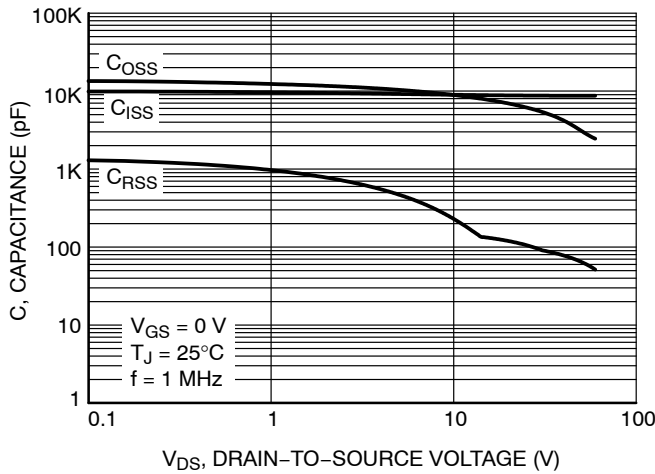


Figure 7. Capacitance Variation

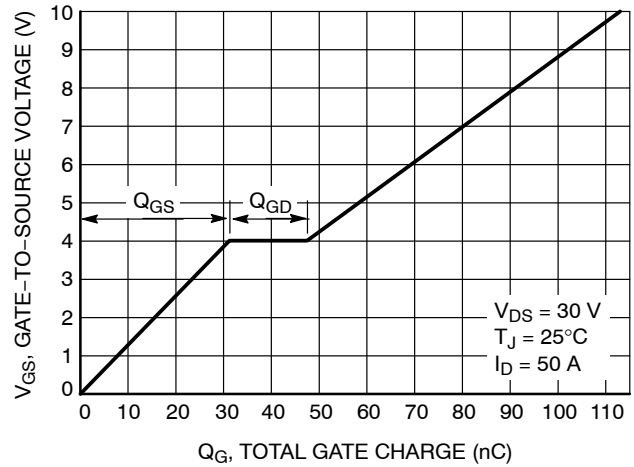


Figure 8. Gate-to-Source Voltage vs. Total Charge

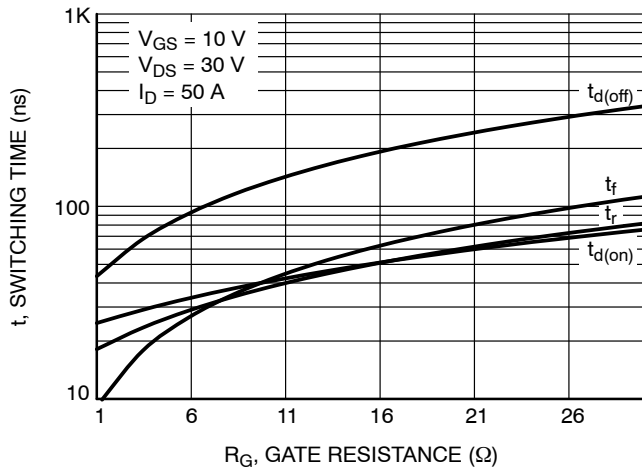


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

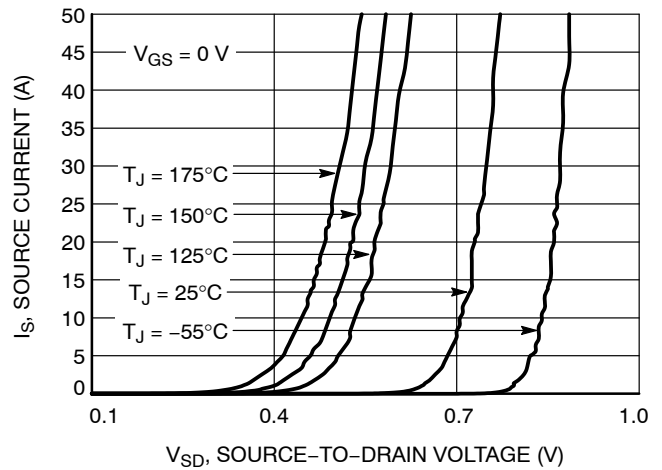


Figure 10. Diode Forward Voltage vs. Current

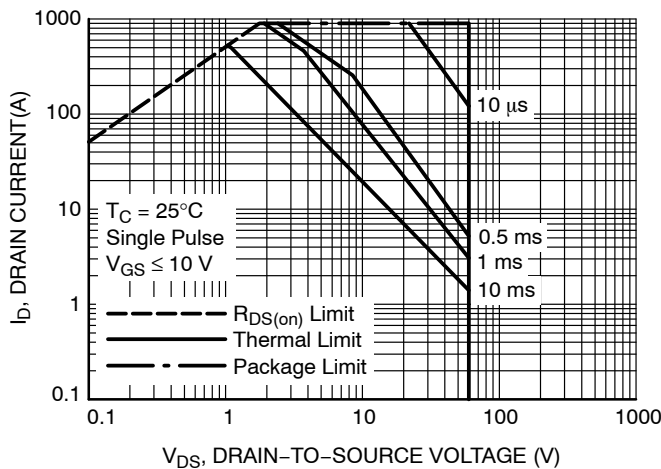


Figure 11. Maximum Rated Forward Biased Safe Operating Area

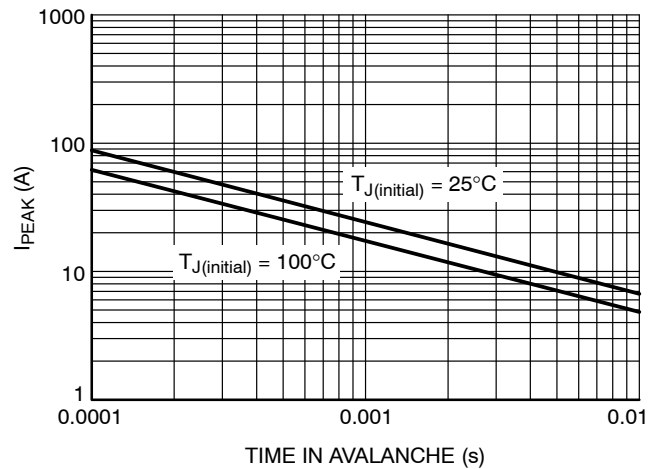


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMTS001N06C

TYPICAL CHARACTERISTICS

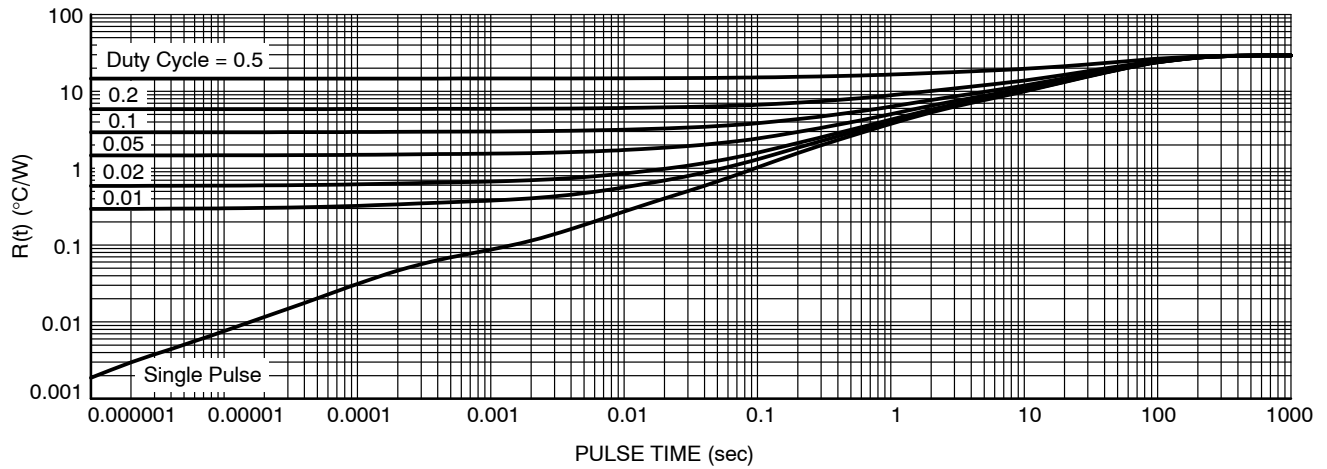


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMTS001N06CTXG	001N06C	DFNW8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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CASE 507AP
ISSUE E

DATE 08 MAY 2024

**GENERIC
MARKING DIAGRAM***



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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