NUP4202W1

ESD Protection Diode, Low Clamping Voltage

The NUP4202W1 surge protection is designed to protect high speed data lines from ESD, EFT, and lightning.

Features
- Low Clamping Voltage
- Stand–Off Voltage: 5 V
- Low Leakage
- Protection for the Following IEC Standards:
  IEC 61000–4–2 Level 4 ESD Protection
- UL Flammability Rating of 94 V–0
- This is a Pb–Free Device

Typical Applications
- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI) and HDMI
- Monitors and Flat Panel Displays
- MP3

MAXIMUM RATINGS (TJ = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Power Dissipation 8 x 20 μs @ TA = 25°C (Note 1)</td>
<td>Ppk</td>
<td>500</td>
<td>W</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>TJ</td>
<td>–40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Solder Temperature – Maximum (10 Seconds)</td>
<td>TL</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Human Body Model (HBM)</td>
<td>ESD</td>
<td>16000</td>
<td>V</td>
</tr>
<tr>
<td>Machine Model (MM)</td>
<td></td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>IEC 61000–4–2 Air (ESD)</td>
<td></td>
<td>20000</td>
<td></td>
</tr>
<tr>
<td>IEC 61000–4–2 Contact (ESD)</td>
<td></td>
<td>20000</td>
<td></td>
</tr>
<tr>
<td>IEC 61000–4–4 (5/50 ns)</td>
<td>EFT</td>
<td>40</td>
<td>A</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Nonrepetitive current pulse per Figure 5 (Pin 5 to Pin 2).

See Application Note AND8308/D for further description of survivability specs.
ELECTRICAL CHARACTERISTICS
(T<sub>A</sub> = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPP</td>
<td>Maximum Reverse Peak Pulse Current</td>
</tr>
<tr>
<td>V&lt;sub&gt;C&lt;/sub&gt;</td>
<td>Clamping Voltage @ IPP</td>
</tr>
<tr>
<td>V&lt;sub&gt;RWM&lt;/sub&gt;</td>
<td>Working Peak Reverse Voltage</td>
</tr>
<tr>
<td>I&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Maximum Reverse Leakage Current @ V&lt;sub&gt;RWM&lt;/sub&gt;</td>
</tr>
<tr>
<td>V&lt;sub&gt;BR&lt;/sub&gt;</td>
<td>Breakdown Voltage @ I&lt;sub&gt;T&lt;/sub&gt;</td>
</tr>
<tr>
<td>I&lt;sub&gt;T&lt;/sub&gt;</td>
<td>Test Current</td>
</tr>
<tr>
<td>I&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Forward Current</td>
</tr>
<tr>
<td>V&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Forward Voltage @ I&lt;sub&gt;F&lt;/sub&gt;</td>
</tr>
<tr>
<td>P&lt;sub&gt;pk&lt;/sub&gt;</td>
<td>Peak Power Dissipation</td>
</tr>
<tr>
<td>C</td>
<td>Capacitance @ V&lt;sub&gt;R&lt;/sub&gt; = 0 and f = 1.0 MHz</td>
</tr>
</tbody>
</table>

*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse Working Voltage</td>
<td>V&lt;sub&gt;RWM&lt;/sub&gt;</td>
<td>(Note 2)</td>
<td></td>
<td></td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>V&lt;sub&gt;BR&lt;/sub&gt;</td>
<td>I&lt;sub&gt;T&lt;/sub&gt; = 1 mA, (Note 3)</td>
<td>6.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reverse Leakage Current</td>
<td>I&lt;sub&gt;R&lt;/sub&gt;</td>
<td>V&lt;sub&gt;RWM&lt;/sub&gt; = 5 V</td>
<td></td>
<td>8.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>Clamping Voltage</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;</td>
<td>IPP = 5 A (Note 4)</td>
<td></td>
<td></td>
<td>8.9</td>
<td>20</td>
</tr>
<tr>
<td>Maximum Peak Pulse Current</td>
<td>IPP</td>
<td>8x20 μs Waveform (Note 4)</td>
<td></td>
<td>28</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Junction Capacitance</td>
<td>C&lt;sub&gt;J&lt;/sub&gt;</td>
<td>VR = 0 V, f = 1 MHz between I/O Pins and GND</td>
<td>3.0</td>
<td>5.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Junction Capacitance</td>
<td>C&lt;sub&gt;J&lt;/sub&gt;</td>
<td>VR = 0 V, f = 1 MHz between I/O Pins</td>
<td></td>
<td>1.5</td>
<td>3.0</td>
<td>pF</td>
</tr>
<tr>
<td>Clamping Voltage</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;</td>
<td>@ IPP = 1 A (Notes 5 and 6)</td>
<td>14.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Clamping Voltage</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;</td>
<td>Per IEC 61000–4–2 (Note 7)</td>
<td>Figure 1 and 2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

2. Surge protection devices are normally selected according to the working peak reverse voltage (V<sub>RWM</sub>), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V<sub>BR</sub> is measured at pulse test current I<sub>T</sub>.
4. Nonrepetitive current pulse per Figure 5 (Pin 5 to Pin 2).
5. Nonrepetitive current pulse per Figure 5 (Any I/O Pins).
6. Surge current waveform per Figure 5.
7. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000–4–2

Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000–4–2
IEC 61000–4–2 Spec.

<table>
<thead>
<tr>
<th>Level</th>
<th>Test Voltage (kV)</th>
<th>First Peak Current (A)</th>
<th>Current at 30 ns (A)</th>
<th>Current at 60 ns (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>7.5</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>15</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>22.5</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>30</td>
<td>16</td>
<td>8</td>
</tr>
</tbody>
</table>

Figure 3. IEC61000–4–2 Spec

ESD Gun

Oscilloscope

50 Ω
Cable

Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation ofDatasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000–4–2 waveform. Since the IEC61000–4–2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

Figure 5. 8 X 20 μs Pulse Waveform

www.onsemi.com
TYPICAL PERFORMANCE CURVES

\( T_J = 25^\circ \text{C} \) unless otherwise noted

**Figure 6. Pulse Derating Curve**

**Figure 7. Junction Capacitance vs Reverse Voltage**

**Figure 8. Clamping Voltage vs. Peak Pulse Current (8 x 20 \( \mu \text{s} \) Waveform)**
The new NUP4202W1 is a low capacitance surge protection diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4202W1 offers surge rated, low capacitance steering diodes and a surge protection diode integrated in a single package (SC-88). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The surge protection device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

NUP4202W1 Configuration Options

The NUP4202W1 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or V_CC + V_f). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB’s ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1
Protection of four data lines and the power supply using V_CC as reference.

For this configuration, connect pin 5 directly to the positive supply rail (V_CC), the data lines are referenced to the supply voltage. The internal surge protection diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2
Protection of four data lines with bias and power supply isolation resistor.

The NUP4202W1 can be isolated from the power supply by connecting a series resistor between pin 5 and V_CC. A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal surge protection and steering diodes, reducing their capacitance.

Option 3
Protection of four data lines using the internal surge protection diode as reference.

In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal surge protection can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the surge protection plus one diode drop (V_c = V_f + V_RWM).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:
Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

For positive pulse conditions:
\[ V_C = V_{CC} + V_f \]

For negative pulse conditions:
\[ V_C = -V_f \]

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.

An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:
\[ V_C = V_{CC} + V_f + (L \frac{dI_{ESD}}{dt}) \]

For negative pulse conditions:
\[ V_C = -V_f - (L \frac{dI_{ESD}}{dt}) \]

As shown in the formulas, the clamping voltage (Vc) not only depends on the Vf of the steering diodes but also on the L \( \frac{dI_{ESD}}{dt} \) factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic inductance will provide significant benefits in transient immunity.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4202W1 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.
TYPICAL APPLICATIONS

Figure 10. ESD Protection for USB Port

Figure 11. Protection for Ethernet 10/100 (Differential Mode)
Figure 12. TI/E1 Interface Protection
PACKAGE DIMENSIONS

SC–88/SC70–6/SOT–363

CASE 419B–02

ISSUE W

NOTES:


2. CONTROLLING DIMENSION: INCH.

3. 419B–01 OBSOLETE, NEW STANDARD 419B–02.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.80</td>
<td>0.95</td>
<td>1.10</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.05</td>
<td>0.10</td>
</tr>
<tr>
<td>A3</td>
<td>0.20 REF*</td>
<td>0.08 REF*</td>
<td></td>
</tr>
<tr>
<td>p</td>
<td>0.10</td>
<td>0.21</td>
<td>0.30</td>
</tr>
<tr>
<td>C</td>
<td>0.10</td>
<td>0.14</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td>1.80</td>
<td>2.00</td>
<td>2.20</td>
</tr>
<tr>
<td>E</td>
<td>1.15</td>
<td>1.25</td>
<td>1.36</td>
</tr>
<tr>
<td>L</td>
<td>0.10</td>
<td>0.20</td>
<td>0.30</td>
</tr>
<tr>
<td>HE</td>
<td>2.00</td>
<td>2.10</td>
<td>2.20</td>
</tr>
</tbody>
</table>

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer’s technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor.”

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

USA/Canada
Phone: 421 33 790 2910
EUROPE, MIDDLE EAST AND AFRICA TECHNICAL SUPPORT:
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: www.onsemi.com
Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative