

# MOSFET - Power, Single N-Channel

**80 V, 1.1 mΩ, 335 A**

## NTMTS1D2N08H

### Features

- Small Footprint (8x8 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	80	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Notes 1, 3)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	335	A
		T <sub>C</sub> = 100°C		237	
Power Dissipation R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 25°C	P <sub>D</sub>	300	W
		T <sub>C</sub> = 100°C		150	
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	41	A
		T <sub>A</sub> = 100°C		29	
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	5	W
		T <sub>A</sub> = 100°C		2.5	
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	900	A
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)			I <sub>S</sub>	335	A
Single Pulse Drain-to-Source Avalanche Energy (L = 3 mH, I <sub>L(pk)</sub> = 34 A)			E <sub>AS</sub>	1734	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

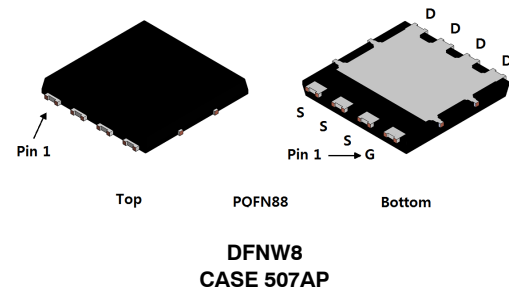
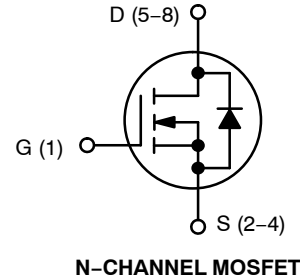
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

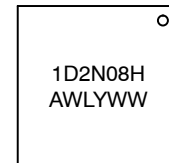
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	30	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	1.1 mΩ @ 10 V	335 A



### MARKING DIAGRAM



A = Assembly Location  
 WL = 2-digit Wafer Lot Code  
 Y = Year Code  
 WW = Work Week Code

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NTMTS1D2N08H

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			57		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 590\text{ }\mu\text{A}$	2.0	2.9	4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-7.6		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 90\text{ A}$		0.93	1.1	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 59\text{ A}$		1.28	1.6	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 90\text{ A}$		400		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 500\text{ kHz}, V_{DS} = 40\text{ V}$		10100		pF
Output Capacitance	$C_{OSS}$			1455		
Reverse Transfer Capacitance	$C_{RSS}$			43		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 64\text{ V}; I_D = 90\text{ A}$		147		nC
Threshold Gate Charge	$Q_{G(TH)}$			27		
Gate-to-Source Charge	$Q_{GS}$			41		
Gate-to-Drain Charge	$Q_{GD}$			32		
Plateau Voltage	$V_{GP}$			4		V

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 64\text{ V}, I_D = 90\text{ A}, R_G = 2.5\text{ }\Omega$		29		ns
Rise Time	$t_r$			14		
Turn-Off Delay Time	$t_{d(OFF)}$			66		
Fall Time	$t_f$			19		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 90\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 90\text{ A}$			84		ns
Reverse Recovery Charge	$Q_{RR}$				189		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

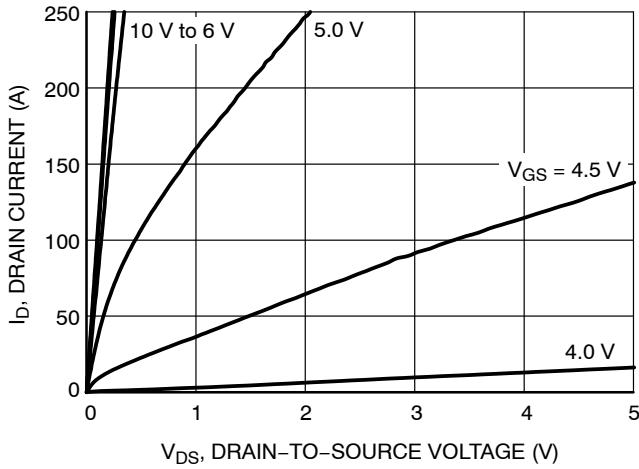


Figure 1. On-Region Characteristics

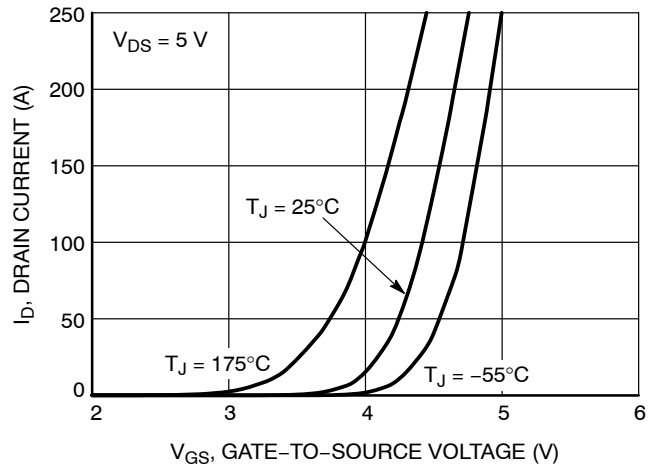


Figure 2. Transfer Characteristics

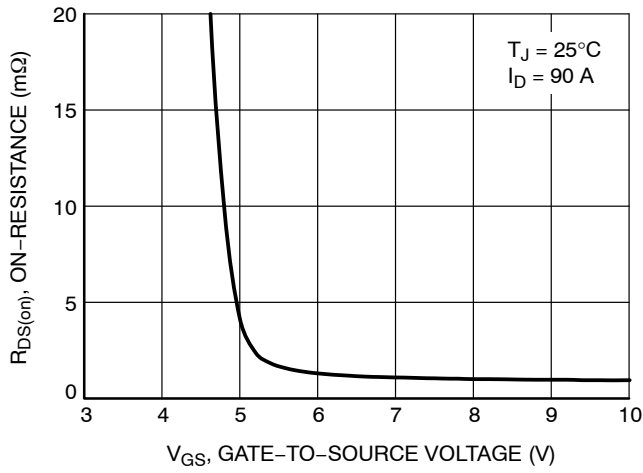


Figure 3. On-Resistance vs. Gate-to-Source Voltage

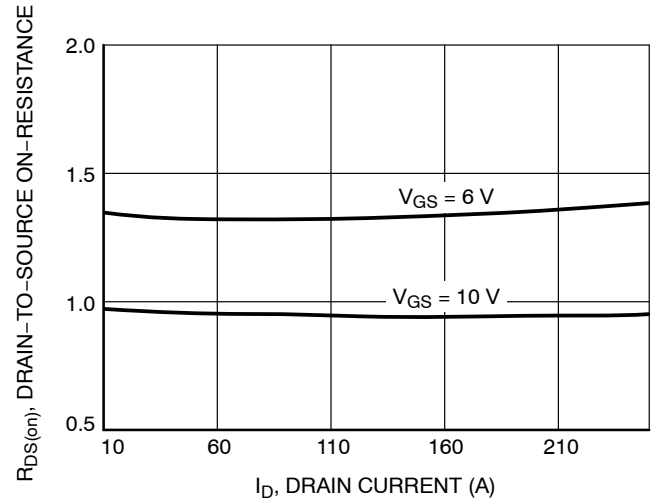


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

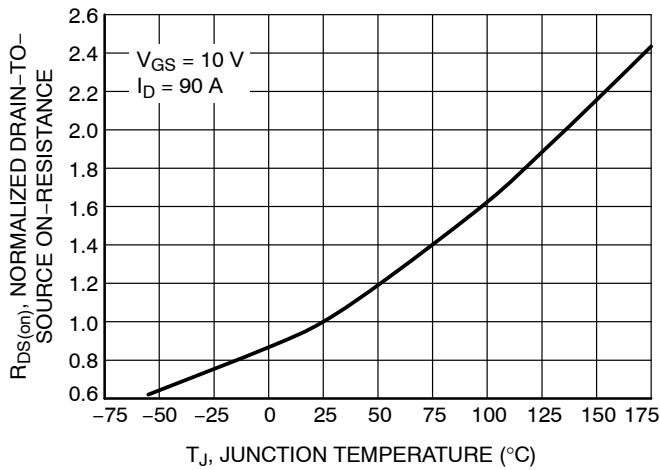


Figure 5. On-Resistance Variation with Temperature

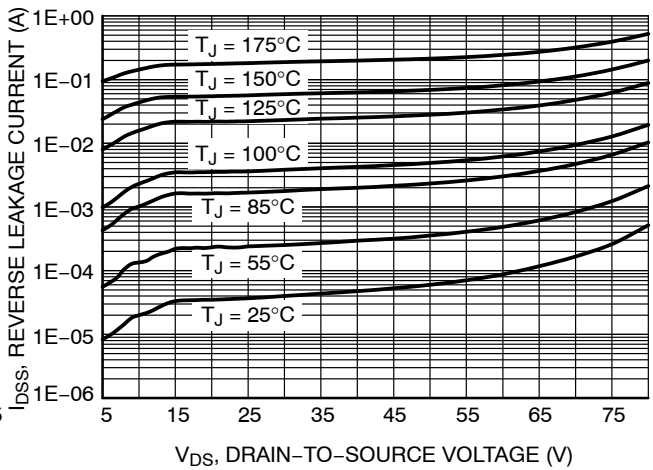


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

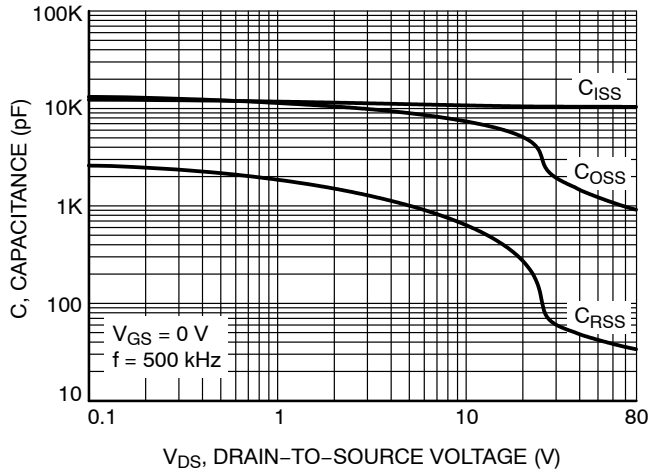


Figure 7. Capacitance Variation

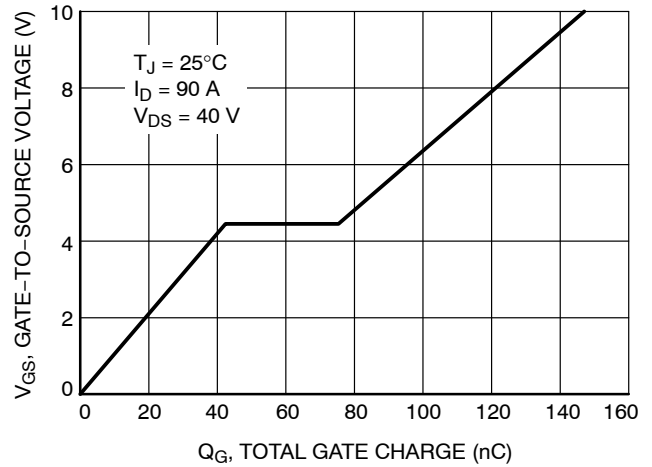


Figure 8. Gate-to-Source Voltage vs. Total Charge

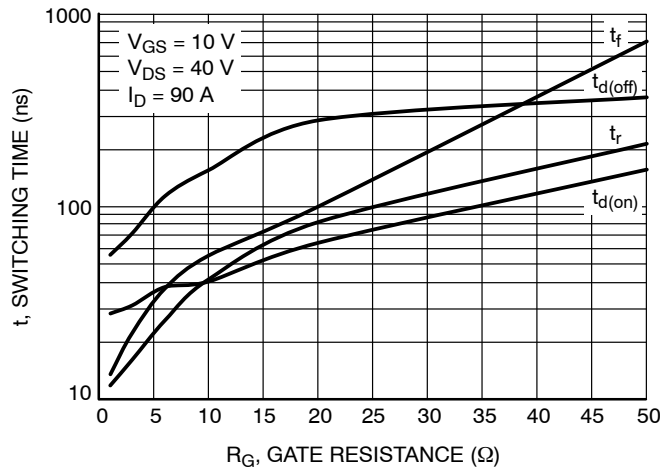


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

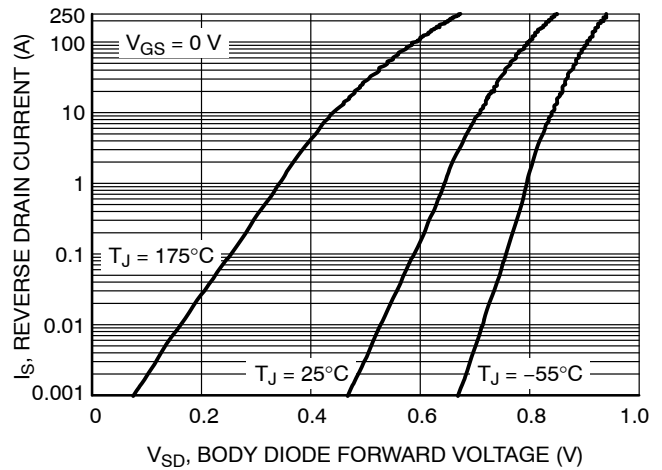


Figure 10. Diode Forward Voltage vs. Current

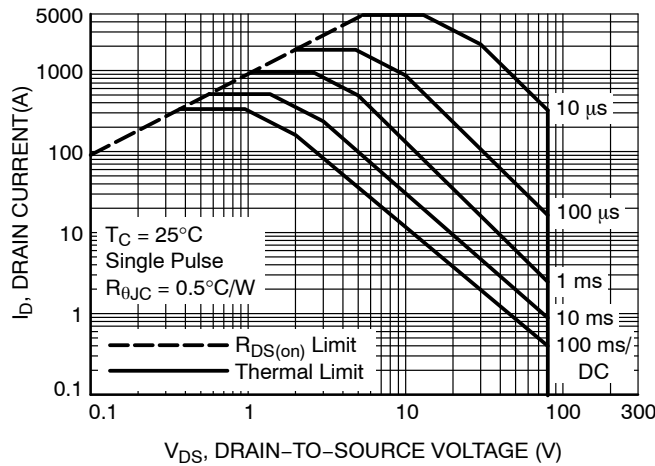


Figure 11. Maximum Rated Forward Biased Safe Operating Area

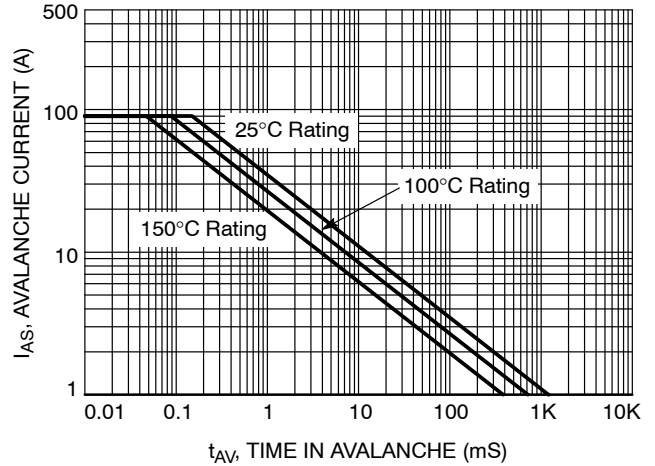


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

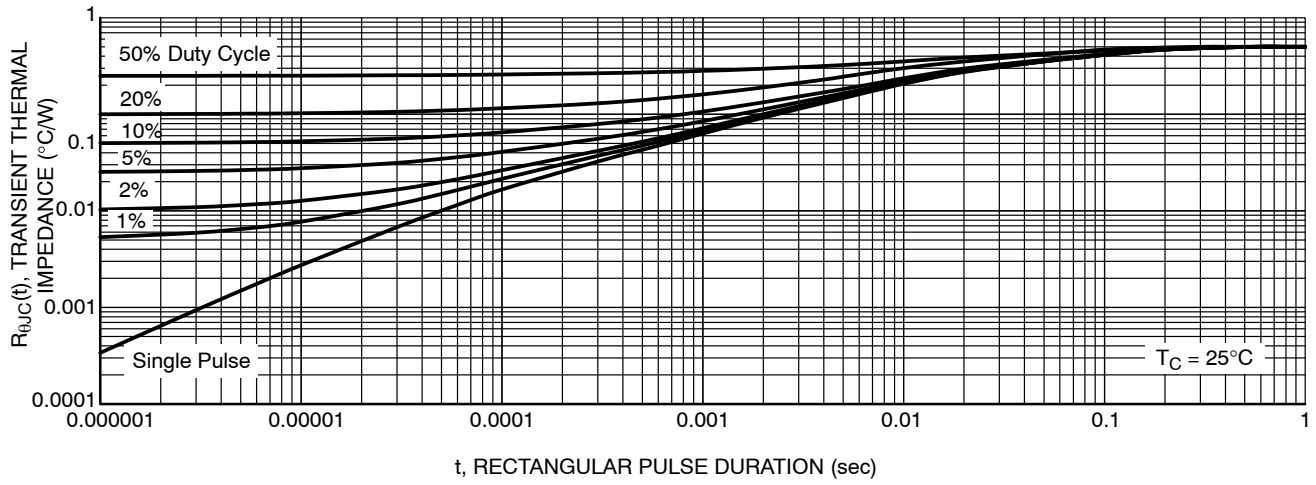


Figure 13. Thermal Response

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NTMTS1D2N08H	NTMTS1D2N08H	DFNW8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


**TDFNW8 8.30x8.40x1.10, 2.00P**  
**CASE 507AP**  
**ISSUE E**

DATE 08 MAY 2024



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot Code  
Y = Year Code  
WW = Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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