MOSFET – Power, N-Channel, SUPERFET® III, FRFET®

650 V, 70 A, 33 mΩ

NTHL033N65S3HF

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	33 mΩ @ 10 V	70 A

Description

SUPERFET III MOSFET is **onsemi**’s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

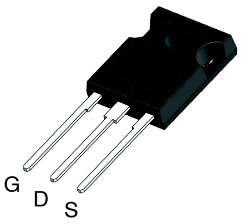
SUPERFET III FRFET MOSFET’s optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

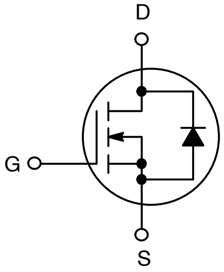
- 700 V @ $T_J = 150°C$
- Typ. $R_{DS(on)} = 28\ m\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 188\ nC$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 1568\ pF$)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

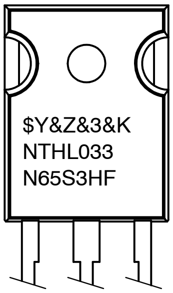
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



TO−247 long leads
CASE 340CX



MARKING DIAGRAM



$Y = **onsemi** Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot
NTHL033N65S3HF = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

January, 2025 − Rev. 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25°C)	70	A
		– Continuous (T_C = 100°C)	53	
I_{DM}	Drain Current	– Pulsed (Note 1)	175	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1250	mJ
I_{AS}	Avalanche Current (Note 2)		12	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		5.0	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	500	W
		– Derate Above 25°C	4.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse–width limited by maximum junction temperature.
2. I_{AS} = 12 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq 35$ A, di/dt ≤ 200 A/μs, $V_{DD} \leq 400$ V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 15 mA, Referenced to 25°C		0.63		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		263		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.5 mA	3.0		5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 35 A		28	33	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 35 A		49		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		6720		pF
C_{oss}	Output Capacitance			159		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		1568		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		292		pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 35 A, V_{GS} = 10 V (Note 4)		188		nC
Q_{gs}	Gate to Source Gate Charge			55		nC
Q_{gd}	Gate to Drain “Miller” Charge			73		nC
ESR	Equivalent Series Resistance	f = 1 MHz		1.1		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 35 A, V_{GS} = 10 V, R_g = 2.2 Ω (Note 4)		43		ns
t_r	Turn-On Rise Time			35		ns
$t_{d(off)}$	Turn-Off Delay Time			110		ns
t_f	Turn-Off Fall Time			28		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				70	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				175	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 35 A			1.3	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 35 A, dI_F/dt = 100 A/μs		173		ns
Q_{rr}	Reverse Recovery Charge			1003		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

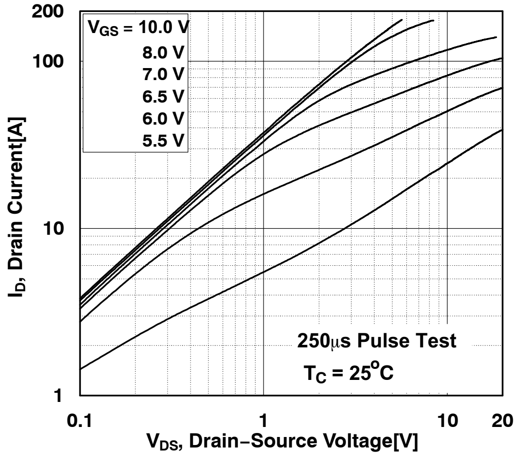


Figure 1. On−Region Characteristics

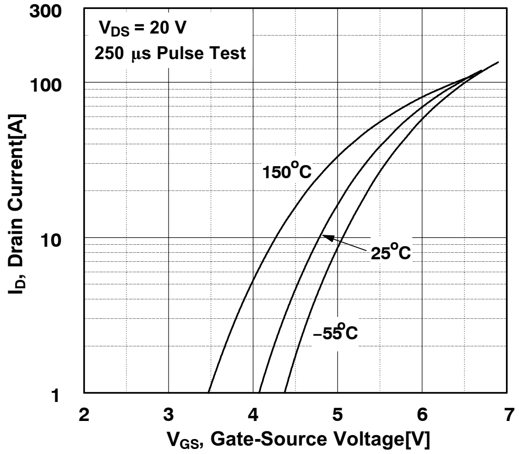


Figure 2. Transfer Characteristics

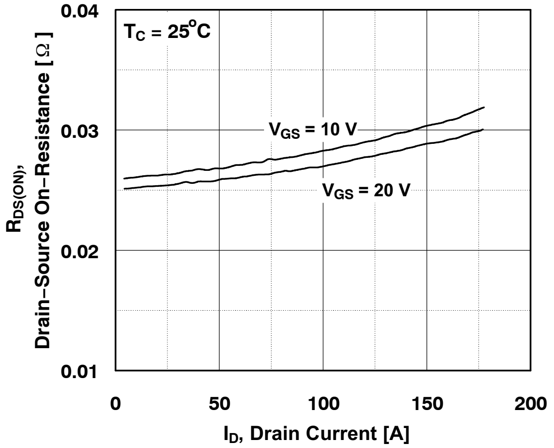


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

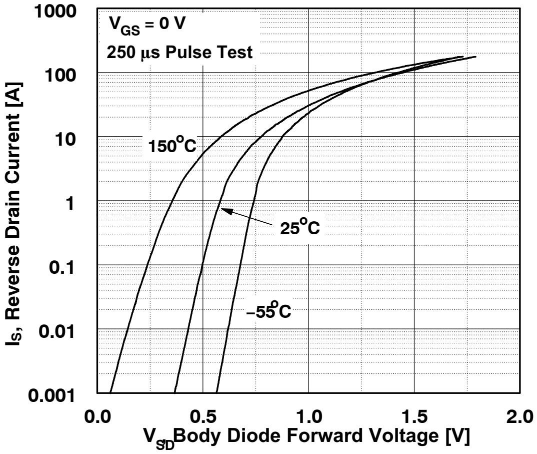


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

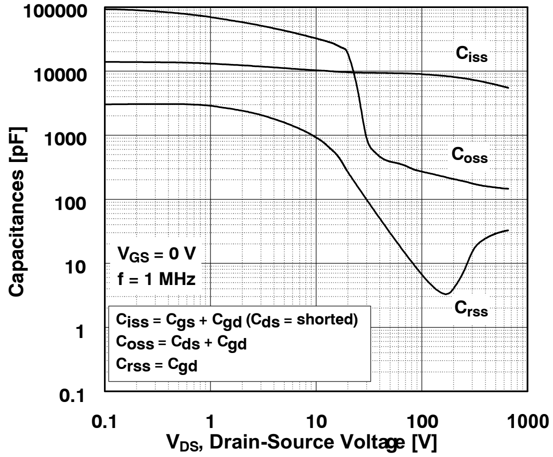


Figure 5. Capacitance Characteristics

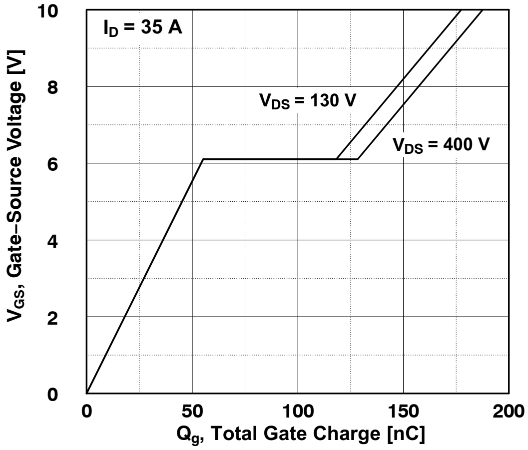


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

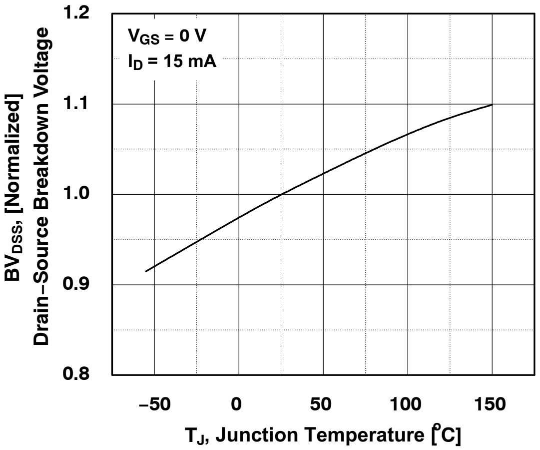


Figure 7. Breakdown Voltage Variation vs. Temperature

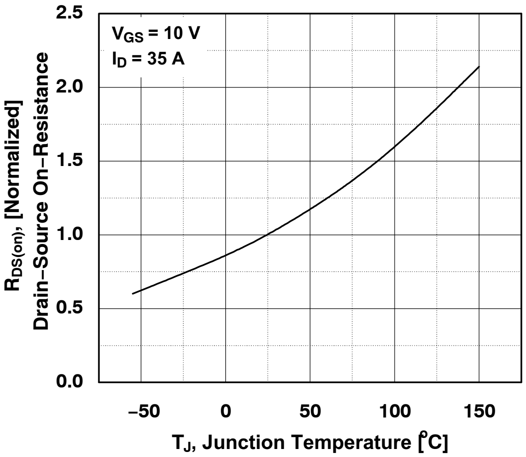


Figure 8. On−Resistance Variation vs. Temperature

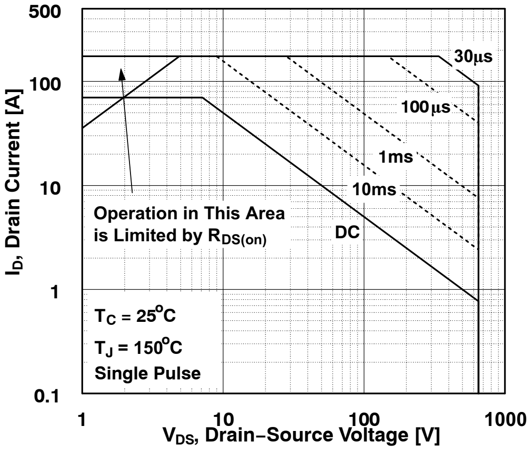


Figure 9. Maximum Safe Operating Area

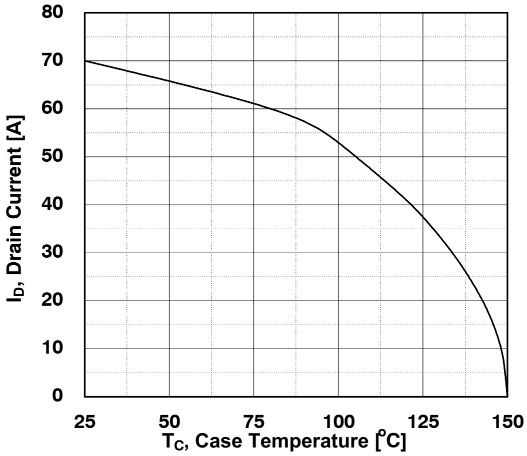


Figure 10. Maximum Drain Current vs. Case Temperature

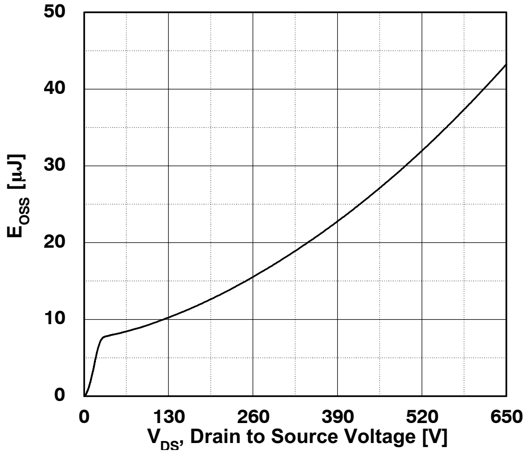


Figure 11. Eoss vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS (continued)

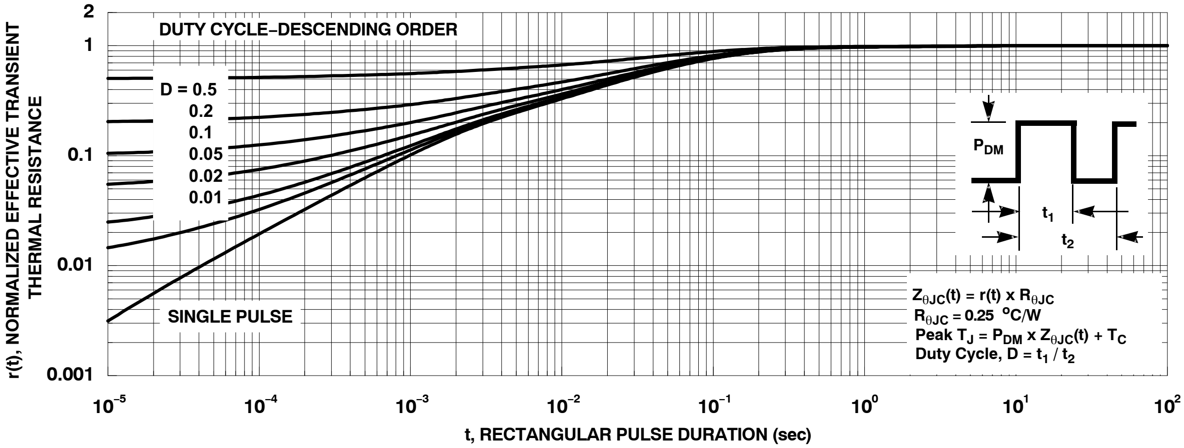


Figure 12. Transient Thermal Response Curve

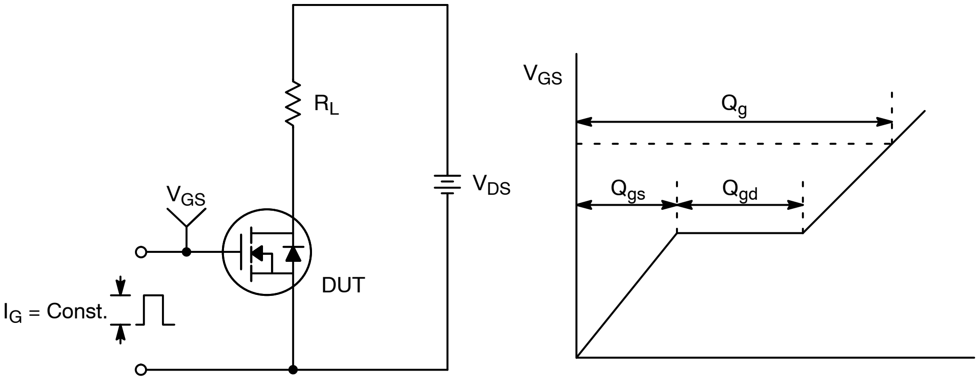


Figure 13. Gate Charge Test Circuit & Waveform

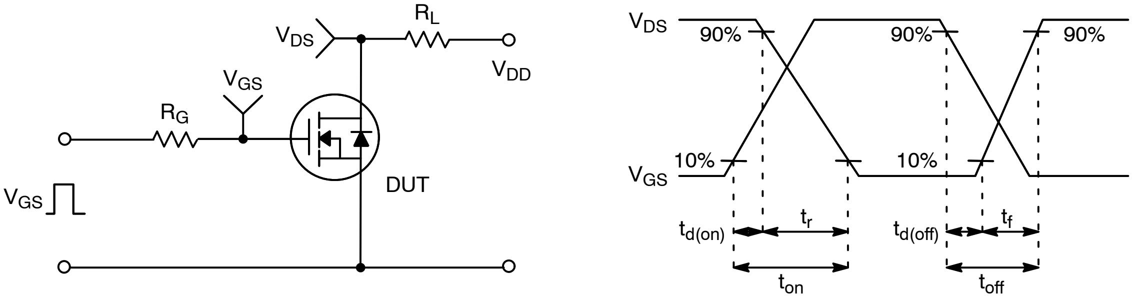


Figure 14. Resistive Switching Test Circuit & Waveforms

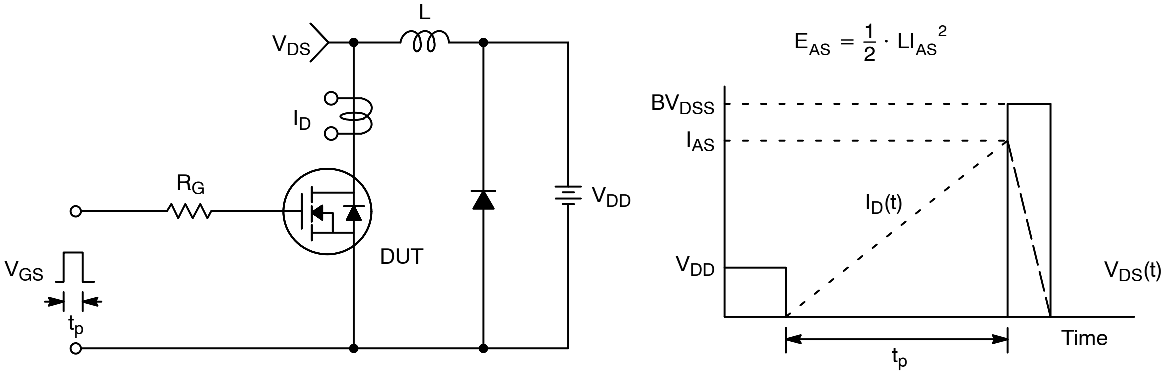


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

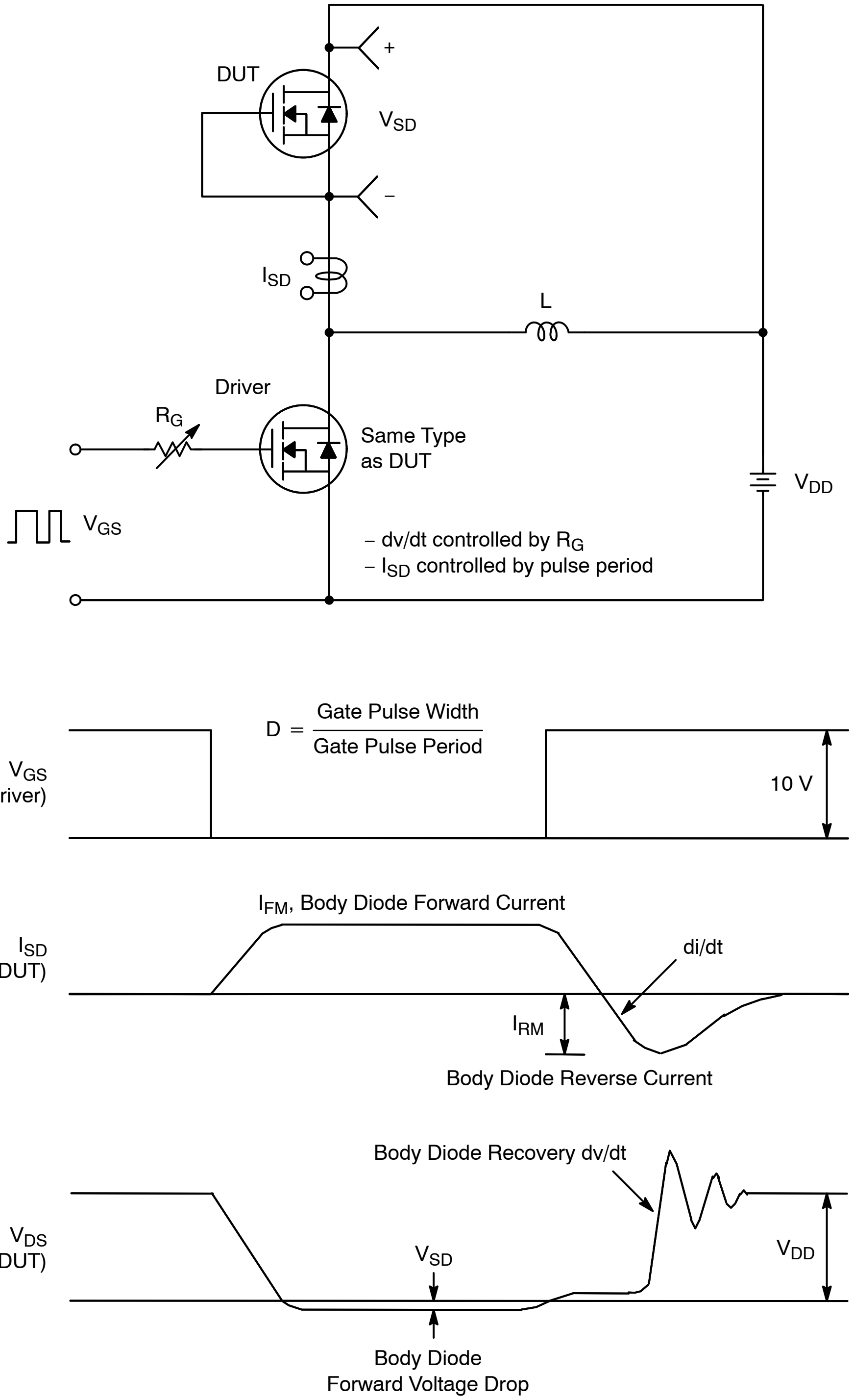


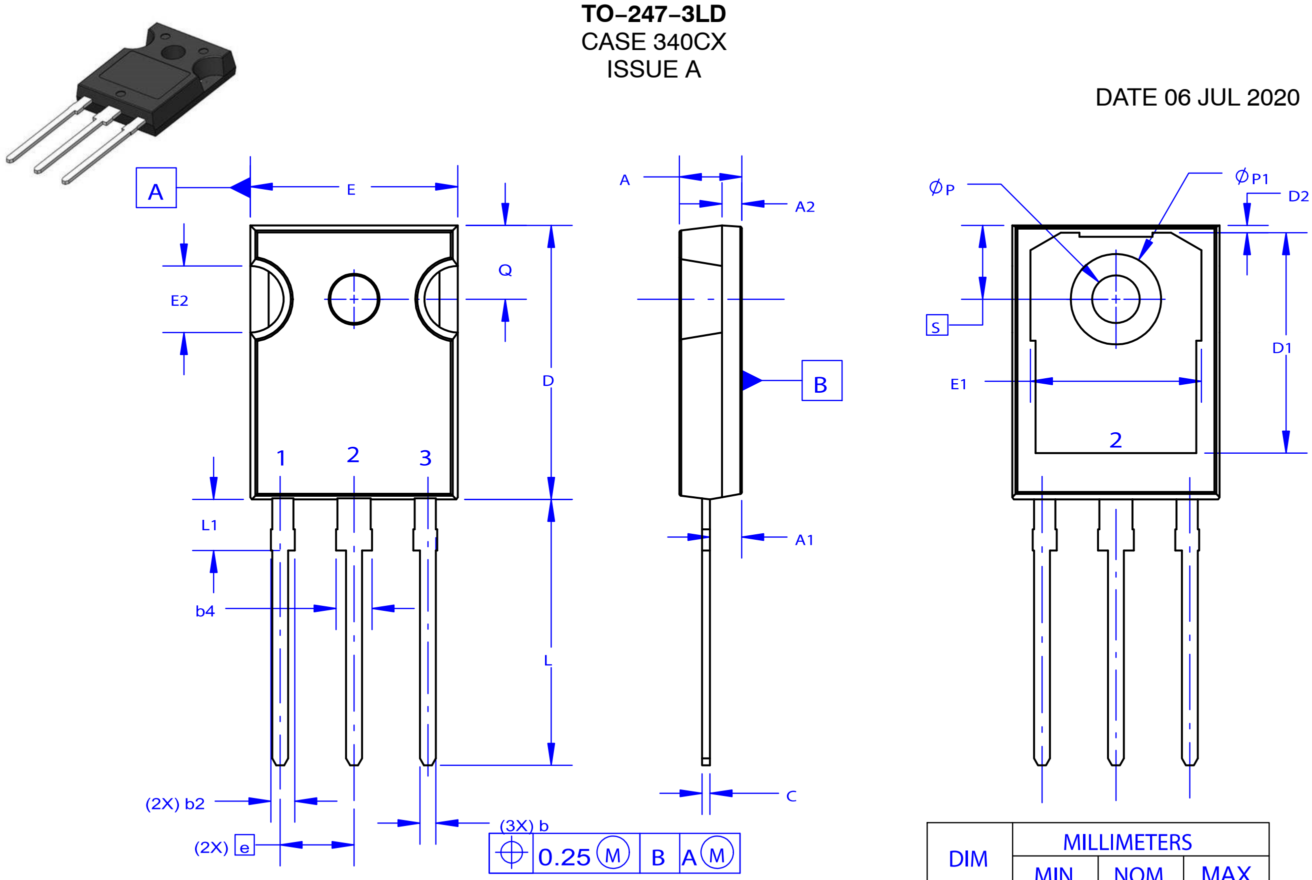
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTHL033N65S3HF	NTHL033N65S3HF	TO−247	Tube	N/A	N/A	30 Units

TO−247−3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−247−3LD**	**PAGE 1 OF 1**

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