# NTGS3441P

# Power MOSFET

## −20 V, −3.16 A, Single P−Channel TSOP−6

### Features

- Ultra Low $R_{DS(on)}$ to Improve Conduction Loss
- Low Gate Charge to Improve Switching Losses
- TSOP−6 Surface Mount Package
- This is a Pb−Free Device

### Applications

- High Side Switch in DC−DC Converters
- Battery Management

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −20 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −2.5 | A |
| | | $T_A$ = 85°C | | −1.8 | |
| | t = 10 s | $T_A$ = 25°C | | −3.16 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 0.98 | W |
| | t = 10 s | | | 1.60 | |
| Continuous Drain Current (Note 2) | Steady State | $T_A$ = 25°C | $I_D$ | −1.8 | A |
| | | $T_A$ = 85°C | | −1.3 | |
| Power Dissipation (Note 2) | | $T_A$ = 25°C | $P_D$ | 0.51 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | −13 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −1.5 | A |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0751 in sq)

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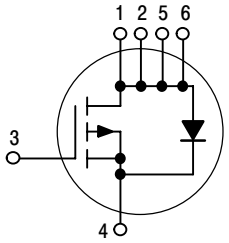
**http://onsemi.com**

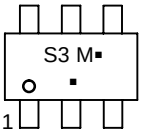
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|---|---|---|
| −20 V | 91 mΩ @ 4.5 V | −3.16 A |
| | 144 mΩ @ 2.7 V | |
| | 188 mΩ @ 2.5 V | |

**P−Channel**



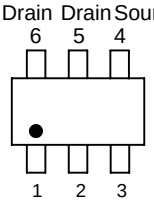

**MARKING DIAGRAM**


**TSOP−6**
**CASE 318G**
**STYLE 1**




PT = Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTGS3441PT1G | TSOP−6 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 128 | °C/W |
| Junction−to−Ambient – t = 10 s (Note 3) | $R_{\theta JA}$ | 78 | |
| Junction−to−Ambient – Steady State (Note 4) | $R_{\theta JA}$ | 244 | |

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
4. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq)

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −20 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 16 | | mV/ °C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −20 V | $T_J$ = 25°C | | | −1 | μA |
| | | | $T_J$ = 125°C | | | −10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | 0.6 | | 1.6 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 3.2 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = −3.0 A | | | 91 | 110 | mΩ |
| | | $V_{GS}$ = 2.7 V, $I_D$ = −1.5 A | | | 144 | 165 | |
| | | $V_{GS}$ = 2.5 V, $I_D$ = −1.5 A | | | 188 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −15 V, $I_D$ =−1.5 A | | | 4.0 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = −15 V | | | 345 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 150 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 40 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = −10 V; $I_D$ = −3.0 A | | | 3.25 | 6.0 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 0.3 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 0.6 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 1.4 | | |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 4.5 V, $V_{DD}$ = −10 V, $I_D$ = −1.5 A, $R_G$ = 4.7 Ω | | | 7.0 | 12 | ns |
| Rise Time | $T_r$ | | | | 14 | 25 | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 13 | 25 | |
| Fall Time | $T_f$ | | | | 4.0 | 8.0 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −3.0 A | $T_J$ = 25°C | | 0.8 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.7 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $d_{IS}/d_t$ = 100 A/μs, $I_S$ = −3.0 A | | | 25 | | ns |
| Charge Time | $T_a$ | | | | 10 | | |
| Discharge Time | $T_b$ | | | | 15 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 15 | | nC |

5. Switching characteristics are independent of operating junction temperatures
6. Pulse Test: pulse width = 300 μs, duty cycle = 2%

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

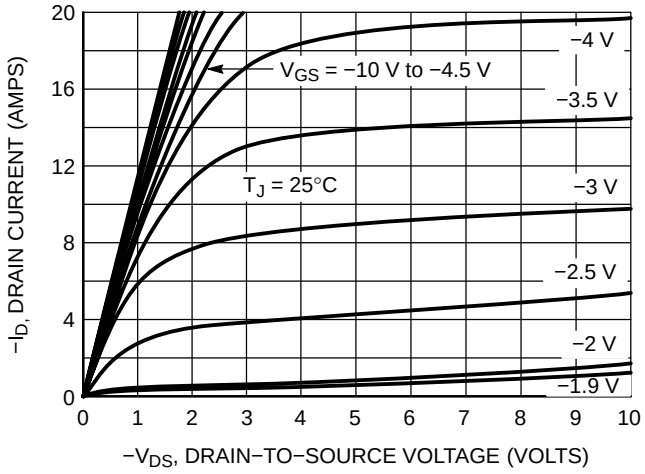



**Figure 1. On−Region Characteristics**

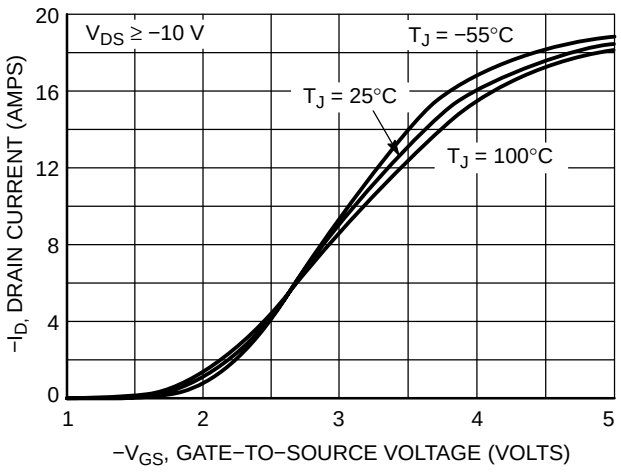



**Figure 2. Transfer Characteristics**

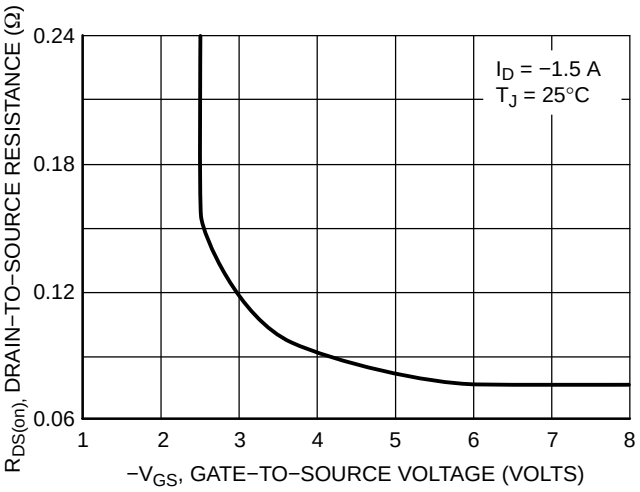



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

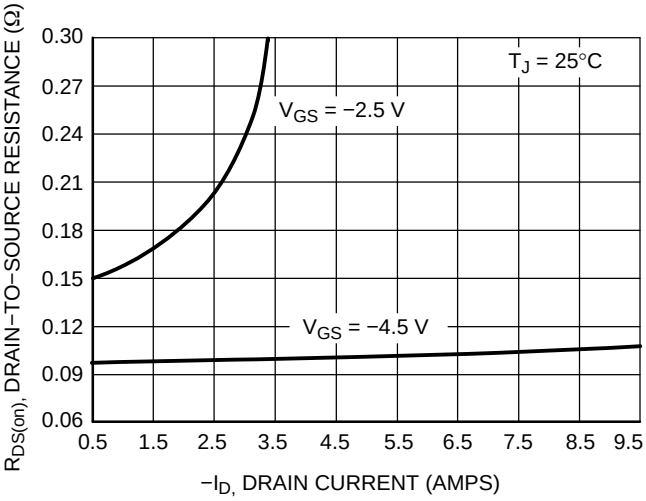



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

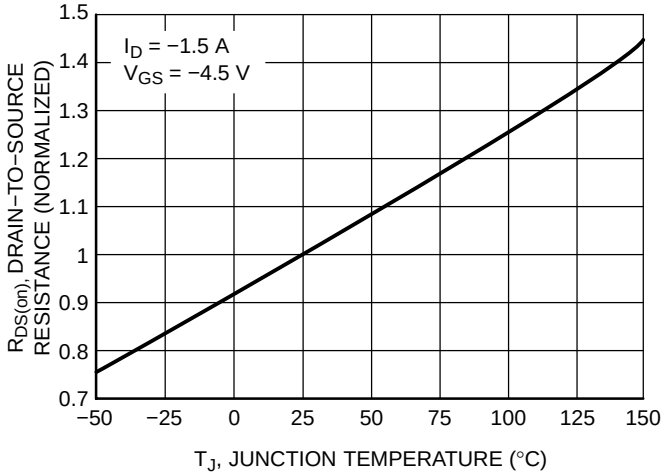



**Figure 5. On−Resistance Variation with Temperature**

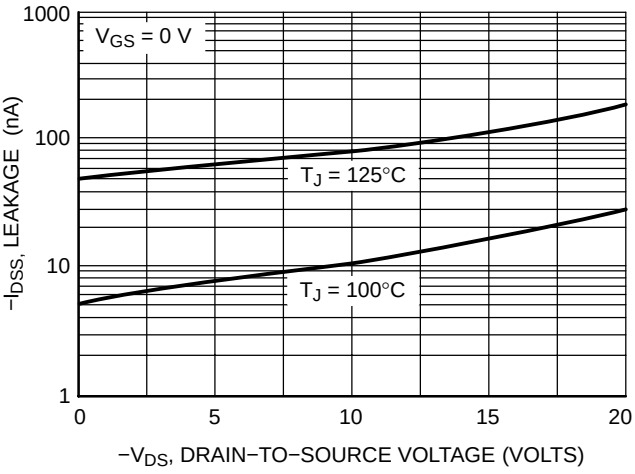



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

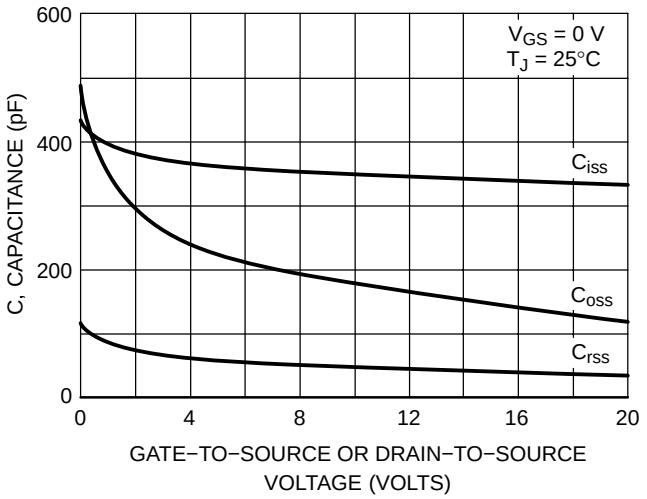



**Figure 7. Capacitance Variation**

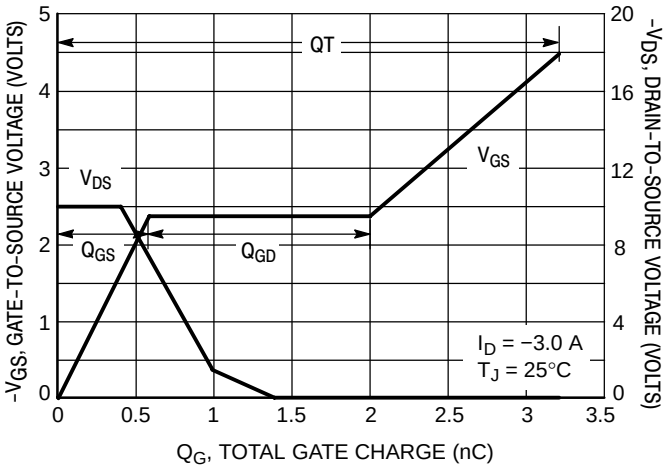



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

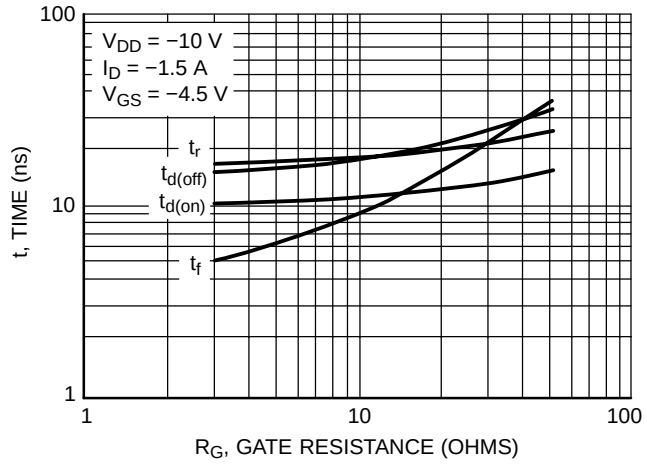



**Figure 9. Gate Threshold Voltage Variation with Temperature**

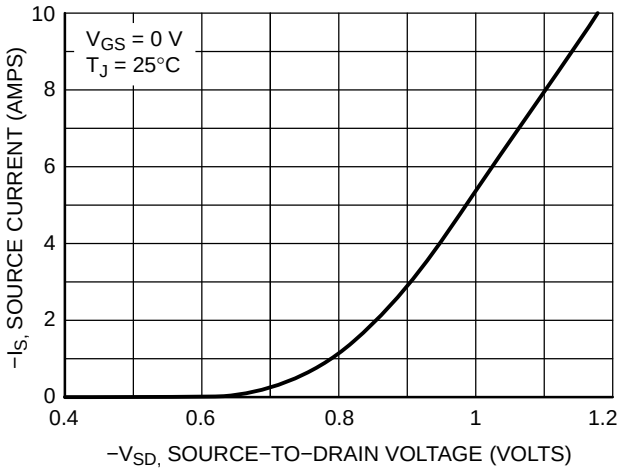
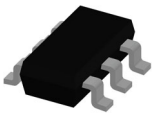


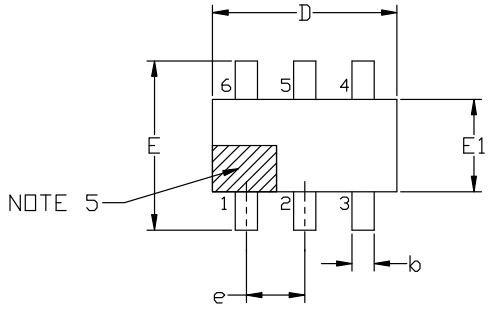

**Figure 10. Diode Forward Voltage vs. Current**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

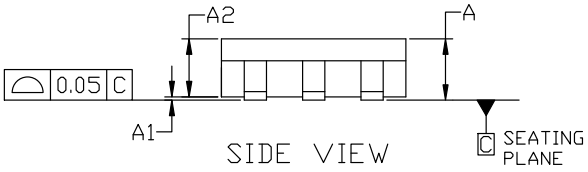


**TSOP−6 3.00x1.50x0.90, 0.95P**
CASE 318G
ISSUE W

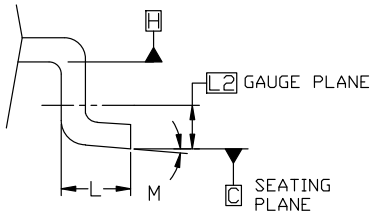
DATE 26 FEB 2024



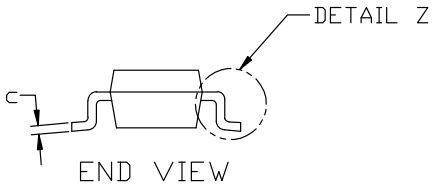

TOP VIEW




SIDE VIEW



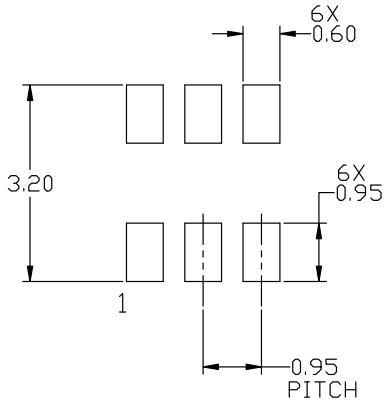

DETAIL Z
SCALE 3:1




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.06 | 0.10 |
| A2 | 0.80 | 0.90 | 1.00 |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.85 | 0.95 | 1.05 |
| L | 0.20 | 0.40 | 0.60 |
| L2 | 0.25 BSC | | |
| M | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT

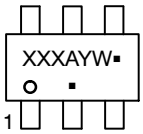
*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB14888C** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **TSOP−6 3.00x1.50x0.90, 0.95P** | | **PAGE 1 OF 2** |

**TSOP−6 3.00x1.50x0.90, 0.95P**
CASE 318G
ISSUE W

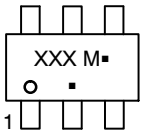
DATE 26 FEB 2024

**GENERIC**
**MARKING DIAGRAM***




**IC**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package




**STANDARD**

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales