PYTHON 5.0/2.0 MegaPixels Global Shutter CMOS Image Sensors

NOIP1SN5000A

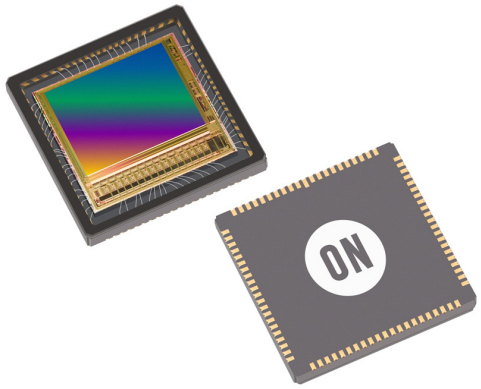

Figure 1. PYTHON 5000

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Data Output Options
  - P1−SN/SE/FN: 8 LVDS Data Channels
  - P3−SN/SE: 4 LVDS Data Channels
- Size Options
  - PYTHON 2000: 1920 x 1200 Active Pixels, 2/3” Optical Format
  - PYTHON 5000: 2592 x 2048 Active Pixels, 1” Optical Format
- 4.8 μm x 4.8 μm Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN), Color (SE) and NIR (FN)
- Zero Row Overhead Time Mode Enabling Higher Frame Rate
- Frame Rate at Full Resolution, 8 LVDS Data Channels (P1−SN/SE/FN only)
  - 100/85 frames per second @ 5 MP (Zero ROT/Non−Zero ROT)
  - 230/180 frames per second @ 2 MP (Zero ROT/Non−Zero ROT)
  - 255/200 frames per second @ Full HD (Zero ROT/Non−Zero ROT)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- Eight/Four/Two/One LVDS High Speed Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- Dual Power Supply (3.3 V and 1.8 V)
- −40°C to +85°C Operational Temperature Range
- 84-pin LCC and 128−pad LGA
- Power Dissipation
  - 1.45 W (P1−SN/SE/FN, 8 LVDS, NZROT)
  - 915 mW (P1−SN/SE/FN, P3−SN/SE, 4 LVDS, NZROT)
  - 520 mW (P1−SN/SE/FN, P3−SN/SE, 2 LVDS, NZROT)
  - 370 mW (P1−SN/SE/FN, P3−SN/SE, 1 LVDS, NZROT)
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Security
- Intelligent Traffic Systems (ITS)

Description

The PYTHON 2000 and PYTHON 5000 image sensors utilize high sensitivity 4.8 μm x 4.8 μm pixels that support low noise “pipelined” and “triggered” global shutter readout modes. The sensors support correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image’s black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to sixteen regions can be programmed, achieving even higher frame rates.

The image data interface of the P1−SN/SE/FN devices consists of eight LVDS lanes, facilitating frame rates up to 100 frames per second in Zero ROT mode for the PYTHON 5000. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end.

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The P3−SN/SE devices are the same as the P1−SN/SE/FN but with only four of the eight LVDS data channels enabled, facilitating frame rates of 45 frames per second in Non Zero ROT (NZROT) for the PYTHON 5000.

ORDERING INFORMATION

Part Number	Description	Package
PYTHON 5000		
NOIP1SN5000A−QDI	5 MegaPixel, Monochrome	84−pin LCC
NOIP1SE5000A−QDI	5 MegaPixel, Bayer Color	
NOIP1FN5000A−QDI	5 MegaPixel, Monochrome with enhanced NIR	
NOIP1SN5000A−QTI	5 MegaPixel, Monochrome, Protective Film	
NOIP1SE5000A−QTI	5 MegaPixel, Bayer Color, Protective Film	
NOIP1FN5000A−QTI	5 MegaPixel, Monochrome with enhanced NIR, Protective Film	
NOIP3SN5000A−QDI	5 MegaPixel, 4 LVDS Outputs, Monochrome	
NOIP3SE5000A−QDI	5 MegaPixel, 4 LVDS Outputs, Bayer Color	
NOIP3SN5000A−QTI	5 MegaPixel, 4 LVDS Outputs, Monochrome, Protective Film	
NOIP3SE5000A−QTI	5 MegaPixel, 4 LVDS Outputs, Bayer Color, Protective Film	
NOIP1SN5000A−LTI	5 MegaPixel, Monochrome, Protective Film	128−pad LGA
NOIP1SE5000A−LTI	5 MegaPixel, Bayer Color, Protective Film	
NOIP1FN5000A−LTI	5 MegaPixel, Monochrome with enhanced NIR, Protective Film	
NOIP3SN5000A−LTI	5 MegaPixel, 4 LVDS Outputs, Monochrome, Protective Film	
NOIP3SE5000A−LTI	5 MegaPixel, 4 LVDS Outputs, Bayer Color, Protective Film	
PYTHON 2000		
NOIP1SN2000A−QDI	2 MegaPixel, Monochrome	84−pin LCC
NOIP1SE2000A−QDI	2 MegaPixel, Bayer Color	
NOIP1FN2000A−QDI	2 MegaPixel, Monochrome with enhanced NIR	
NOIP1SN2000A−QTI	2 MegaPixel, Monochrome, Protective Film	
NOIP1SE2000A−QTI	2 MegaPixel, Bayer Color, Protective Film	
NOIP1FN2000A−QTI	2 MegaPixel, Monochrome with enhanced NIR, Protective Film	
NOIP1SN2000A−LTI	2 MegaPixel, Monochrome, Protective Film	128−pad LGA
NOIP1SE2000A−LTI	2 MegaPixel, Bayer Color, Protective Film	
NOIP1FN2000A−LTI	2 MegaPixel, Monochrome with enhanced NIR, Protective Film	

The P1−SN/SE/FN base part references the mono, color and NIR enhanced versions of the 8 LVDS interface; the P3−SN/SE base part references the mono and color version of the 4 LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

Package Mark for LCC−84 Pin Package

Line 1: NOIP**yxx RRRR**A where y is either “1” for 8 LVDS Outputs, “3” for 4 LVDS Outputs.
where xx denotes mono micro lens (SN) or color micro lens (SE) or NIR micro lens (FN)
RRRR is the resolution (5000), (2000)
Line 2: **−QDI** (LCC−84 without protective film), **−QTI** (LCC−84 with protective film)
Line 3: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

Package Mark for LGA−128 Pad Package

Package Side 1: NOIP**yxxRRRR**A**−LTI** where y is either “1” for 8 LVDS Outputs, “3” for 4 LVDS Outputs.
where xx denotes mono micro lens (SN) or color micro lens (SE)
RRRR is the resolution (5000), (2000)
−LTI (LGA−128 with protective film)
Package Side 2: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

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SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS (Note 1)

Parameter	Specification
Pixel Type	In−pixel CDS. Global shutter pixel architecture
Shutter Type	Pipelined and triggered global shutter
Frame Rate Zero ROT/ Non−Zero ROT Mode	P1−SN/SE/FN: PYTHON 2000: 230/180 fps PYTHON 5000: 100/85 fps P3−SN/SE: NA/45 fps
Master Clock	P1−SN/SE/FN, P3−SN/SE: 72 MHz when PLL is used, 360 MHz (10-bit) / 288 MHz (8-bit) when PLL is not used
Windowing	16 Randomly programmable windows. Normal, sub-sampled readout mode
ADC Resolution (Note 1)	10-bit, 8-bit
LVDS Outputs	P1−SN/SE/FN: 8/4/2/1 data + sync + clock P3−SN/SE: 4/2/1 data + sync + clock
Data Rate	P1−SN/SE/FN: 8 x 720 Mbps (10-bit) / 8 x 576 Mbps (8-bit) P3−SN/SE/FN: 4 x 720 Mbps (10−bit)
Power Dissipation (10−bit mode)	P1−SN/SE/FN: 1.45 W (8 data channels) P1−SN/SE/FN, P3−SN/SE: 915 mW (4 data channels) P1−SN/SE/FN, P3−SN/SE: 520 mW (2 data channels) P1−SN/SE/FN, P3−SN/SE: 370 mW (1 data channel)
Package Type	84-pin LCC, 128-pad LGA

Table 2. NOMINAL ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active Pixels	PYTHON 5000: 2592 (H) x 2048 (V) PYTHON 2000: 1984 (H) x 1264 (V)
Pixel Size	4.8 μm x 4.8 μm
Conversion Gain	0.096 LSB10/e^-, 140 μV/e^-
Temporal Noise	< 10.7 e^- (Non−Zero ROT, 1x gain) < 9.4 e^- (Non−Zero ROT, 2x gain)
Responsivity at 550 nm	7.5 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/5000
Full Well Charge	10000 e^-
Quantum Efficiency at 550 nm	57%
Pixel FPN	< 1.55 LSB10 (Non−Zero ROT) < 1.35 (Zero−ROT)
PRNU	< 10 LSB10 on half scale response of 525 LSB10
MTF	66% @ 535 nm − X-dir & Y-dir
Pixel Storage Node Leakage (PSNL) @ 20°C (t_int = 30 ms)	300 LSB10/s, 2800 e^-/s
Dark Signal @ 20°C	9.3 e^-/s, 1.0 LSB10/s
Dark Current Doubling Temperature	5.2°C
Dynamic Range	60 dB
Signal to Noise Ratio (SNR max)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
T_J	Operating junction temperature range	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Symbol	Parameter	Min	Max	Unit
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
T_S	ABS storage temperature range	−40	+150	°C
	ABS storage humidity range at 85°C		85	%RH

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Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2012	2000		V
	Charged Device Model (CDM): EIA/JESD22−C101, Class C1	500		
LU	Latch−up: JESD−78	100		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The ADC is 11−bit, down−scaled to 10−bit. The PYTHON uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. **onsemi** recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters − P1 − SN/SE/FN (ZROT) (Note: All ground pins (gnd_18, gnd_33 and gnd_colpc) should be connected to an external 0 V ground reference.)					
vdd_33	Supply voltage, 3.3 V	**3.2**	3.3	**3.4**	V
Idd_33	Current consumption 3.3 V supply		355		mA
vdd_18	Supply voltage, 1.8 V	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V supply		140		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply		10		mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V		1.45		W
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
Power Supply Parameters − P3 − SN/SE (NZROT) (Note: All ground pins (gnd_18, gnd_33 and gnd_colpc) should be connected to an external 0 V ground reference.)					
vdd_33	Supply voltage, 3.3 V	**3.2**	3.3	**3.4**	V
Idd_33	Current consumption 3.3 V supply (4/2/1 LVDS)		215		mA
vdd_18	Supply voltage, 1.8 V	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V supply (4/2/1 LVDS)		105		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply (4/2/1 LVDS)		5		mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V 4 LVDS, NZROT 2 LVDS, NZROT 1 LVDS, NZROT		 915 520 370		mW
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
I/O − P1−SN/SE/FN, P3−SN/SE (EIA/TIA−644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling − 4 data channels, 1 synchronization channel			720	Mbps
fserclock	Clock rate of output clock Clock output for mesochronous signaling			360	MHz
Vicm	LVDS input common mode level	0.3	1.25	1.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

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Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
I/O – P1–SN/SE/FN, P3–SN/SE (EIA/TIA–644): Conforming to standard/additional specifications and deviations listed					
Tccsk	Channel to channel skew (Training pattern should be used to correct per channel skew)			50	ps
Clock Specifications – P1–SN/SE/FN, P3–SN/SE					
fin	Input clock rate when PLL used			72	MHz
fin	Input clock when LVDS input used			360	MHz
tidc	Input clock duty cycle when PLL used	45	50	55	%
tj	Input clock jitter			20	ps
fspi	SPI clock rate when PLL used			10	MHz
ratspi (=fin/fspi)	10–bit (8 LVDS channels), PLL used – P1–SN/SE/FN only	6			
	10–bit (4 LVDS channels), PLL used	12			
	10–bit (2 LVDS channels), PLL used	24			
	10–bit (1 LVDS channel), PLL used	48			
	10–bit (8 LVDS channels), LVDS input used	30			
	10–bit (4 LVDS channels), LVDS input used	60			
ratspi (=fin/fspi)	10–bit (2 LVDS channels), LVDS input used	120			
	10–bit (1 LVDS channel), LVDS input used	240			
	8–bit (8 LVDS channels), PLL used	6			
	8–bit (4 LVDS channels), PLL used	12			
	8–bit (2 LVDS channels), PLL used	24			
	8–bit (1 LVDS channel), PLL used	48			
	8–bit (8 LVDS channels), LVDS input used	24			
	8–bit (4 LVDS channels), LVDS input used	48			
	8–bit (2 LVDS channels), LVDS input used	96			
	8–bit (1 LVDS channel), LVDS input used	192			

Frame Specifications – P1–SN/SE/FN

		Maximum			
		Non–Zero ROT	Zero ROT		Units
fps_roi1	Xres x Yres = 2592 x 2048	85	100		fps
fps_roi2	Xres x Yres = 2048 x 2048	100	130		fps
fps_roi3	Xres x Yres = 1920 x 1200	180	230		fps
fps_roi4	Xres x Yres = 1920 x 1080	200	255		fps
fps_roi5	Xres x Yres = 1600 x 1200	205	275		fps
fps_roi6	Xres x Yres = 1024 x 1024	395	480		fps
fps_roi7	Xres x Yres = 1280 x 720	390	550		fps
fps_roi8	Xres x Yres = 800 x 600	620	985		fps
fps_roi9	Xres x Yres = 640 x 480	855	1450		fps
fps_roi10	Xres x Yres = 512 x 512	890	1555		fps

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5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
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Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
Frame Specifications – P1–SN/SE/FN					
fps_roi11	Xres x Yres = 256 x 256	2065	2830		fps
fps_roi12	Xres x Yres = 544 x 20	7980	10345		fps
fpix	Pixel rate (8 channels at 72 Mpix/s)	576	576		Mpix/s

Frame Specifications – P3–SN/SE

		Maximum (Non–Zero ROT)			
		4 LVDS	2 LVDS	1 LVDS	Units
fps_roi1	Xres x Yres = 2592 x 2048	45	25	10	fps
fps_roi2	Xres x Yres = 2048 x 2048	55	30	15	fps
fps_roi3	Xres x Yres = 1920 x 1200	100	55	25	fps
fps_roi4	Xres x Yres = 1920 x 1080	110	60	30	fps
fps_roi5	Xres x Yres = 1600 x 1200	115	60	30	fps
fps_roi6	Xres x Yres = 1024 x 1024	195	105	55	fps
fps_roi7	Xres x Yres = 1280 x 720	230	125	65	fps
fps_roi8	Xres x Yres = 800 x 600	385	220	115	fps
fps_roi9	Xres x Yres = 640 x 480	550	320	175	fps
fps_roi10	Xres x Yres = 512 x 512	590	350	190	fps
fps_roi11	Xres x Yres = 256 x 256	1590	990	580	fps
fps_roi12	Xres x Yres = 544 x 20	6260	4340	2690	fps
fpix	Pixel rate (8 channels at 72 Mpix/s)	288	144	72	Mpix/s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
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8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

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Color Filter Array

The PYTHON color sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

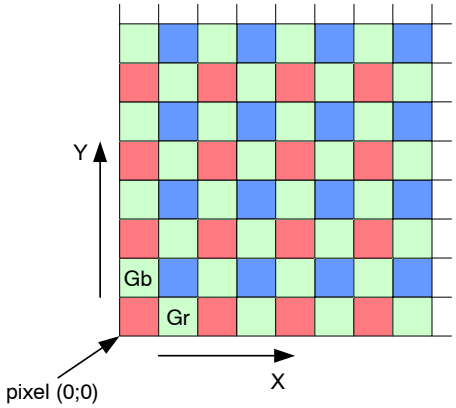

Figure 2. Color Filter Array for the Pixel Array

Quantum Efficiency

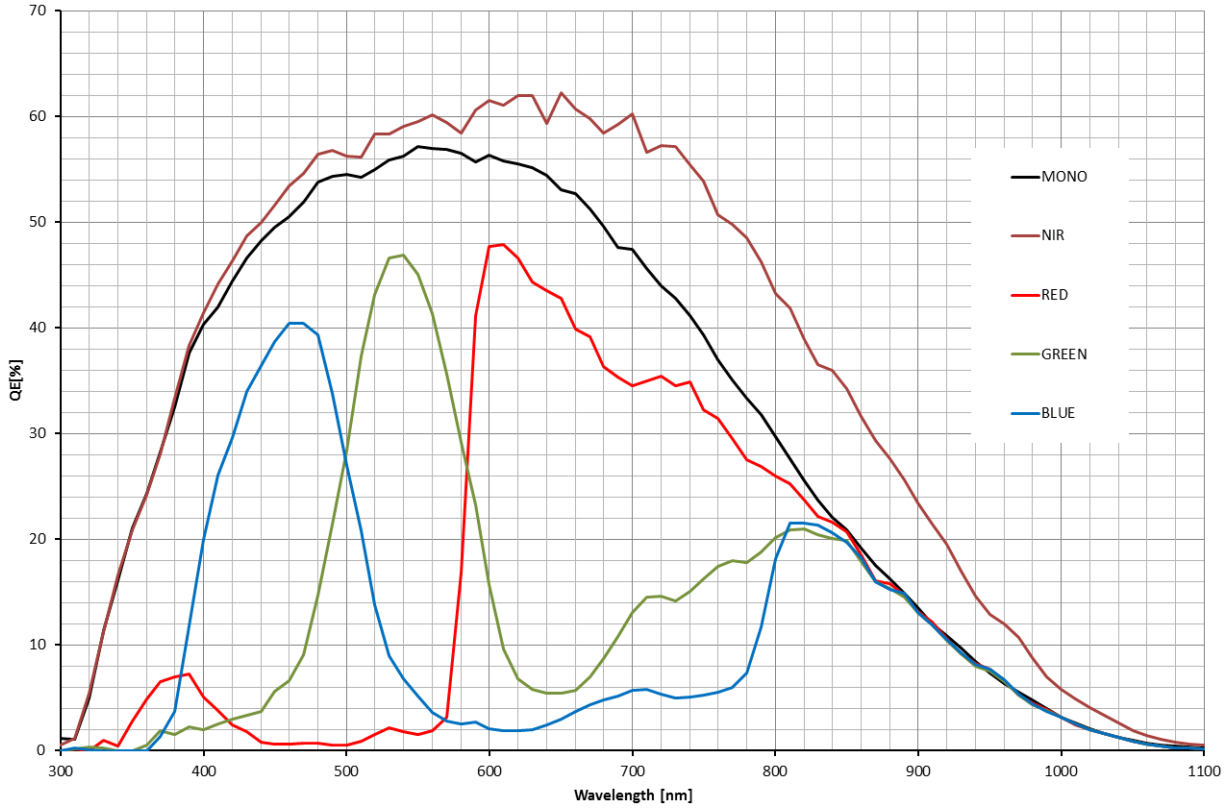

Figure 3. Quantum Efficiency Curves

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Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

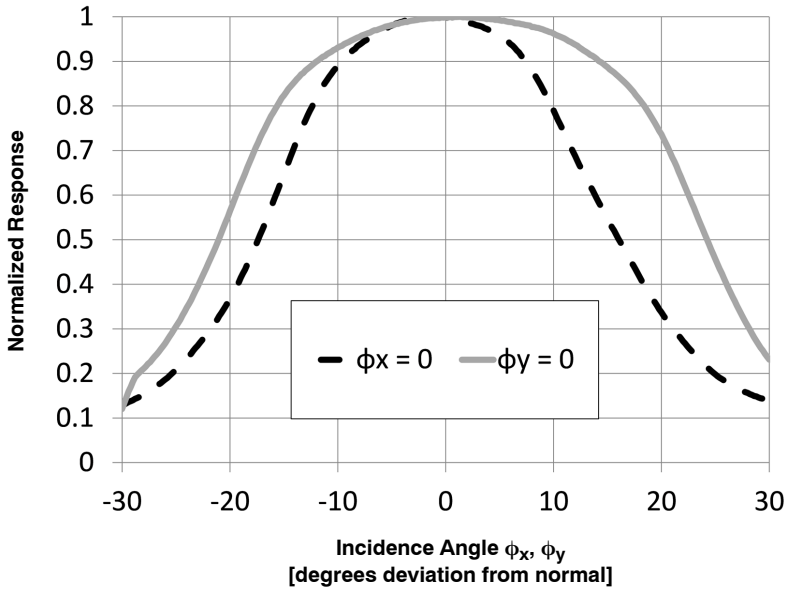
Angular Dependency of Photoresponse of a Pixel

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 4, where definitions of angles ϕx and ϕy are as described by Figure 5.

Microlens Shift across Array and CRA

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 6.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. In the standard version of Python 5000, the CRA varies nearly linearly with distance from the center as illustrated in Figure 7, with a corner CRA of approximately 5.4 degrees. This edge CRA is matching a lens with exit pupil distance of ~80 mm.



Note that the Photoresponse Peaks near Normal Incidence for Center Pixels

Figure 4. Center Pixel Photoresponse to a Fixed Optical Power with Incidence Angle Varied along ϕx and ϕy

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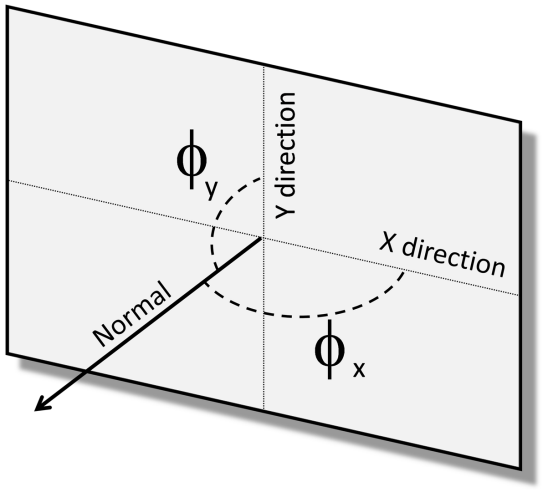
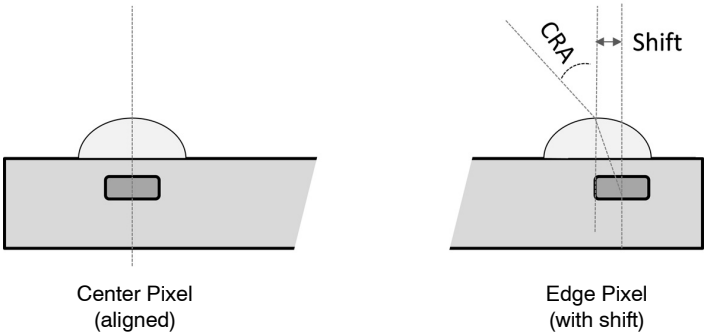


Figure 5. Definition of Angles Used in Figure 4



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axes of the microlens and the photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the normal of the pixel array.

Figure 6. Principle of Microlens Shift

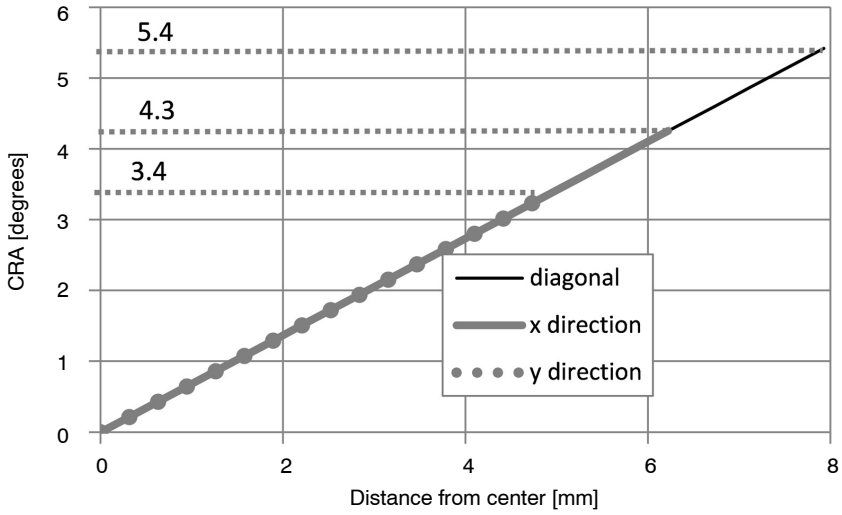


Figure 7. Variation of Peak Responsivity Angle (CRA)

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OVERVIEW

Figures 8 gives an overview of the major functional blocks of the PYTHON sensor.

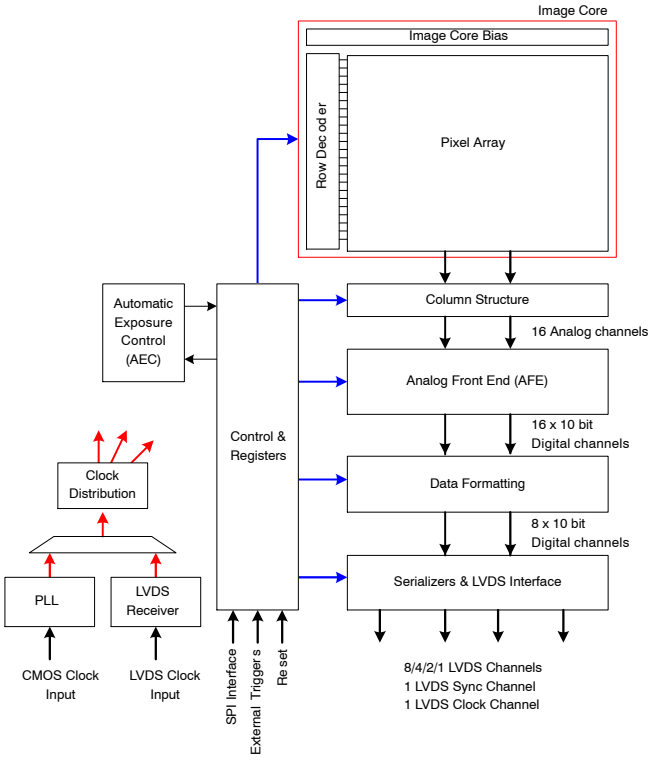

Figure 8. Block Diagram

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The PYTHON 5000 pixel array contains 2592 (H) x 2048 (V) readable pixels with a pixel pitch of 4.8 µm.

The PYTHON 2000 image array contains 1984 (H) x 1264 (V) readable pixels, inclusive of 32 pixels on each side to allow for reprocessing or color reconstruction.

The sensors use in−pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in global shutter mode with the function of the row drivers is to access the image array to reset or read the pixel data. The row drivers are controlled by the on−chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 72 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz in 10−bit mode and 288 MHz in 8−bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample−and−hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 16 parallel differential outputs operating at a frequency of 36 MHz. At this stage, the reset signal and integrated signal values are transferred into an FPN−corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal. The column multiplexer also supports read−1−skip−1 and read−2−skip−2 mode. Enabling this mode increases the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents used on chip. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

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Analog Front End

The AFE contains 16 channels, each containing a PGA and a 10−bit ADC.

For each of the 16 channels, a pipelined 10−bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10−bit or 8−bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10−bit mode, the maximum output data rate is 720 Mbps per channel. In 8−bit mode, the maximum output data rate is 576 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system−level image reconstruction.

Channel Multiplexer

The P1−SN/SE/FN LVDS channel multiplexer provides a 8:4, 8:2 and 8:1 feature, in addition to utilizing all 8 output channels.

The P3−SN/SE LVDS channel multiplexer provides a 4:2 and 4:1 feature, in addition to utilizing all 4 output channels.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

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OPERATING MODES

Global Shutter Mode

The PYTHON 2000 and PYTHON 5000 operates in pipelined or triggered global shutter modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 9 shows the integration and readout sequence for the global shutter mode. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

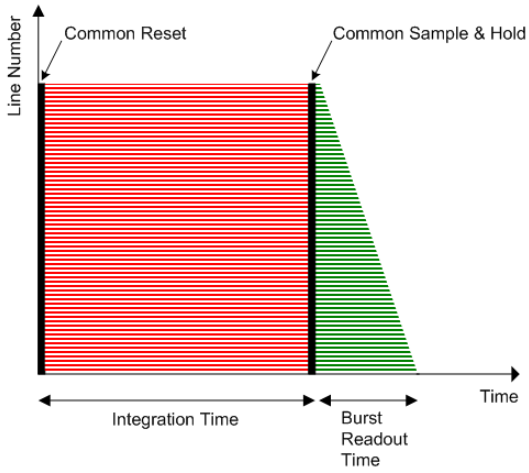

Figure 9. Global Shutter Operation

Pipelined Global Shutter Mode

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 10 shows the exposure and readout time line in pipelined global shutter mode.

Master Mode

The PYTHON 2000 and PYTHON 5000 operate in pipelined or triggered global shuttering modes. In this mode, light, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

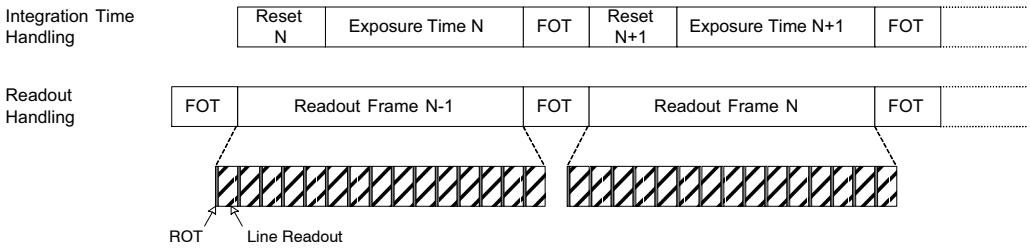

Figure 10. Pipelined Shutter Operation in Master Mode

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins. Figure 11 shows the relation between the external trigger signal and the exposure/readout timing.

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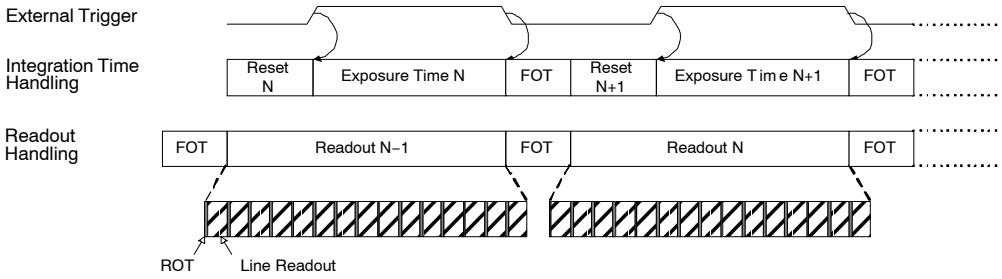

Figure 11. Pipelined Shutter Operation in Slave Mode

Triggered Global Shutter Mode

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global shutter mode can also be controlled in a master or in a slave mode.

Master Mode

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 12 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

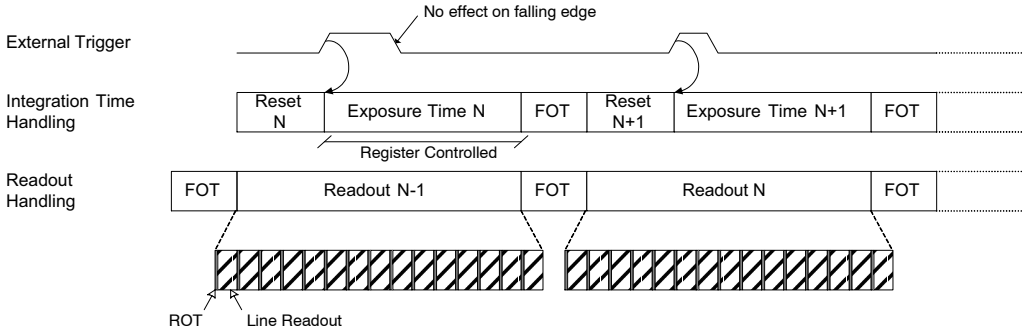

Figure 12. Triggered Shutter Operation in Master Mode

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de−asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

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Non−Zero and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 13.

In Reduced/Zero ROT operation mode (refer to Figure 14), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter (‘overhead’ spent per line is reduced).

The integration time and gain parameters can be reconfigured without any visible image artifact in Normal ROT mode. Column−level offset corrections are required in Zero ROT mode. Refer to Column−Level Image Correction application note in the PYTHON Developer’s Guide AND9362/D available at the Image Sensor Portal.

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock−rate.

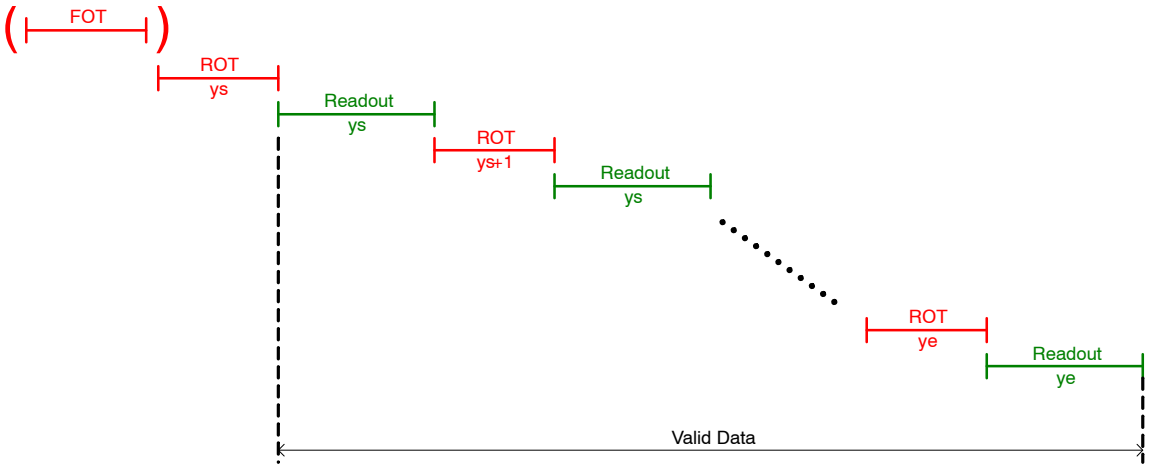

Figure 13. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Non−Zero ROT Readout.

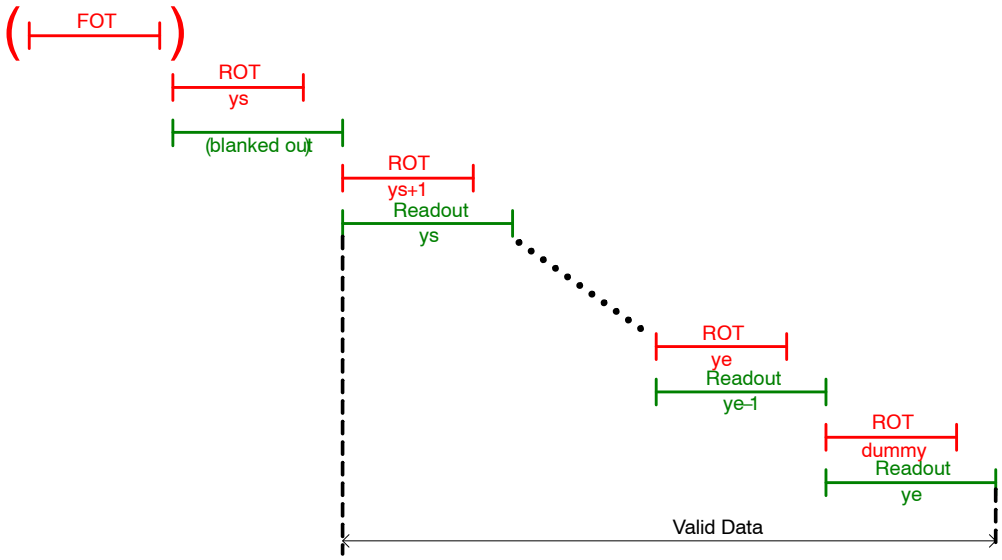

Figure 14. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.

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SENSOR OPERATION

Flowchart

Figure 15 shows the sensor operation flowchart. The sensor has six different ‘states’. Every state is indicated with the oval circle. These states are Power off, Low power standby, Standby (1), Standby (2), Idle, Running.

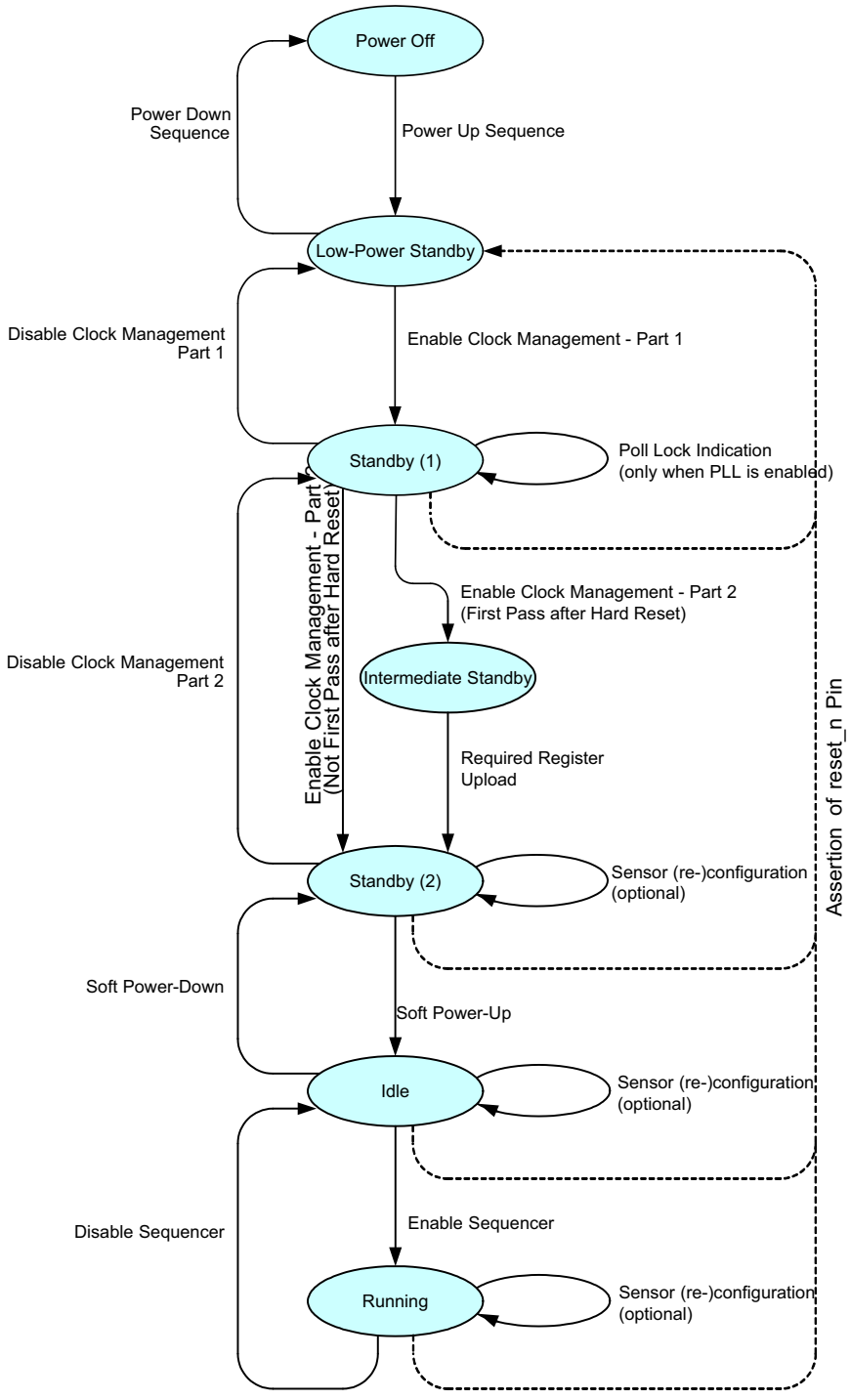

Figure 15. Sensor Operation Flowchart

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Sensor States

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are set to their default values (see Table 27).

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management – Part 1 on page 16

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 16 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp−up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de−asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

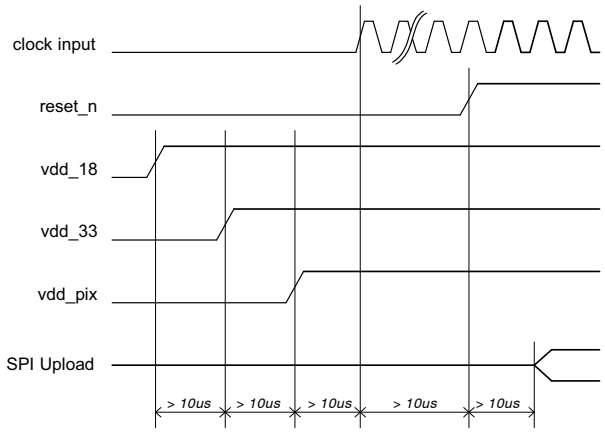

Figure 16. Power Up Sequence

Enable Clock Management

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre−defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

All SPI uploads to be executed to configure the sensor are available to customers under NDA at the **onsemi** Image Sensor Portal.

If the PLL is not used, the LVDS clock input must be running.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

Check the PLL_lock flag 24[0] by reading the SPI register. When the flag is set, the ‘Enable Clock Management− Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 15 on page 15.

Required Register Upload

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction.

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads.

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 16.

The ‘Enable Sequencer’ action consists of enabling bit 192[0].

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User Actions: Functional Modes to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of disabling bit 192[0].

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads.

Disable Clock Management

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation.

Power Down Sequence

Figure 17 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

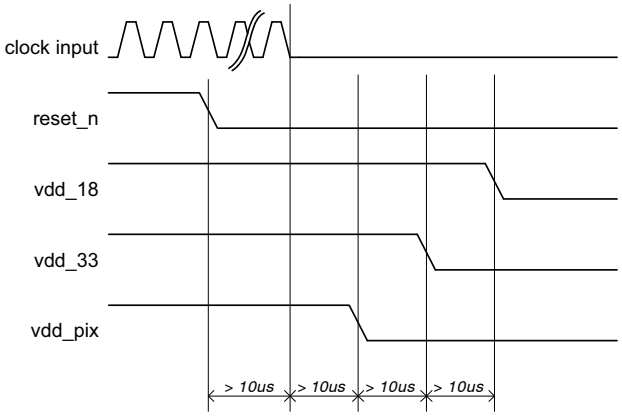

Figure 17. Power Down Sequence

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Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30−32 for more information.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 26 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 27 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 6. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64−71	Configure according to recommendation
Charge Pump	72	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: • triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 7. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128−129 197[12:8]	Reconfiguration of these registers may have an impact on the black−level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.

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Table 7. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Sync codes	129[13] 116–126	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144, 146–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 8. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 8. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling	192[7]	Subsampling is synchronized to a new frame start.
ROI configuration	195 256–303	A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	199–203	Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master).
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] – gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re−enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 18 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

Figure 19 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de−asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

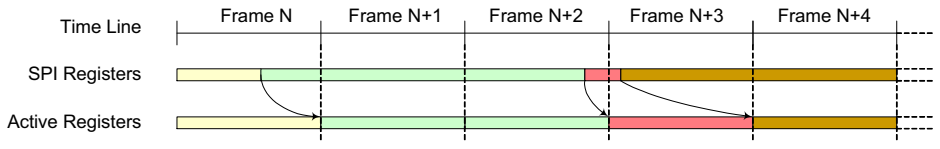

Figure 18. Frame Synchronization of Configurations (no freezing)

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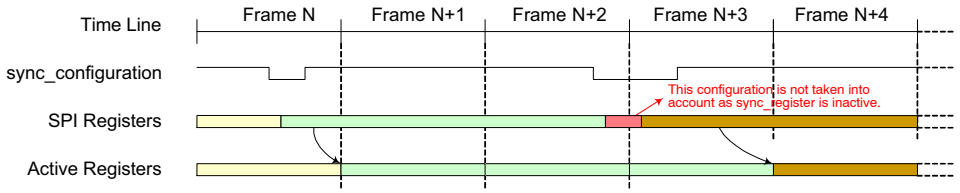

Figure 19. reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 9 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 9. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[15:0] subsampling	Update of active ROI configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. reconfiguration of active windows is not gated by this setting.

Window Configuration

Global Shutter Mode

Up to 16 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 303. Each window can be activated or deactivated separately using register 195. It is possible to reconfigure the inactive windows while the sensor is acquiring images.

Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one register.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 16 columns contained in one kernel. This implies 16 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black−level algorithm are listed in Table 19.

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Table 10. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Address	Register Name	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. **Note:** When the automatic black−level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black−level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Each black line contains 162 kernels.
197[12:8]	gate_first_line	A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black−level calibration functionality is enabled when set to '1'. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to '0', the automatic black−level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to '0'. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to '0', the black calibration offset is added to each pixel. If set to '1', the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to '1'.
128[10:8]	black_samples	The black samples are low−pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is 2^ black_samples. **Note:** An error is reported by the device if more samples than available are requested (refer to register 136).
Black Level Filtering Monitoring		
136	blackcal_error0	An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

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Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 20 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON sensor uses 9−bit addresses and 16−bit data words.

Data driven by the system is colored blue in Figure 16, while data driven by the sensor is colored yellow. The data in grey indicates high−Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle after selecting the sensor, the 9−bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 20. The sensor samples this address data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16−bit data, most significant bit first.
   - For read commands, the sensor returns the data on the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Note that the maximum frequency for the SPI interface scales with the input clock frequency, bit depth and LVDS output multiplexing as described in Table 5.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

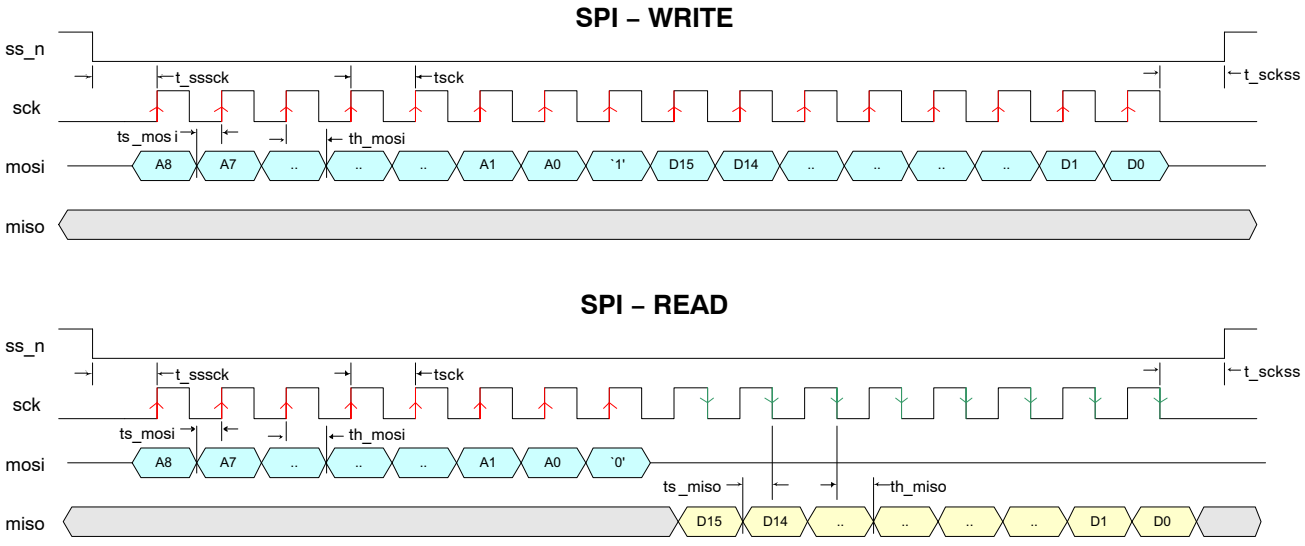

Figure 20. SPI Read and Write Timing Diagram

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Table 11. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2−10	ns
th_miso	Hold time for miso	tsck/2−20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

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IMAGE SENSOR TIMING AND READOUT

Global Shutter Mode

Pipelined Global Shutter (Master)

The integration time is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers reset_length and exposure and is read as number of system clock cycles.

The exposure control for (Pipelined) Global Master mode is depicted in Figure 21.

The pixel values are transferred to the storage node during FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the reset_length and mult_timer registers, as shown in the figure. Note that meanwhile the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTE: The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.

- Make sure that the sum of the reset time and exposure time exceeds the time required to readout all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.
- Alternatively, it is possible to specify the frame time and exposure time. The sensor automatically calculates the required reset time. This mode is enabled by the fr_mode register. The frame time is specified in the register fr_length.

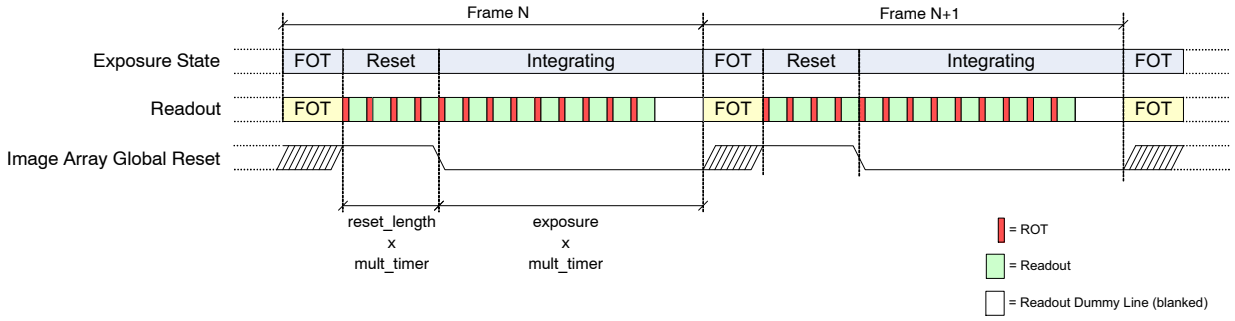

Figure 21. Integration Control for (Pipelined) Global Shutter Mode (Master)

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Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger0 pin. The exposure or integration time is defined by the registers exposure and mult_timer, as in the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 22.

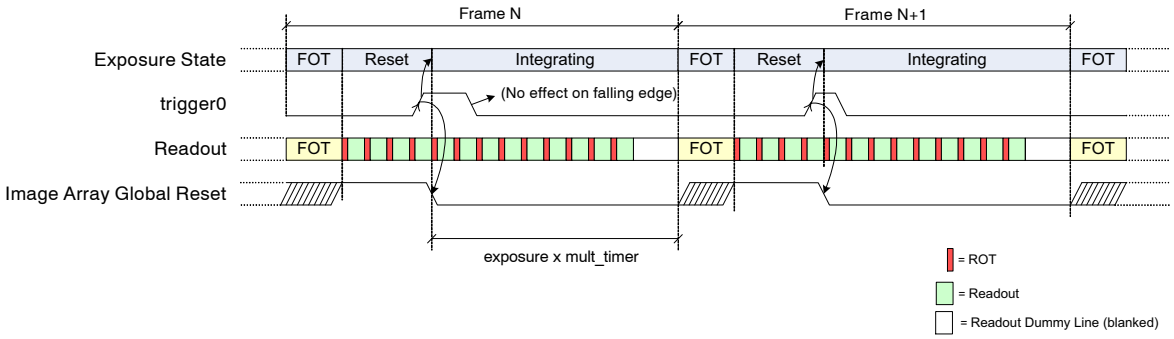

Figure 22. Exposure Time Control in Triggered Shutter Mode (Master)

Notes:

- The falling edge on the trigger pin does not have any impact. Note however the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The registers fr_length, exposure and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer to the pixel storage node and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 23.

Notes:

- The registers exposure, fr_length, and mult_timer are not used in this mode.
- The start of exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the trigger is de−asserted before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

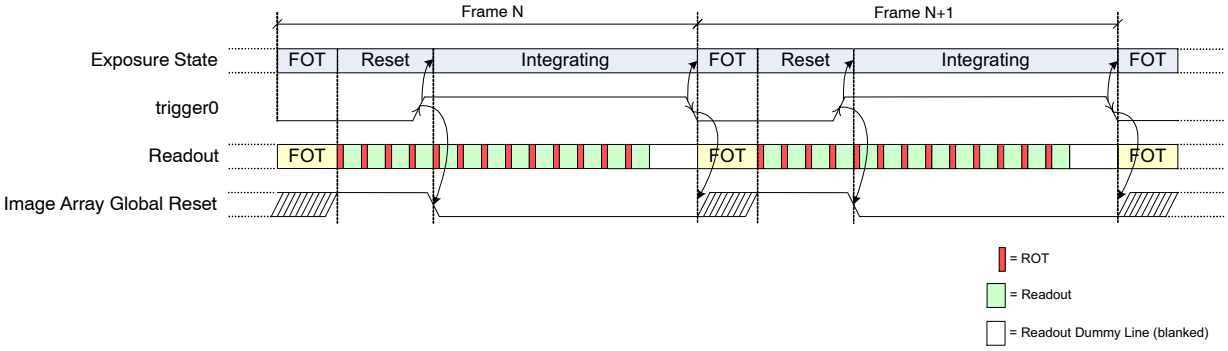

Figure 23. Exposure Time Control in Global−Slave Mode

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ADDITIONAL FEATURES

Multiple Window Readout

The PYTHON 2000 and PYTHON 5000 sensor supports multiple window readout, which means that only the user−selected Regions Of Interest (ROI) are read out. This allows limiting data output for every frame, which in turn allows increasing the frame rate. In global shutter mode, up to eight ROIs can be configured.

Window Configuration

Figure 24 shows the four parameters defining a region of interest (ROI).

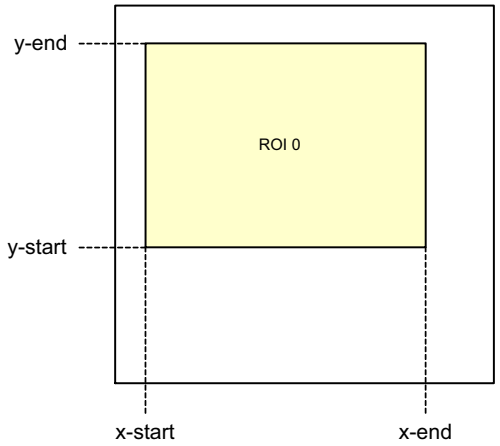

Figure 24. Region of Interest Configuration

- x−start[7:0]

x−start defines the x−starting point of the desired window. The sensor reads out 16 pixels in one single clock cycle. As a consequence, the granularity for configuring the x−start position is also 16 pixels for no sub sampling. The value configured in the x−start register is multiplied by 16 to find the corresponding column in the pixel array.

- x−end[7:0]

This register defines the window end point on the x−axis. Similar to x−start, the granularity for this configuration is one kernel. x−end needs to be larger than x−start.

- y−start[9:0]

The starting line of the readout window. The granularity of this setting is one line, except with color sensors where it needs to be an even number.

- y−end[9:0]

The end line of the readout window. y−end must be configured larger than y−start. This setting has the same granularity as the y−start configuration.

Up to eight windows can be defined, possibly (partially) overlapping, as illustrated in Figure 25.

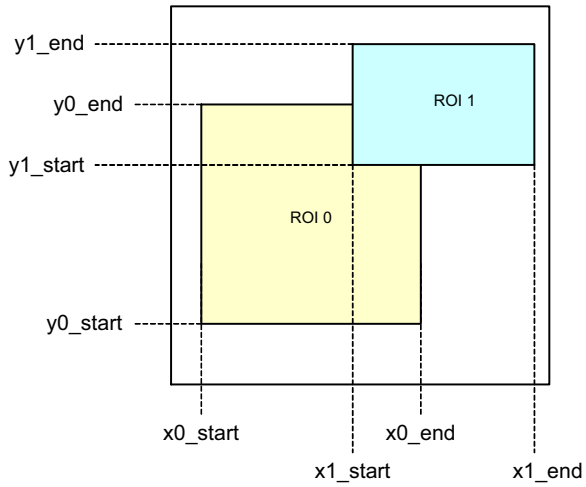

Figure 25. Overlapping Multiple Window Configuration

The sequencer analyses each line that needs to be read out for multiple windows.

Restrictions

The following restrictions for each line are assumed for the user configuration:

- Windows are ordered from left to right, based on their x−start address:

$$x_start_roi(i) \leq x_start_roi(j) \; AND$$

$$x_end_roi(i) \leq x_end_roi(j)$$

$$\text{Where } j > i$$

Processing Multiple Windows

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y−counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, it is initialized to the y−start address of the first window and it runs until the y−end address of the last window to be read out. The last window is configured by the configuration registers and it is not necessarily window #15.

The x−counter starts counting from the x−start address of the window with the lowest ID which is active on the addressed line. Only windows for which the current y−address is enclosed are taken into account for scanning. Other windows are skipped.

Figure 26 illustrates a practical example of a configuration with five windows. The current position of the read pointer (ys) is indicated by a red line crossing the image

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array. For this position of the read pointer, three windows need to be read out. The initial start position for the x−kernel pointer is the x−start configuration of ROI1. Kernels are scanned up to the ROI3 x−end position. From there, the x−pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4's x−end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI1.

Notes:

- The starting point for the readout pointer at the start of a frame is the y−start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in y−direction. In Figure 26, this is the case when reaching the end of ROI0 where the read pointer jumps to the y−start position of ROI1
- The x−pointer starting position is equal to the x−start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x−pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.
- Each window can be activated separately. There is no restriction on which window and how many of the 16 windows are active.

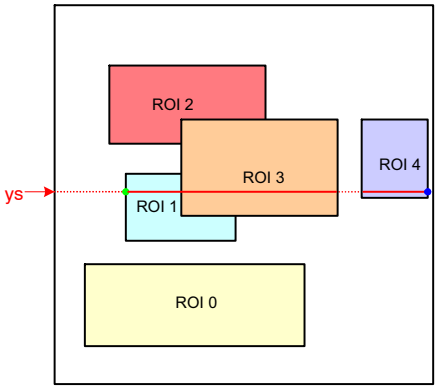

Figure 26. Scanning the Image Array with Five Windows

Subsampling

Subsampling is used to reduce the image resolution. This allows increasing the frame rate. Two subsampling modes are supported: for monochrome and NIR enhanced sensors (P1−SN/FN and P3−SN) and color sensors (P1−SE and P3−SE).

Monochrome Sensors

For monochrome sensors, the read−1−skip−1 subsampling scheme is used. Subsampling occurs both in x− and y− direction.

Color Sensors

For color sensors, the read−2−skip−2 subsampling scheme is used. Subsampling occurs both in x− and y− direction. Figure 27 shows which pixels are read and which ones are skipped.

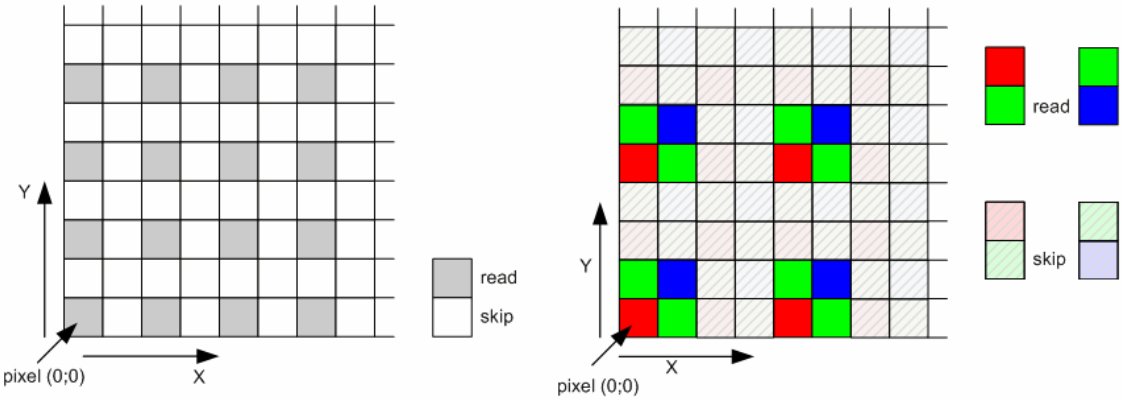

Figure 27. Subsampling Scheme for Monochrome and Color Sensors

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Reverse Readout in Y−direction

Reverse readout in y−direction can be done by asserting reverse_y (reg 194[8]). The reference for y_start and y_end pointers is reversed.

Channel Multiplexing

The PYTHON 2000 and PYTHON 5000 image sensors contains a function for channel multiplexing the output channels. Using this function, one may for instance use the device with sync+clock+8 data channels. Enabling the channel multiplexing is done through register 32[5:4]. The default value of 0 disables all channel multiplexing. Higher values sets higher degree of channel multiplexing. The channels that are used per degree of multiplexing are shown in Table 5. The unused data channels are powered down and will not send any data.

Table 12. LVDS DATA OUTPUT CHANNELS USED WITH CHANNEL MULTIPLEXING

# outputs	PYTHON 2000 / PYTHON 5000 − LVDS Channels								Register 32[5:4] Data	Register 211 Data
8 channels	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	0	0x0E49
4 channels	Ch 0		Ch 2		Ch 4		Ch 6		1	0x0E39
2 channels	Ch 0		Ch 2						2	0x0E29
1 channel	Ch 0								3	0x0E19

1. P1−SN/SE/FN supports 8, 4, 2, 1 LVDS outputs while P3−SN/SE supports 4, 2, 1 LVDS outputs.
2. Use P3−SN/SE bias uploads for P1−SN/SE/FN when operating in mux mode.

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is minimal equal to 1. The length of the black lines depends on the operation mode. The sensor always reads out the entire line (162 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual output interface, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, however without Frame Start and Ends (only Line Start/End). The Sync code following the Line Start and Line End indications (“window ID”) contains the active window number, which is 0. Black reference data is classified by a BL code.

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Signal Path Gain

Analog Gain Stages

Referring to Table 13, several gain settings are available in the analog data path to apply gain to the analog signal before it is digitized.

The moment a gain reconfiguration is applied and becomes valid can be controlled by the gain_lat_comp configuration.

With ‘gain_lat_comp’ set to ‘0’, the new gain configurations are applied from the very next frame.

With ‘gain_lat_comp’ set to ‘1’, the new gain settings are postponed by one extra frame. This feature is useful when exposure time and gain are reconfigured together, as an exposure time update always has one frame latency.

Table 13. SIGNAL PATH GAIN STAGES

Address	Gain Setting	Analog Gain Non−Zero and Zero ROT
204[12:0]	0x01E1	1
204[12:0]	0x00A1	1.6
204[12:0]	0x0021	2
204[12:0]	0x0083	2.6
204[12:0]	0x0085	3.2
204[12:0]	0x0081	4
204[12:0]	0x0086	5.3
204[12:0]	0x0082	8

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Digital Gain Stage

The digital gain stage allows fine gain adjustments on the digitized samples. The gain configuration is an absolute 5.7 unsigned number (5 digits before and 7 digits after the decimal point).

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Automatic Exposure Control

The exposure control mechanism has the shape of a general feedback control system. Figure 28 shows the high level block diagram of the exposure control loop.

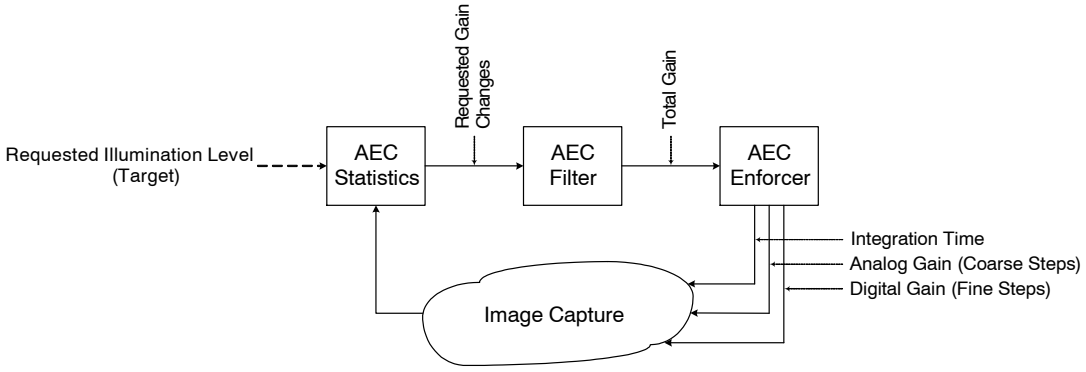

Figure 28. Automatic Exposure Control Loop

Three main blocks can be distinguished:

- The **statistics block** compares the average of the current image's samples to the configured target value for the average illumination of all pixels
- The relative gain change request from the statistics block is filtered through the **AEC Filter block** in the time domain (low pass filter) before being integrated. The output of the filter is the total requested gain in the complete signal path.
- The **enforcer block** accepts the total requested gain and distributes this gain over the integration time and gain stages (both analog and digital)

The automatic exposure control loop is enabled by asserting the aec_enable configuration in register 160.

NOTE: Dual and Triple slope integration is not supported in conjunction with the AEC.

AEC Statistics Block

The statistics block calculates the average illumination of the current image. Based on the difference between the calculated illumination and the target illumination the statistics block requests a relative gain change.

Statistics Subsampling and Windowing

For average calculation, the statistics block will sub−sample the current image or windows by taking every fourth sample into account. Note that only the pixels read out through the active windows are visible for the AEC. In the case where multiple windows are active, the samples will be selected from the total samples. Samples contained in a region covered by multiple (overlapping) window will be taking into account only once.

It is possible to define an AEC specific sub−window on which the AEC will calculate it's average. For instance, the sensor can be configured to read out a larger frame, while the illumination is measured on a smaller region of interest, e.g. center weighted as shown in Table 14.

Table 14. AEC SAMPLE SELECTION

Register	Name	Description
192[10]	roi_aec_enable	When 0x0, all active windows are selected for statistics calculation. When 0x1, the AEC samples are selected from the active pixels contained in the region of interest defined by roi_aec
253−255	roi_aec	These registers define a window from which the AEC samples will be selected when roi_aec_enable is asserted. Configuration is similar to the regular region of interests. The intersection of this window with the active windows define the selected pixels. It is important that this window at least overlaps with one or more active windows.

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Target Illumination

The target illumination value is configured by means of register *desired_intensity* as shown in Table 15.

Table 15. AEC TARGET ILLUMINATION CONFIGURATION

Register	Name	Description
161[9:0]	desired_intensity	Target intensity value, on 10−bit scale. For 8−bit mode, target value is configured on desired_intensity[9:2]

Color Sensor

The weight of each color can be configured for color sensors by means of scale factors. Note these scale factor are only used to calculate the statistics in order to compensate for (off−chip) white balancing and/or color matrices. The pixel values itself are not modified.

The scale factors are configured as 3.7 unsigned numbers (0x80 = unity). Refer to Table 16 for color scale factors. For mono sensors, configure these factors to their default value.

Table 16. COLOR SCALE FACTORS

Register	Name	Description
162[9:0]	red_scale_factor	Red scale factor for AEC statistics
163[9:0]	green1_scale_factor	Green1 scale factor for AEC statistics
164[9:0]	green2_scale_factor	Green2 scale factor for AEC statistics
165[9:0]	blue_scale_factor	Blue scale factor for AEC statistics

AEC Filter Block

The filter block low−pass filters the gain change requests received from the statistics block.

The filter can be restarted by asserting the restart_filter configuration of register 160.

AEC Enforcer Block

The enforcer block calculates the four different gain parameters, based on the required total gain, thereby respecting a specific hierarchy in those configurations. Some (digital) hysteresis is added so that the (analog) sensor settings don't need to change too often.

Exposure Control Parameters

The several gain parameters are described below, in the order in which these are controlled by the AEC for large adjustments. Small adjustments are regulated by digital gain only.

- Exposure Time

The exposure is the time between the global image array reset de−assertion and the pixel charge transfer. The granularity of the integration time steps is configured by the *mult_timer* register.

NOTE: The *exposure_time* register is ignored when the AEC is enabled. The register *fr_length* defines the frame time and needs to be configured accordingly.

- Analog Gain

The sensor has two analog gain settings. Typically the AEC shall only regulate the first stage.

- Digital Gain

The last gain stage is a gain applied on the digitized samples. The digital gain is represented by a 5.7 unsigned number (i.e. 7 bits after the decimal point). While the analog gain steps are coarse, the digital gain stage makes it possible to achieve very fine adjustments.

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AEC Control Range

The control range for each of the exposure parameters can be pre−programmed in the sensor. Table 17 lists the relevant registers.

Table 17. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS

Register	Name	Description
168[15:0]	min_exposure	Lower bound for the integration time applied by the AEC
169[1:0]	min_mux_gain	Lower bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
169[3:2]	min_afe_gain	Lower bound for the second stage analog amplifier. This stage has only one configuration with the following approximative gain: 0x0 = 1.00x
169[15:4]	min_digital_gain	Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format
170[15:0]	max_exposure	Upper bound for the integration time applied by the AEC
171[1:0]	max_mux_gain	Upper bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
171[3:2]	max_afe_gain	Upper bound for the second stage analog amplifier This stage has only one configuration with the following approximative gain: 0x0 = 1.00x
171[15:4]	max_digital_ gain	Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format

AEC Update Frequency

As an integration time update has a latency of one frame, the exposure control parameters are evaluated and updated every other frame.

Note: The gain update latency must be postpone to match the integration time latency. This is done by asserting the *gain_lat_comp* register on address 204[13].

Exposure Control Status Registers

Configured integration and gain parameters are reported to the user by means of status registers. The sensor provides two levels of reporting: the status registers reported in the AEC address space are updated once the parameters are recalculated and requested to the internal sequencer. The status registers residing in the sequencer's address space on the other hand are updated once these parameters are taking effect on the image readout. Refer to Table 18 reflecting the AEC and Sequencer Status registers.

Table 18. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
AEC Status Registers		
184[15:0]	total_pixels	Total number of pixels taken into account for the AEC statistics.
186[9:0]	average	Calculated average illumination level for the current frame.
187[15:0]	exposure	AEC calculated exposure. Note: this parameter is updated at the frame end.
188[1:0]	mux_gain	AEC calculated analog gain (1^{st} stage) Note: this parameter is updated at the frame end.
188[3:2]	afe_gain	AEC calculated analog gain (2^{nd} stage) Note: this parameter is updated at the frame end.
188[15:4]	digital_gain	AEC calculated digital gain (5.7 unsigned format) Note: this parameter is updated at the frame end.

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Table 18. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
Sequencer Status Registers		
242[15:0]	mult_timer	mult_timer for current frame Note: this parameter is updated once it takes effect on the image.
243[15:0]	reset_length	Image array reset length for the current frame. Note: this parameter is updated once it takes effect on the image.
244[15:0]	exposure	Exposure for the current frame. Note: this parameter is updated once it takes effect on the image.
245[15:0]	exposure_ds	Dual slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
246[15:0]	exposure_ts	Triple slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
247[4:0]	mux_gainsw	1st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
247[12:5]	afe_gain	2nd stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
248[11:0]	db_gain	Digital gain configuration for the current frame (5.7 unsigned format). Note: this parameter is updated once it takes effect on the image.
248[12]	dual_slope	Dual slope configuration for the current frame **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.
248[13]	triple_slope	Triple slope configuration for the current frame. **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.

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Mode Changes and Frame Blanking

Dynamically reconfiguring the sensor may lead to corrupted or non-uniformilly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is summarized in the following table for the sensor's image related modes.

NOTE: Major mode switching (i.e. switching between master, triggered or slave mode) must be performed while the sequencer is disabled (reg_seq_enable = 0x0).

Table 19. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

Configuration	Corrupted Frame	Blanked Out Frame	Notes
Shutter Mode and Operation			
triggered_mode	Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0.		
slave_mode	Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0.		
subsampling	Enabling: No Disabling: Yes	Configurable	Configurable with blank_subsampling_ss register.
Frame Timing			
black_lines	No	No	
Exposure Control			
mult_timer	No	No	Latency is 1 frame
fr_length	No	No	Latency is 1 frame
exposure	No	No	Latency is 1 frame
Gain			
mux_gainsw	No	No	Latency configurable by means of gain_lat_comp register
afe_gain	No	No	Latency configurable by means of gain_lat_comp register.
db_gain	No	No	Latency configurable by means of gain_lat_comp register.
Window/ROI			
roi_active	See Note	No	Windows containing lines previously not read out may lead to corrupted frames.
roi*_configuration*	See Note	No	Reconfiguring the windows by means of roi*_configuration* may lead to corrupted frames when configured close to frame boundaries. It is recommended to (re)configure an inactive window and switch the roi_active register. See Notes on roi_active.
Black Calibration			
black_samples	No	No	If configured within range of configured black lines
auto_blackal_enable	See Note	No	Manual correction factors become instantly active when auto_blackcal_enable is deasserted during operation.
blackcal_offset	See Note	No	Manual blackcal_offset updates are instantly active.
CRC Calculation			
crc_seed	No	No	Impacts the transmitted CRC
Sync Channel			
bl_0	No	No	Impacts the Sync channel information, not the Data channels.
img_0	No	No	Impacts the Sync channel information, not the Data channels.
crc_0	No	No	Impacts the Sync channel information, not the Data channels.
tr_0	No	No	Impacts the Sync channel information, not the Data channels.

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Temperature Sensor

The PYTHON has an on−chip temperature sensor which returns a digital code (Tsensor) of the silicon junction temperature. The Tsensor output is a 8−bit digital count between 0 and 255, proportional to the temperature of the silicon substrate. This reading can be translated directly to a temperature reading in °C by calibrating the 8−bit readout at 0°C and 85°C to achieve an output accuracy of ±2°C. The Tsensor output can also be calibrated using a single temperature point (example: room temperature or the ambient temperature of the application), to achieve an output accuracy of ±5°C.

Note that any process variation will result in an offset in the bit count and that offset will remain within ±5°C over the temperature range of 0°C and 85°C. Tsensor output digital code can be read out through the SPI interface.

Output of the temperature sensor to the SPI:

tempd_reg_temp<7:0>: This is the 8−bit N count readout proportional to temperature.

Input from the SPI:

The *reg_tempd_enable* is a global enable and this enables or disables the temperature sensor when logic high or logic low respectively. The temperature sensor is reset or disabled when the input *reg_tempd_enable* is set to a digital low state.

Calibration using one temperature point

The temperature sensor resolution is fixed for a given type of package for the operating range of 0°C to +85°C and hence devices can be calibrated at any ambient temperature of the application, with the device configured in the mode of operation.

Interpreting the actual temperature for the digital code readout:

The formula used is

$\mathbf{T_J = R\ (Nread - Ncalib) + Tcalib}$

T_J = junction die temperature

R = resolution in degrees/LSB (typical 0.75 deg/LSB)

Nread = Tsensor output (LSB count between 0 and 255)

Tcalib = Tsensor calibration temperature

Ncalib = Tsensor output reading at Tcalib

Monitor Pins

The internal sequencer has two monitor outputs (monitor0 and monitor1) that can be used to communicate the internal states from the sequencer. A three−bit register configures the assignment of the pins as shown in Table 20.

Table 20. REGISTER SETTING FOR THE MONITOR SELECT PIN

monitor_select [2:0] 192 [13:11]	monitor pin	Description
0x0	monitor0 monitor1	'0' '0'
0x1	monitor0 monitor1	Integration Time ROT Indication ('1' during ROT, '0' outside)
0x2	monitor0 monitor1	Integration Time Dual/Triple Slope Integration (asserted during DS/TS FOT sequence)
0x3	monitor0 monitor1	Start of x−Readout Indication Black Line Indication ('1' during black lines, '0' outside)
0x4	monitor0 monitor1	Frame Start Indication Start of ROT Indication
0x5	monitor0 monitor1	First Line Indication ('1' during first line, '0' for all others) Start of ROT Indication
0x6	monitor0 monitor1	ROT Indication ('1' during ROT, '0' outside) Start of X−Readout Indication
0x7	monitor0 monitor1	Start of X−readout Indication for Black Lines Start of X−readout Indication for Image Lines

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DATA OUTPUT FORMAT

The PYTHON 2000 and PYTHON 5000 image sensors are available in two LVDS output configuration, P1−SN/SE/FN and P3−SN/SE. The P1−SN/SE/FN configuration utilizes eight LVDS output channels together with an LVDS clock output and an LVDS synchronization output channel. The P3−SN/SE configuration consists of four LVDS output channels together with an LVDS clock output and an LVDS synchronization output channel.

P1−SN/SE/FN, P3−SN/SE: Interface Version

LVDS Output Channels

The image data output occurs through eight LVDS data channels where a synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

Referring to Table 21, the eight data channels on the P1−SN/SE/FN option are used to output the image data only, while on the P3−SN/SE option, four data channel channels are utilized. The sync channel transmits information about the data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC codes).

8−bit / 10−bit Mode

The sensor can be used in 8−bit or 10−bit mode.

In 10−bit mode, the words on data and sync channel have a 10−bit length. The output data rate is 720 Mbps.

In 8−bit mode, the words on data and sync channel have an 8−bit length, the output data rate is 576 Mbps.

Note that the 8−bit mode can only be used to limit the data rate at the consequence of image data word depth. It is not supported to operate the sensor in 8−bit mode at a higher clock frequency to achieve higher frame rates. The P1−SN/SE/FN option supports 10−bit/8−bit in ZROT/NZROT mode, while the P3−SN/SE option supports 10−bit NZROT mode only.

Frame Format

The frame format in 8−bit mode is identical to the 10−bit mode with the exception that the Sync and data word depth is reduced to eight bits.

The frame format in 10−bit mode is explained by example of the readout of two (overlapping) windows as shown in Figure 29(a).

The readout of a frame occurs on a line−by−line basis. The read pointer goes from left to right, bottom to top.

Figure 29 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes information of ‘ROI 0’ are sent out, starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of ‘ROI 0’ and ‘ROI 1’ are sent out, until the line position of y0_end is reached. From there on, only data of ‘ROI 1’ appears on the data output channels until line position y1_end is reached

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the four data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS); the line end of the last line is replaced with a Frame End indication (FE). Each such frame synchronization code is followed by a window ID (range 0 to 7). For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out (as shown in the illustration: no LE/FE is transmitted for the overlapping part of window 0).

NOTES: In Figure 29, only Frame Start and Frame End Sync words are indicated in (b). CRC codes are also omitted from the figure.

For additional information on the synchronization codes, please refer to PYTHON Image Sensor Family Developer’s Guide AND9362/D.

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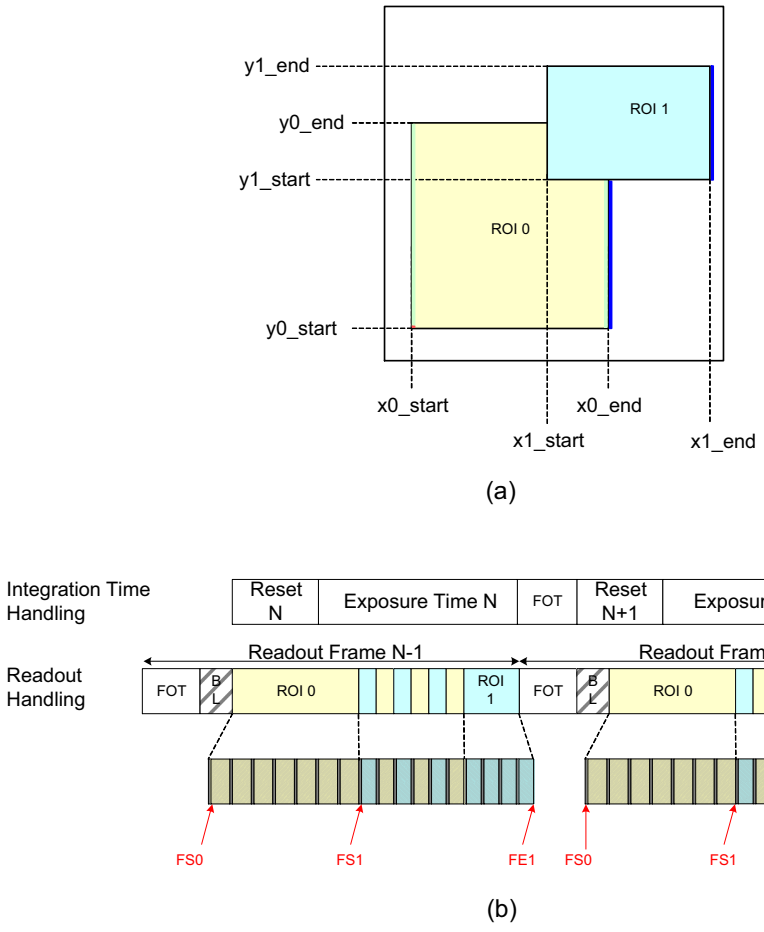

Figure 29. P1−SN/SE/FN, P3−SN/SE: Frame Sync Codes

Figure 30 shows the detail of a black line readout during global or full−frame readout.

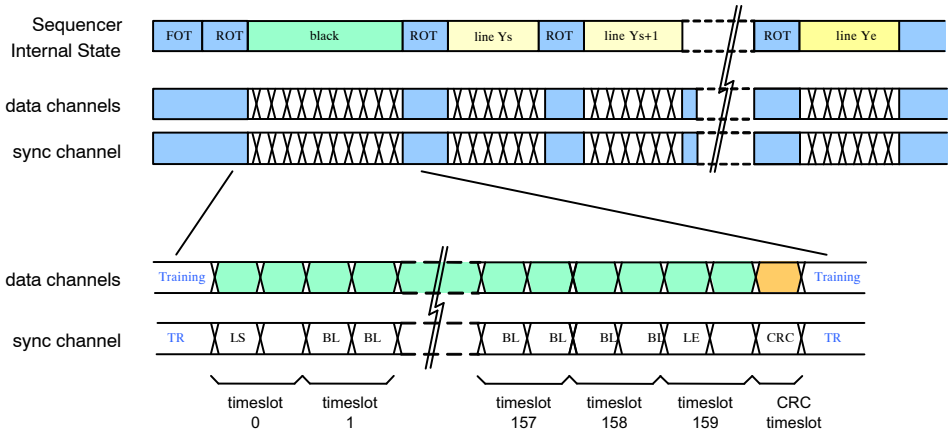

Figure 30. P1−SN/SE/FN, P3−SN/SE: Time Line for Black Line Readout

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Figure 31 shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.

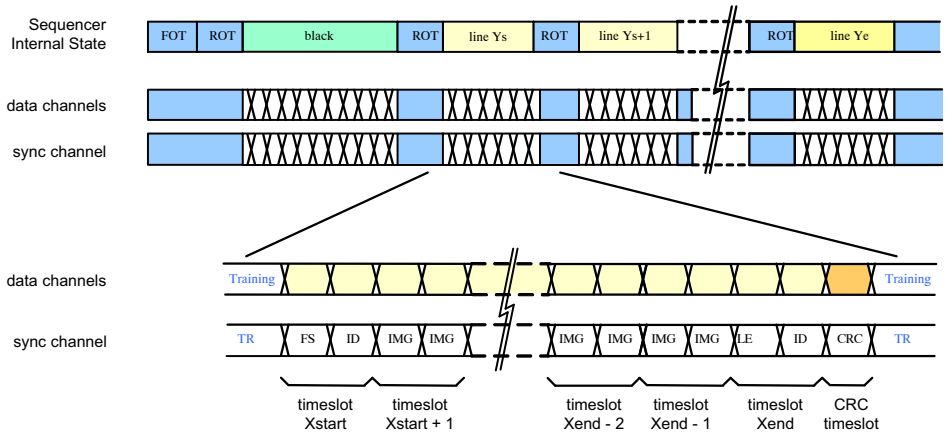

Figure 31. P1−SN/SE/FN, P3−SN/SE: Time Line for Single Window Readout (at the start of a frame)

Figure 32 shows the detail of the readout of a number of lines for readout of two overlapping windows.

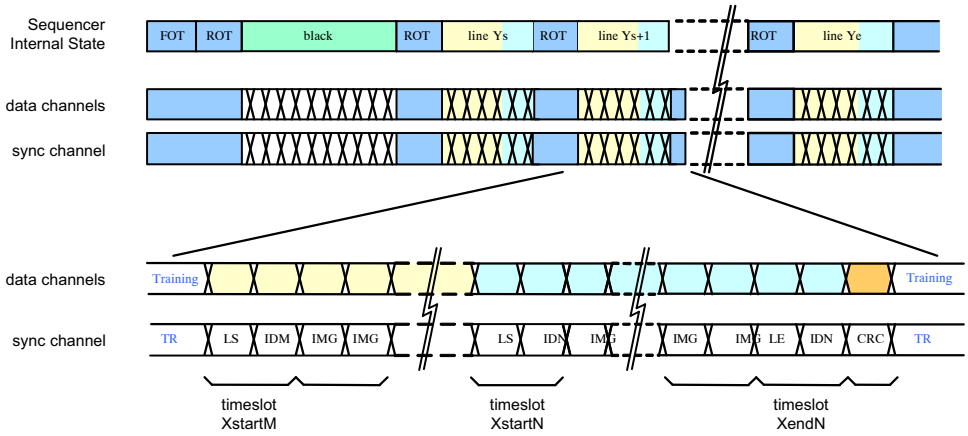

Figure 32. P1−SN/SE/FN, P3−SN/SE: Time Line Showing the Readout of Two Overlapping Windows

Frame Synchronization for 10−bit Mode

Table 21 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable) for 10−bit mode. If more than one window is active at the same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 21. FRAME SYNCHRONIZATION CODE DETAILS FOR 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:7	N/A	0x5	Frame start (FS) indication
9:7	N/A	0x6	Frame end (FE) indication
9:7	N/A	0x1	Line start (LS) indication
9:7	N/A	0x2	Line end (LE) indication
6:0	117[6:0]	0x2A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting

Window Identification

Frame synchronization codes are always followed by a 3−bit window identification (bits 2:0). This is an integer number, ranging from 0 to 7, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

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Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 22.

Table 22. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:0	118 [9:0]	0x015	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
9:0	119 [9:0]	0x035	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
9:0	125 [9:0]	0x059	CRC value. The data on the data output channels is the CRC code of the finished image data line.
9:0	126 [9:0]	0x3A6	Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Frame Synchronization in 8−bit Mode

The frame synchronization words are configured using the same registers as in 10−bit mode. The two least significant bits of these configuration registers are ignored and not sent out. Table 32 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8−bit mode.

Table 23. FRAME SYNCHRONIZATION CODE DETAILS FOR 8−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:5	N/A	0x5	Frame start (FS) indication
7:5	N/A	0x6	Frame end (FE) indication
7:5	N/A	0x1	Line start (LS) indication
7:5	N/A	0x2	Line end (LE) indication
4:0	117 [6:2]	0x0A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting.

Window Identification

Similar to 10−bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 5:2 (all other bit positions are ‘0’). The same restriction for overlapping windows applies in 8−bit mode.

Data Classification Codes

BL, IMG, CRC, and TR codes are defined by the same registers as in 10−bit mode. Bits 9:2 of the respective configuration registers are used as classification code with default values shown in Table 24.

Table 24. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 8−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:0	118 [9:2]	0x05	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
7:0	119 [9:2]	0x0D	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
7:0	125 [9:2]	0x16	CRC value. The data on the data output channels is the CRC code of the finished image data line.
7:0	126 [9:2]	0xE9	Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

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Training Patterns on Data Channels

In 10−bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable independent of the training code on the sync channel as shown in Table 25.

Table 25. TRAINING CODE ON SYNC CHANNEL IN 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
[9:0]	116 [9:0]	0x3A6	Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel.

In 8−bit mode, the training pattern for the data channels is defined by the same register as in 10−bit mode, where the lower two bits are omitted; see Table 26.

Table 26. TRAINING PATTERN ON DATA CHANNEL IN 8−BIT MODE

Data Word Bit Position	Register Address	Default Value	Description
[7:0]	116 [9:2]	0xE9	Data Channel Training Pattern (Training pattern).

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10−bit operation mode is $x^{10} + x^9 + x^6 + x^3 + x^2 + x + 1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the crc_seed register. When ‘0’, the CRC is seeded by all−‘0’; when ‘1’ it is seeded with all−‘1’.

In 8−bit mode, the polynomial is $x^8 + x^6 + x^3 + x^2 + 1$. The CRC seed is configured by means of the crc_seed register.

NOTE: The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

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Data Order for P1−SN/SE/FN, P3−SN/SE

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is sixteen pixels in x−direction by one pixel in y−direction. The data order in 8−bit mode is identical to the 10−bit mode.

Figure 33 indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner (front view on top of the package). The data order of this image data on the data output channels depends on the subsampling mode.

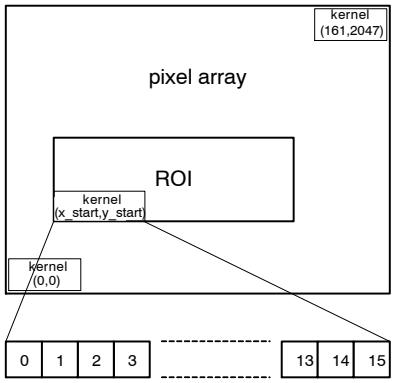

Figure 33. Kernel Organization in Pixel Array − Top View

- P1−SN/SE/FN, P3−SN/SE: Subsampling Disabled
  - 8 LVDS Output Channels (P1−SN/SE/FN only)

The image data is read out in kernels of 16 pixels in x−direction by one pixel in y−direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 34 shows how a kernel is read out over the eight output channels. For even positioned kernels, the kernels are read out ascending, while for odd positioned kernels the data order is reversed (descending).

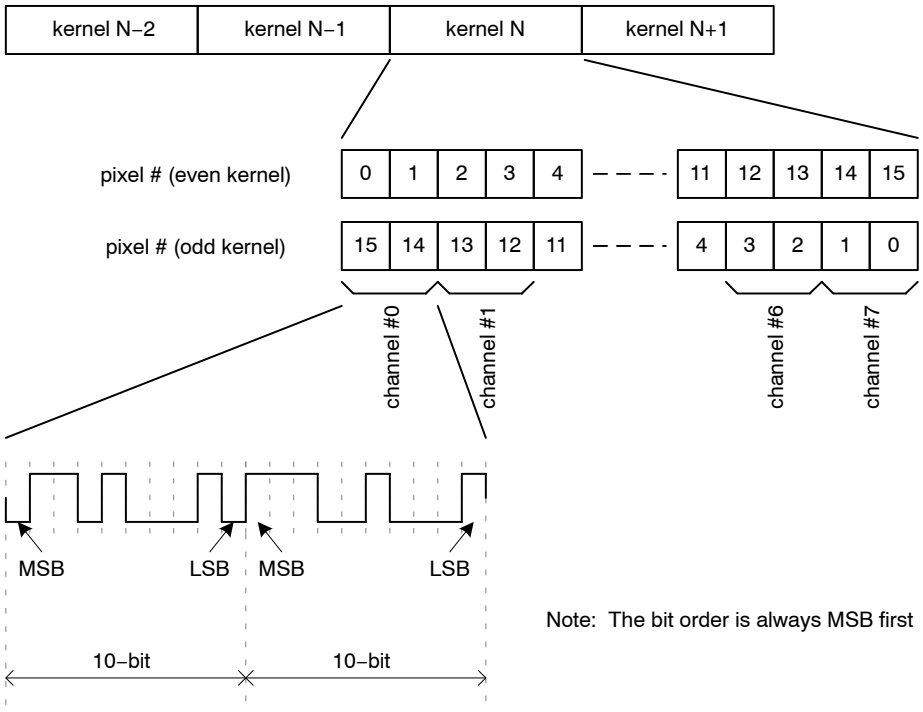

Figure 34. P1−SN/SE/FN: 8 LVDS Data Output Order when Subsampling is Disabled

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♦ 4 LVDS Output Channels

Figure 35 shows how a kernel is read out over the four output channels. For even positioned kernels, the kernels are read out ascending but in pair of even and odd pixels, while for odd positioned kernels, the data order is reversed (descending – in pair of even and odd pixels).

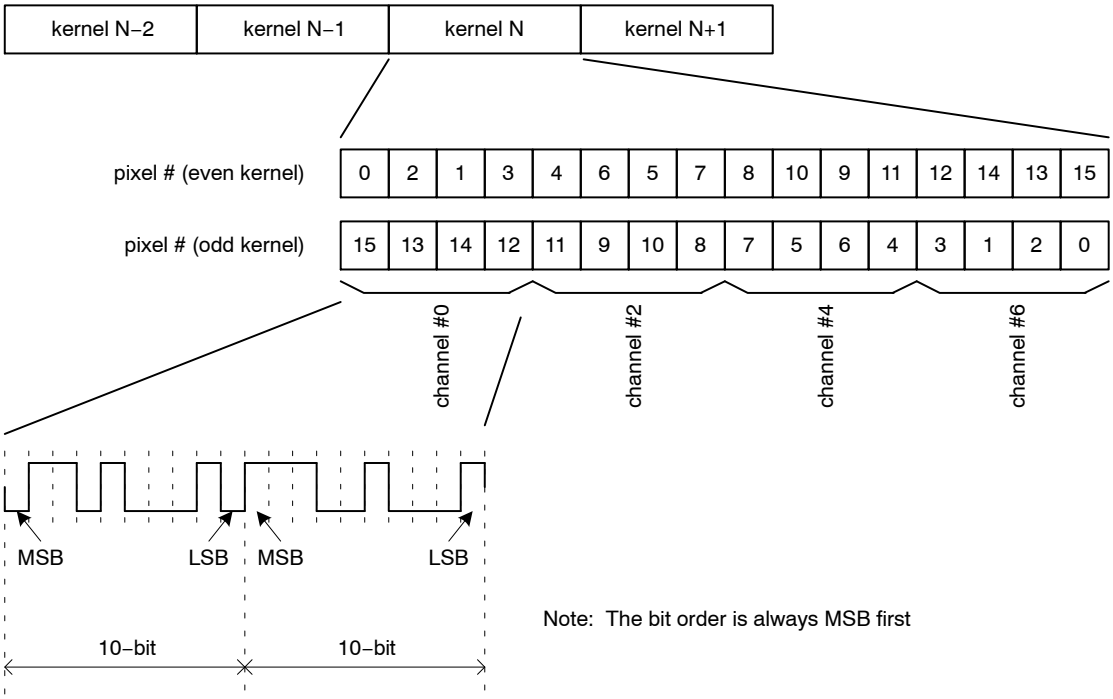

Figure 35. P1−SN/SE/FN, P3−SN/SE: 4 LVDS Data Output Order when Subsampling is Disabled

♦ 2 LVDS Output Channels

Figure 36 shows how a kernel is read out over 2 output channels. Each group of four adjacent channels is multiplexed on to one channel. For even positioned kernels, the kernels are read out in an ascending order but in sets of four even and four odd pixels, while for odd positioned kernels the data order is reversed (descending and in sets of four odd and four even pixels).

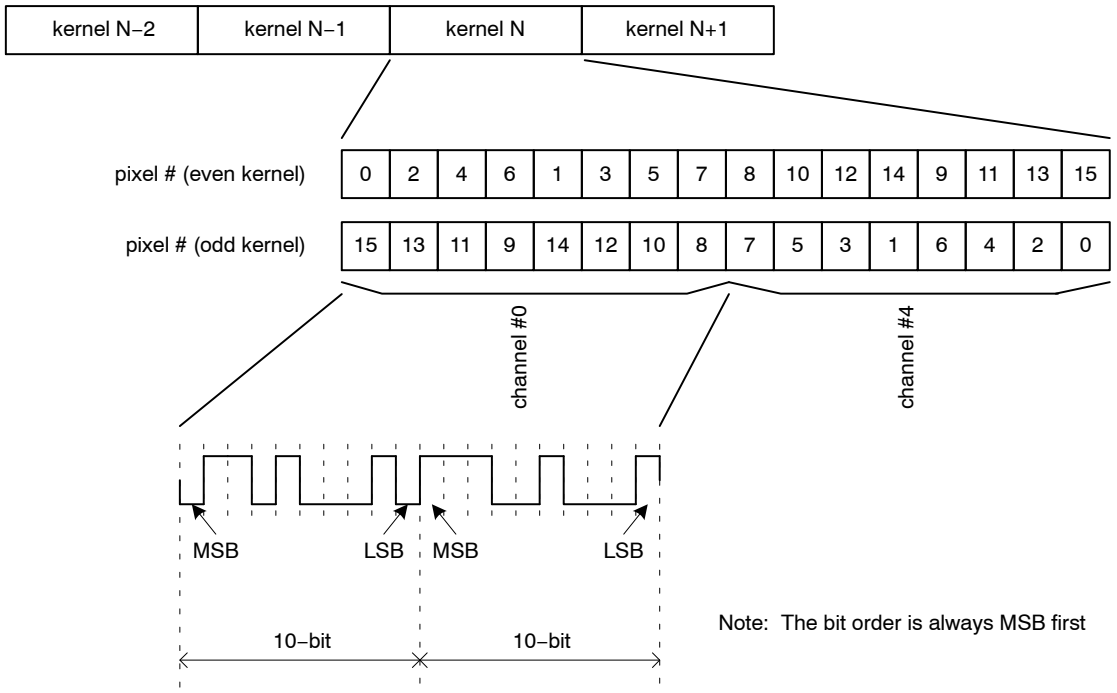

Figure 36. P1−SN/SE/FN, P3−SN/SE: 2 LVDS Data Output Order when Subsampling is Disabled

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♦ 1 LVDS Output Channel

Figure 37 shows how a kernel is read out over 1 output channel. Eight adjacent channels are multiplexed into one channel. For even positioned kernels, the kernels are read out ascending but in sets of 8 even and 8 odd pixels, while for odd positioned kernels the data order is reversed (descending – in sets of 8 odd and 8 even pixels).

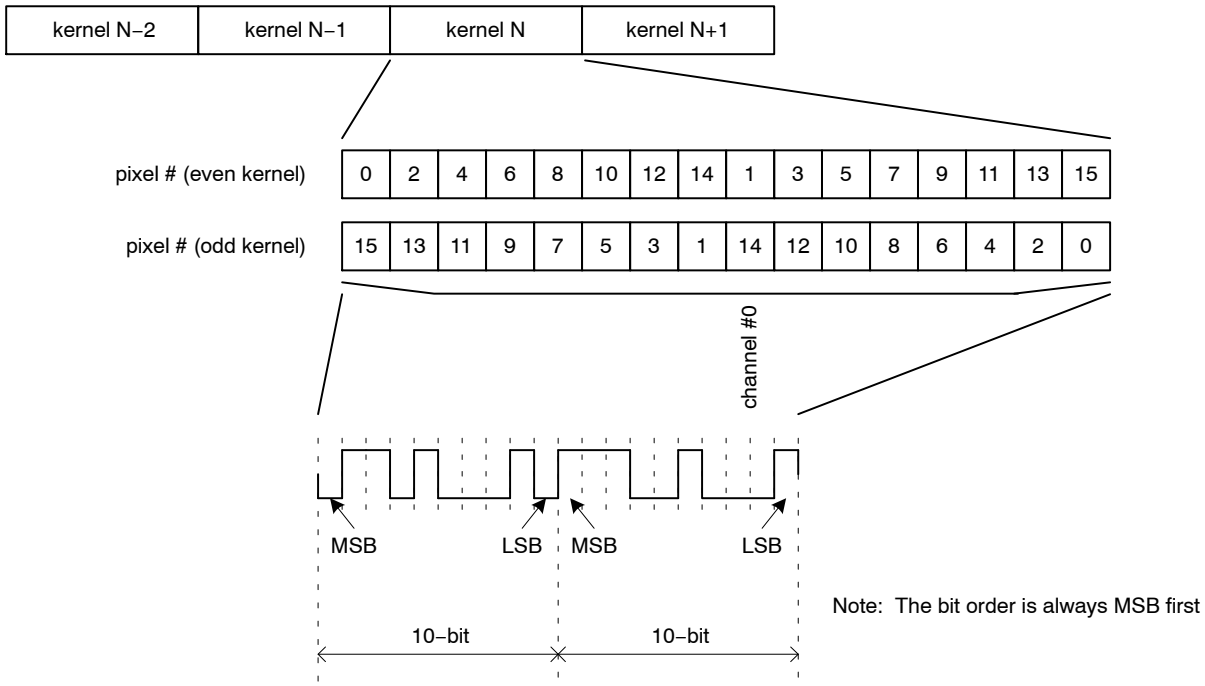

Figure 37. P1−SN/SE/FN, P3−SN/SE: 1 LVDS Data Output Order when Subsampling is Disabled

- P1−SN/FN, P3−SN: Subsampling on Monochrome Sensor

During subsampling on a monochrome sensor, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 32 pixels in the x−direction and one pixel in the y−direction. Only the pixels at the even pixel positions inside that kernel are read out.

♦ 8 LVDS Output Channels (P1−SN/FN only)

Figure 38 shows the data order for 8 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

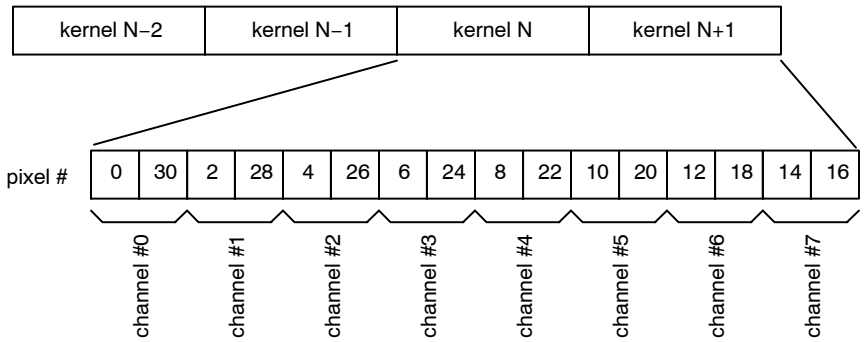

Figure 38. P1−SN/FN: Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

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♦ 4 LVDS Output Channels

Figure 39 shows the data order for 4 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

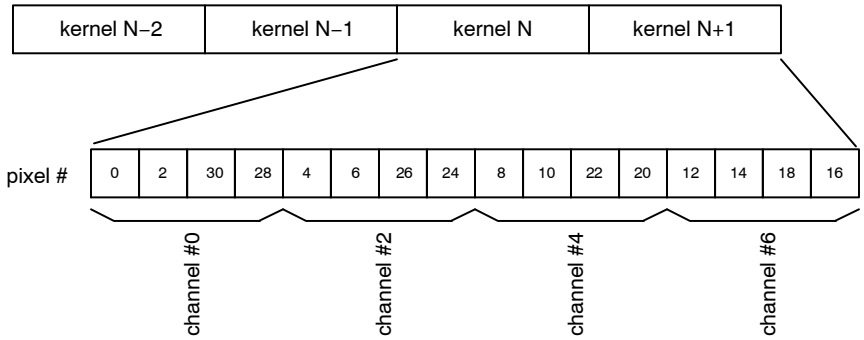

Figure 39. P1−SN/FN, P3−SN: Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

♦ 2 LVDS Output Channels

Figure 40 shows the data order for 2 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

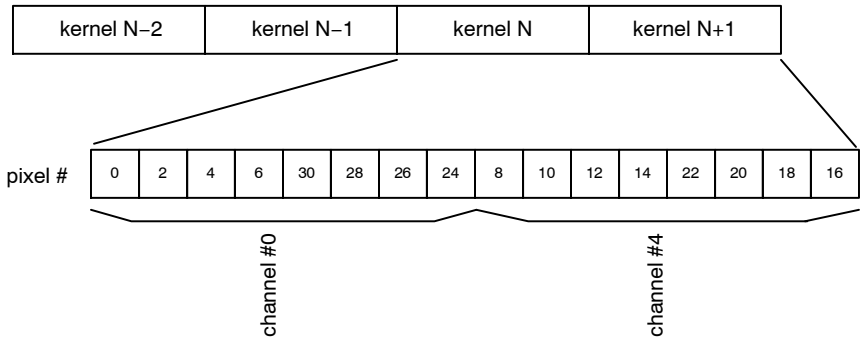

Figure 40. P1−SN/FN, P3−SN: Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

♦ 1 LVDS Output Channel

Figure 41 shows the data order for 1 LVDS output channel. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

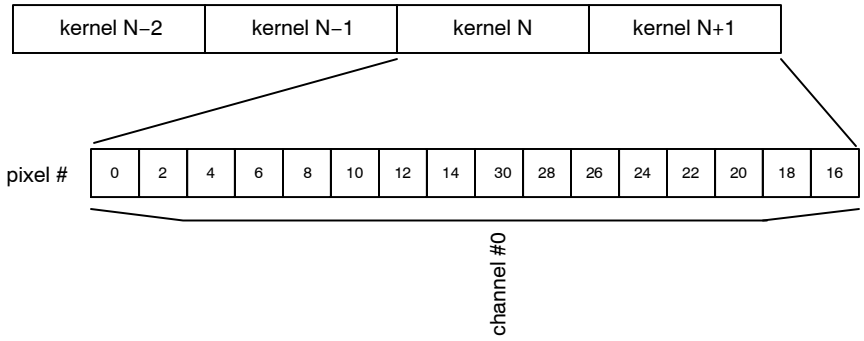

Figure 41. P1−SN/FN, P3−SN: Data Output Order for 1 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

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- P1−SE, P3−SE: Subsampling on Color Sensor

During subsampling on a color sensor, lines are read in a read-2-skip−2 manner. To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x−direction and one pixel in the y−direction. Only the pixels 0, 1, 4, 5, 8, 9, … 28, 29 are read out.

♦ 8 LVDS Output Channels (P1−SE only)

Figure 42 shows the data order for 8 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

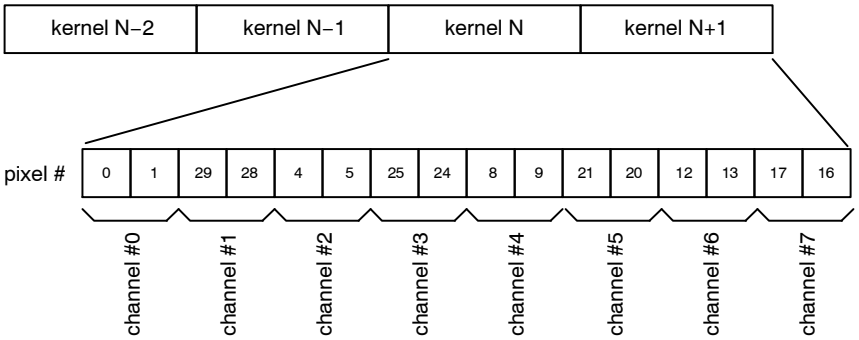

Figure 42. P1−SE: Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Color Sensor

♦ 4 LVDS Output Channels

Figure 43 shows the data order for 4 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

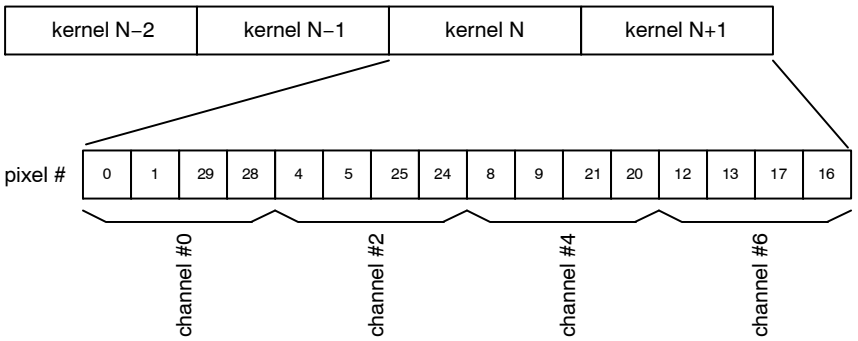

Figure 43. P1−SE, P3−SE: Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Color Sensor

♦ 2 LVDS Output Channels

Figure 44 shows the data order for 2 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

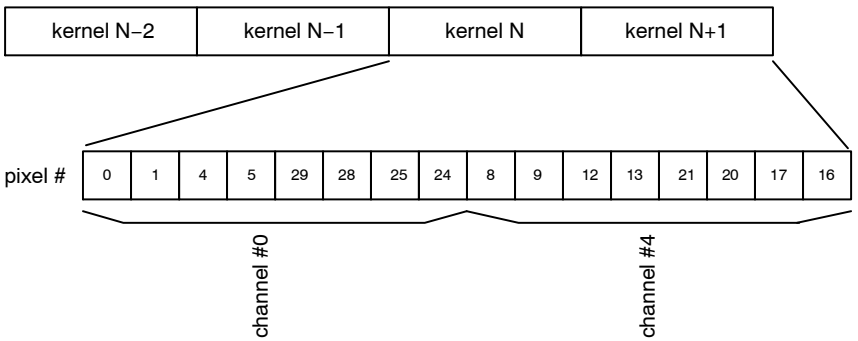

Figure 44. P1−SE, P3−SE: Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Color Sensor

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♦ 1 LVDS Output Channel

Figure 45 shows the data order for 1 LVDS output channel. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

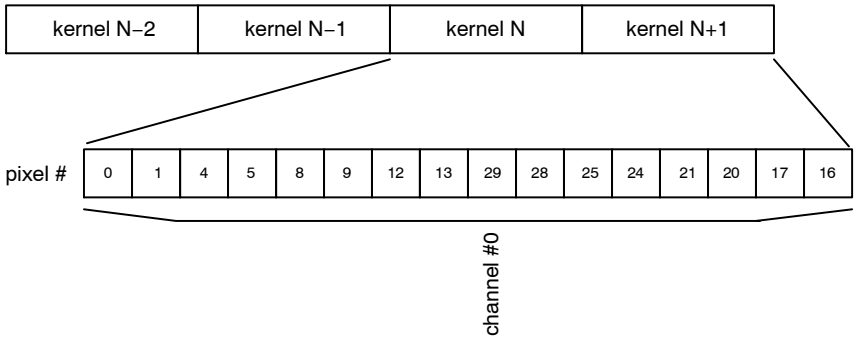

Figure 45. P1−SE, P3−SE: Data Output Order for 1 LVDS Output Channel in Subsampling Mode on a Color Sensor

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REGISTER MAP

The table below represents the register map for the NOIP1xx5000A part. Deviating default values for the NOIP1xx2000A sensor are mentioned between brackets (“[ ]”).

Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
Chip ID [Block Offset: 0]							
0	0		chip_id	0x5032	20530	Chip ID	Status
		[15:0]	id	0x5032	20530	Chip ID	
1	1		reserved	0x0001 [0x0101]	1 [257]	Reserved	Status
		[3:0]	reserved	0x1	1	Reserved	
		[9:8]	resolution	0x0 [0x1]	0 [1]	Sensor Resolution ‘0’: PYTHON 5000 ‘1’: PYTHON 2000	
		[11:10]	reserved	0x0	0	Reserved	
2	2		chip_configuration	0x0000	0	Chip General Configuration	RW
		[0]	color	0x0	0	Colour/Monochrome Configuration ‘0’: Monochrome ‘1’: Color	
		[3:2]	glob_config	0x0	0	Sensor pinout configuration	
		[15:4]	reserved	0x000	0	Reserved	
Reset Generator [Block Offset: 8]							
0	8		soft_reset_pll	0x0099	153	PLL Soft Reset Configuration	RW
		[3:0]	pll_soft_reset	0x9	9	PLL Reset 0x9: Soft Reset State others: Operational	
		[7:4]	pll_lock_soft_reset	0x9	9	PLL Lock Detect Reset 0x9: Soft Reset State others: Operational	
1	9		soft_reset_cgen	0x0009	9	Clock Generator Soft Reset	RW
		[3:0]	cgen_soft_reset	0x9	9	Clock Generator Reset 0x9: Soft Reset State others: Operational	
2	10		soft_reset_analog	0x0999	2457	Analog Block Soft Reset	RW
		[3:0]	mux_soft_reset	0x9	9	Column MUX Reset 0x9: Soft Reset State others: Operational	
		[7:4]	afe_soft_reset	0x9	9	AFE Reset 0x9: Soft Reset State others: Operational	
		[11:8]	ser_soft_reset	0x9	9	Serializer Reset 0x9: Soft Reset State others: Operational	
PLL [Block Offset: 16]							
0	16		power_down	0x0004	4	PLL Configuration	RW
		[0]	pwd_n	0x0	0	PLL Power Down ‘0’: Power Down, ‘1’: Operational	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[1]	enable	0x0	0	PLL Enable ‘0’: disabled, ‘1’: enabled	
		[2]	bypass	0x1	1	PLL Bypass ‘0’: PLL Active, ‘1’: PLL Bypassed	
1	17		reserved	0x2113	8467	Reserved	RW
		[7:0]	reserved	0x13	19	Reserved	
		[12:8]	reserved	0x1	1	Reserved	
		[14:13]	reserved	0x1	1	Reserved	
I/O [Block Offset: 20]							
0	20		config1	0x0000	0	IO Configuration	RW
		[0]	clock_in_pwd_n	0x0	0	Power down Clock Input	
		[9:8]	reserved	0x0	0	Reserved	
		[10]	reserved	0x0	0	Reserved	
PLL Lock Detector [Block Offset: 24]							
0	24		pll_lock	0x0000	0	PLL Lock Indication	Status
		[0]	lock	0x0	0	PLL Lock Indication	
2	26		reserved	0x2280	8832	Reserved	RW
		[7:0]	reserved	0x80	128	Reserved	
		[10:8]	reserved	0x2	2	Reserved	
		[14:12]	reserved	0x2	2	Reserved	
3	27		reserved	0x3D2D	15661	Reserved	RW
		[7:0]	reserved	0x2D	45	Reserved	
		[15:8]	reserved	0x3D	61	Reserved	
Clock Generator [Block Offset: 32]							
0	32		config0	0x0004	4	Clock Generator Configuration	RW
		[0]	enable_analog	0x0	0	Enable analogue clocks ‘0’: disabled, ‘1’: enabled	
		[1]	enable_log	0x0	0	Enable logic clock ‘0’: disabled, ‘1’: enabled	
		[2]	select_pll	0x1	1	Input Clock Selection ‘0’: Select LVDS clock input, ‘1’: Select PLL clock input	
		[3]	adc_mode	0x0	0	Set operation mode of CGEN block ‘0’: divide by 5 mode (10−bit mode), ‘1’: divide by 4 mode (8−bit mode)	
		[5:4]	mux	0x0	0	Multiplex Mode	
		[11:8]	reserved	0x0	0	Reserved	
		[14:12]	reserved	0x0	0	Reserved	
General Logic [Block Offset: 34]							
0	34		config0	0x0000	0	Clock Generator Configuration	RW

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[0]	enable	0x0	0	Logic General Enable Configuration '0': Disable '1': Enable	
0	38		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
1	39		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
Image Core [Block Offset: 40]							
0	40		image_core_config0	0x0000	0	Image Core Configuration	RW
		[0]	imc_pwd_n	0x0	0	Image Core Power Down '0': powered down, '1': powered up	
		[1]	mux_pwd_n	0x0	0	Column Multiplexer Power Down '0': powered down, '1': powered up	
		[2]	colbias_enable	0x0	0	Bias Enable '0': disabled '1': enabled	
1	41		image_core_config1	0x0B5A	2906	Image Core Configuration	RW
		[3:0]	dac_ds	0xA	10	Double Slope Reset Level	
		[7:4]	dac_ts	0x5	5	Triple Slope Reset Level	
		[10:8]	reserved	0x3	3	Reserved	
		[12:11]	reserved	0x1	1	Reserved	
		[13]	reserved	0x0	0	Reserved	
		[14]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	
2	42		reserved	0x0001	1	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x0	0	Reserved	
		[6:4]	reserved	0x0	0	Reserved	
		[10:8]	reserved	0x0	0	Reserved	
		[15:12]	reserved	0x0	0	Reserved	
3	43		reserved	0x0000	0	Reserved	RW
		[0]	reserved	0x0	0	Reserved	
		[1]	reserved	0x0	0	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[6:4]	reserved	0x0	0	Reserved	
		[7]	reserved	0x0	0	Reserved	
		[15:8]	reserved	0x0	0	Reserved	
AFE [Block Offset: 48]							
0	48		power_down	0x0000	0	AFE Configuration	RW

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[0]	pwd_n	0x0	0	Power down for AFE's '0': powered down, '1': powered up	
Bias [Block Offset: 64]							
0	64		power_down	0x0000	0	Bias Power Down Configuration	RW
		[0]	pwd_n	0x0	0	Power down bandgap '0': powered down, '1': powered up	
1	65		configuration	0x888B	34955	Bias Configuration	RW
		[0]	extres	0x1	1	External Resistor Selection '0': internal resistor, '1': external resistor	
		[3:1]	reserved	0x5	5	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
2	66		reserved	0x53C8	21448	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0xC	12	Reserved	
		[14:8]	reserved	0x53	83	Reserved	
3	67		reserved	0x8888	34952	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
4	68		lvds_bias	0x0088	136	LVDS Bias Configuration	RW
		[3:0]	lvds_ibias	0x8	8	LVDS Ibias	
		[7:4]	lvds_iref	0x8	8	LVDS Iref	
5	69		reserved	0x0888	2184	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
6	70		reserved	0x8888	34952	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
7	71		reserved	0x8888	34952	Reserved	RW
		[15:0]	reserved	0x8888	34952	Reserved	
Charge Pump [Block Offset: 72]							
0	72		configuration	0x2220	8736	Charge Pump Configuration	RW
		[0]	trans_pwd_n	0x0	0	PD Trans Charge Pump Enable '0': disabled, '1': enabled	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[1]	resfd_calib_pwd_n	0x0	0	FD Charge Pump Enable '0': disabled, '1': enabled	
		[2]	sel_sample_pwd_n	0x0	0	Select/Sample Charge Pump Enable '0': disabled '1': enabled	
		[6:4]	reserved	0x2	2	Reserved	
		[10:8]	reserved	0x2	2	Reserved	
		[14:12]	reserved	0x2	2	Reserved	
Charge Pump [Block Offset: 80]							
0	80		reserved	0x0000	0	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[3:2]	reserved	0x0	0	Reserved	
		[5:4]	reserved	0x0	0	Reserved	
		[7:6]	reserved	0x0	0	Reserved	
		[9:8]	reserved	0x0	0	Reserved	
1	81		reserved	0x8881	34945	Reserved	RW
		[15:0]	reserved	0x8881	34945	Reserved	
Temperature Sensor [Block Offset: 96]							
0	96		enable	0x0000	0	Temperature Sensor Configuration	RW
		[0]	enable	0x0	0	Temperature Diode Enable '0': disabled, '1': enabled	
		[1]	reserved	0x0	0	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[4]	reserved	0x0	0	Reserved	
		[5]	reserved	0x0	0	Reserved	
		[13:8]	offset	0x0	0	Temperature Offset (signed)	
1	97		temp	0x0000	0	Temperature Sensor Status	Status
		[7:0]	temp	0x00	0	Temperature Readout	
Temperature Sensor [Block Offset: 104]							
0	104		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0	0	Reserved	
1	105		reserved	0x0000	0	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[6:2]	reserved	0x0	0	Reserved	
		[7]	reserved	0x0	0	Reserved	
		[9:8]	reserved	0x0	0	Reserved	
		[14:10]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	
2	106		reserved	0x0000	0	Reserved	Status

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15:0]	reserved	0x0000	0	Reserved	
3	107		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
4	108		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
5	109		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
6	110		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
7	111		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
Serializers / LVDS / IO [Block Offset: 112]							
0	112		power_down	0x0000	0	LVDS Power Down Configuration	RW
		[0]	clock_out_pwd_n	0x0	0	Power down for Clock Output. ‘0’: powered down, ‘1’: powered up	
		[1]	sync_pwd_n	0x0	0	Power down for Sync channel ‘0’: powered down, ‘1’: powered up	
		[2]	data_pwd_n	0x0	0	Power down for data channels (4 channels) ‘0’: powered down, ‘1’: powered up	
Sync Words [Block Offset: 116]							
4	116		trainingpattern	0x03A6	934	Data Formating – Training Pattern	RW
		[9:0]	trainingpattern	0x3A6	934	Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels.	
5	117		sync_code0	0x002A	42	LVDS Power Down Configuration	RW
		[6:0]	frame_sync_0	0x02A	42	Frame Sync Code LSBs – Even kernels	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
6	118		sync_code1	0x0015	21	Data Formating – BL Indication	RW
		[9:0]	bl_0	0x015	21	Black Pixel Identification Sync Code – Even kernels	
7	119		sync_code2	0x0035	53	Data Formating – IMG Indication	RW
		[9:0]	img_0	0x035	53	Valid Pixel Identification Sync Code – Even kernels	
8	120		sync_code3	0x0025	37	Data Formating – IMG Indication	RW
		[9:0]	ref_0	0x025	37	Reference Pixel Identification Sync Code – Even kernels	
9	121		sync_code4	0x002A	42	LVDS Power Down Configuration	RW
		[6:0]	frame_sync_1	0x02A	42	Frame Sync Code LSBs – Odd kernels	
10	122		sync_code5	0x0015	21	Data Formating – BL Indication	RW
		[9:0]	bl_1	0x015	21	Black Pixel Identification Sync Code – Odd kernels	
11	123		sync_code6	0x0035	53	Data Formating – IMG Indication	RW
		[9:0]	img_1	0x035	53	Valid Pixel Identification Sync Code – Odd kernels	
12	124		sync_code7	0x0025	37	Data Formating – IMG Indication	RW
		[9:0]	ref_1	0x025	37	Reference Pixel Identification Sync Code – Odd kernels	
13	125		sync_code8	0x0059	89	Data Formating – CRC Indication	RW
		[9:0]	crc	0x059	89	CRC Value Identification Sync Code	
14	126		sync_code9	0x03A6	934	Data Formating – TR Indication	RW
		[9:0]	tr	0x3A6	934	Training Value Identification Sync Code	
15	127		reserved	0x02AA	682	Reserved	RW
		[9:0]	reserved	0x2AA	682	Reserved	
Data Block [Block Offset: 128]							
0	128		blackcal	0x4008	16392	Black Calibration Configuration	RW
		[7:0]	black_offset	0x08	8	Desired black level at output	
		[10:8]	black_samples	0x0	0	Black pixels taken into account for black calibration. Total samples = 2**black_samples	
		[14:11]	reserved	0x8	8	Reserved	
		[15]	crc_seed	0x0	0	CRC Seed '0': All−0 '1': All−1	
1	129		general_configuration	0x0001	1	Black Calibration and Data Formating Configuration	RW
		[0]	auto_blackcal_enable	0x1	1	Automatic blackcalibration is enabled when 1, bypassed when 0	
		[9:1]	blackcal_offset	0x00	0	Black Calibration offset used when auto_black_cal_en = '0'.	
		[10]	blackcal_offset_dec	0x0	0	blackcal_offset is added when 0, subtracted when 1	
		[11]	reserved	0x0	0	Reserved	
		[12]	reserved	0x0	0	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[13]	8bit_mode	0x0	0	Shifts window ID indications by 4 cycles. '0': 10 bit mode, '1': 8 bit mode	
		[14]	ref_mode	0x0	0	Data contained on reference lines: '0': reference pixels '1': black average for the corresponding data channel	
		[15]	ref_bcal_enable	0x0	0	Enable black calibration on reference lines '0': Disabled '1': Enabled	
2	130		reserved	0x000F	15	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x1	1	Reserved	
		[2]	reserved	0x1	1	Reserved	
		[3]	reserved	0x1	1	Reserved	
		[4]	reserved	0x0	0	Reserved	
		[8]	reserved	0x0	0	Reserved	
8	136		blackcal_error0	0x0000	0	Black Calibration Status	Status
		[15:0]	blackcal_error[15:0]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0−16	
9	137		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
10	138		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
11	139		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
12	140		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
13	141		reserved	0xFFFF	65535	Reserved	RW
		[15:0]	reserved	0xFFFF	65535	Reserved	
16	144		test_configuration	0x0000	0	Data Formating Test Configuration	RW
		[0]	testpattern_en	0x0	0	Insert synthesized testpattern when '1'	
		[1]	inc_testpattern	0x0	0	Incrementing testpattern when '1', constant testpattern when '0'	
		[2]	prbs_en	0x0	0	Insert PRBS when '1'	
		[3]	frame_testpattern	0x0	0	Frame test patterns when '1', unframed testpatterns when '0'	
		[4]	reserved	0x0	0	Reserved	
17	145		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved		0	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
18	146		test_configuration0	0x0100	256	Data Formating Test Configuration	RW
		[7:0]	testpattern0_lsb	0x00	0	Testpattern used on datapath #0 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern1_lsb	0x01	1	Testpattern used on datapath #1 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
19	147		test_configuration1	0x0302	770	Data Formating Test Configuration	RW
		[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
20	148		test_configuration2	0x0504	1284	Data Formating Test Configuration	RW
		[7:0]	testpattern4_lsb	0x04	4	Testpattern used on datapath #4 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern5_lsb	0x05	5	Testpattern used on datapath #5 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
21	149		test_configuration3	0x0706	1798	Data Formating Test Configuration	RW
		[7:0]	testpattern6_lsb	0x06	6	Testpattern used on datapath #6 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern7_lsb	0x07	7	Testpattern used on datapath #7 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
22	150		test_configuration16	0x0000	0	Data Formating Test Configuration	RW
		[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[9:8]	testpattern4_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[11:10]	testpattern5_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[13:12]	testpattern6_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[15:14]	testpattern7_msb	0x0	0	Testpattern used when testpattern_en = '1'	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
26	154		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
27	155		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
AEC [Block Offset: 160]							
0	160		configuration	0x0010	16	AEC Configuration	RW
		[0]	enable	0x0	0	AEC Enable	
		[1]	restart_filter	0x0	0	Restart AEC filter	
		[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains	
		[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1	
		[4]	amp_pri	0x1	1	Column amplifier gets higher priority than AFE PGA in gain distribution if 1. Vice versa if 0	
1	161		intensity	0x60B8	24760	AEC Configuration	RW
		[9:0]	desired_intensity	0xB8	184	Target average intensity	
		[15:10]	reserved	0x018	24	Reserved	
2	162		red_scale_factor	0x0080	128	Red Scale Factor	RW
		[9:0]	red_scale_factor	0x80	128	Red Scale Factor 3.7 unsigned	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
3	163		green1_scale_factor	0x0080	128	Green1 Scale Factor	RW
		[9:0]	green1_scale_factor	0x80	128	Green1 Scale Factor 3.7 unsigned	
4	164		green2_scale_factor	0x0080	128	Green2 Scale Factor	RW
		[9:0]	green2_scale_factor	0x80	128	Green2 Scale Factor 3.7 unsigned	
5	165		blue_scale_factor	0x0080	128	Blue Scale Factor	RW
		[9:0]	blue_scale_factor	0x80	128	Blue Scale Factor 3.7 unsigned	
6	166		reserved	0x03FF	1023	Reserved	RW
		[15:0]	reserved	0x03FF	1023	Reserved	
7	167		reserved	0x0800	2048	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[3:2]	reserved	0x0	0	Reserved	
		[15:4]	reserved	0x080	128	Reserved	
8	168		min_exposure	0x0001	1	Minimum Exposure Time	RW
		[15:0]	min_exposure	0x0001	1	Minimum Exposure Time	
9	169		min_gain	0x0800	2048	Minimum Gain	RW
		[1:0]	min_mux_gain	0x0	0	Minimum Column Amplifier Gain	
		[3:2]	min_afe_gain	0x0	0	Minimum AFE PGA Gain	
		[15:4]	min_digital_gain	0x080	128	Minimum Digital Gain 5.7 unsigned	
10	170		max_exposure	0x03FF	1023	Maximum Exposure Time	RW
		[15:0]	max_exposure	0x03FF	1023	Maximum Exposure Time	
11	171		max_gain	0x100D	4109	Maximum Gain	RW
		[1:0]	max_mux_gain	0x1	1	Maximum Column Amplifier Gain	
		[3:2]	max_afe_gain	0x3	3	Maximum AFE PGA Gain	
		[15:4]	max_digital_gain	0x100	256	Maximum Digital Gain 5.7 unsigned	
12	172		reserved	0x0083	131	Reserved	RW
		[7:0]	reserved	0x083	131	Reserved	
		[13:8]	reserved	0x00	0	Reserved	
		[15:14]	reserved	0x0	0	Reserved	
13	173		reserved	0x2824	10276	Reserved	RW
		[7:0]	reserved	0x024	36	Reserved	
		[15:8]	reserved	0x028	40	Reserved	
14	174		reserved	0x2A96	10902	Reserved	RW
		[3:0]	reserved	0x6	6	Reserved	
		[7:4]	reserved	0x9	9	Reserved	
		[11:8]	reserved	0xA	10	Reserved	
		[15:12]	reserved	0x2	2	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
15	175		reserved	0x0080	128	Reserved	RW
		[9:0]	reserved	0x080	128	Reserved	
16	176		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
17	177		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	
18	178		reserved	0x0080	128	Reserved	RW
		[9:0]	reserved	0x080	128	Reserved	
19	179		reserved	0x00AA	170	Reserved	RW
		[9:0]	reserved	0x0AA	170	Reserved	
20	180		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	
21	181		reserved	0x0155	341	Reserved	RW
		[9:0]	reserved	0x155	341	Reserved	
24	184		total_pixels0	0x0000	0	AEC Status	Status
		[15:0]	total_pixels[15:0]	0x0000	0	Total number of pixels sampled for Average, LSB	
25	185		total_pixels1	0x0000	0	AEC Status	Status
		[7:0]	total_pixels[23:16]	0x0	0	Total number of pixels sampled for Average, MSB	
26	186		average_status	0x0000	0	ASE Status	Status
		[9:0]	average	0x000	0	AEC Average Status	
		[12]	avg_locked	0x0	0	AEC Average Lock Status	
27	187		exposure_status	0x0000	0	ASE Status	Status
		[15:0]	exposure	0x0000	0	AEC Expsosure Status	
28	188		gain_status	0x0000	0	ASE Status	Status
		[1:0]	mux_gain	0x0	0	AEC MUX Gain Status	
		[3:2]	afe_gain	0x0	0	AEC AFE Gain Status	
		[15:4]	digital_gain	0x000	0	AEC Digital Gain Status 5.7 unsigned	
29	189		reserved	0x0000	0	Reserved	Status
		[12:0]	reserved	0x000	0	Reserved	
		[13]	reserved	0x0	0	Reserved	

Sequencer [Block Offset: 192]

0	192		general_configuration	0x0000	0	Sequencer General Cofniguration	RW
		[0]	enable	0x0	0	Enable sequencer ‘0’: Idle, ‘1’: enabled	
		[1]	reserved	0x0	0	Reserved	
		[2]	zero_rot_enable	0x0	0	Zero ROT mode Selection. ‘0’: Non−Zero ROT, ‘1’: Zero ROT’	
		[3]	reserved	0x0	0	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[4]	triggered_mode	0x0	0	Triggered Mode Selection (Snapshot Shutter only) '0': Normal Mode, '1': Triggered Mode	
		[5]	slave_mode	0x0	0	Master/Slave Selection (Snapshot Shutter only) '0': master, '1': slave	
		[6]	nzrot_xsm_delay_enable	0x0	0	Insert delay between end of ROT and start of readout in Non−Zero ROT readout mode if '1'. ROT delay is defined by register xsm_delay	
		[7]	subsampling	0x0	0	Subsampling mode selection '0': no subsampling, '1': subsampling	
		[8]	reserved	0x0	0	Reserved	
		[10]	roi_aec_enable	0x0	0	Enable windowing for AEC Statistics. '0': Subsample all windows '1': Subsample configured window	
		[13:11]	monitor_select	0x0	0	Control of the monitor pins	
		[14]	reserved	0x0	0	Reserved	
		[15]	sequence	0x0	0	Enable a sequenced readout with different parameters for even and odd frames.	
1	193		delay_configuration	0x0000	0	Sequencer delay configuration	RW
		[7:0]	reserved	0x00	0	Reserved	
		[15:8]	xsm_delay	0x00	0	Delay between ROT end and X−readout (Non−Zero ROT and Zero ROT mode) Delay between ROT end and X−readout (Normal ROT mode with nzrot_xsm_delay_enable = '1')	
2	194		integration_control	0x00E4	228	Integration Control	RW
		[0]	dual_slope_enable	0x0	0	Enable Dual Slope	
		[1]	triple_slope_enable	0x0	0	Enable Triple Slope	
		[2]	fr_mode	0x1	1	Representation of fr_length. '0': reset length '1': frame length	
		[3]	reserved	0x0	0	Reserved	
		[4]	int_priority	0x0	0	Integration Priority '0': Frame readout has priority over integration '1': Integration End has priority over frame readout	
		[5]	halt_mode	0x1	1	The current frame will be completed when the sequencer is disabled and halt_mode = '1'. When '0', the sensor stops immediately when disabled, without finishing the current frame.	
		[6]	fss_enable	0x1	1	Generation of Frame Sequence Start Sync code (FSS) '0': No generation of FSS '1': Generation of FSS	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[7]	fse_enable	0x1	1	Generation of Frame Sequence End Sync code (FSE) '0': No generation of FSE '1': Generation of FSE	
		[8]	reverse_y	0x0	0	Reverse readout '0': bottom to top readout '1': top to bottom readout	
		[9]	reserved	0x0	0	Reserved	
		[11:10]	subsampling_mode	0x0	0	Subsampling mode 0x0: Subsampling in x and y (VITA compatible) 0x1: Subsampling in x, not y 0x2: Subsampling in y, not x 0x3: Subsampling in x an y	
		[13:12]	reserved	0x0	0	Reserved	
		[14]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
3	195		roi_active0_0	0x0001	1	Active ROI Selection	RW
		[15:0]	roi_active0	0x01	1	Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active	
4	196		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
5	197		black_lines	0x0102	258	Black Line Configuration	RW
		[7:0]	black_lines	0x02	2	Number of black lines. Minimum is 1. Range 1−255	
		[12:8]	gate_first_line	0x1	1	Blank out first lines 0: no blank 1−31: blank 1−31 lines	
6	198		reserved	0x0000	0	Reserved	RW
		[11:0]	reserved	0x000	0	Reserved	
7	199		mult_timer0	0x0001	1	Exposure/Frame Rate Configuration	RW
		[15:0]	mult_timer0	0x0001	1	Mult Timer Defines granularity (unit = 1/PLL clock) of exposure and reset_length	
8	200		fr_length0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	fr_length0	0x0000	0	Frame/Reset length Reset length when fr_mode = ‘0’, Frame Length when fr_mode = ‘1’ Granularity defined by mult_timer	
9	201		exposure0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure0	0x0000	0	Exposure Time Granularity defined by mult_timer	
10	202		exposure_ds0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure_ds0	0x0000	0	Exposure Time (Dual Slope) Granularity defined by mult_timer	
11	203		exposure_ts0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure_ts0	0x0000	0	Exposure Time (Triple Slope) Granularity defined by mult_timer	
12	204		gain_configuration0	0x01E3	483	Gain Configuration	RW
		[4:0]	mux_gainsw0	0x03	3	Column Gain Setting	
		[12:5]	afe_gain0	0xF	15	AFE Programmable Gain Setting	
		[13]	gain_lat_comp	0x0	0	Postpone gain update by 1 frame when ‘1’ to compensate for exposure time updates latency. Gain is applied at start of next frame if ‘0’	
13	205		digital_gain_configuration0	0x0080	128	Gain Configuration	RW
		[11:0]	db_gain0	0x080	128	Digital Gain	
14	206		sync_configuration	0x037F	895	Synchronization Configuration	RW

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[0]	sync_rs_x_length	0x1	1	Update of rs_x_length will not be sync'ed at start of frame when '0'	
		[1]	sync_black_lines	0x1	1	Update of black_lines will not be sync'ed at start of frame when '0'	
		[2]	sync_dummy_lines	0x1	1	Update of dummy_lines will not be sync'ed at start of frame when '0'	
		[3]	sync_exposure	0x1	1	Update of exposure will not be sync'ed at start of frame when '0'	
		[4]	sync_gain	0x1	1	Update of gain settings (gain_sw, afe_gain) will not be sync'ed at start of frame when '0'	
		[5]	sync_roi	0x1	1	Update of roi updates (active_roi) will not be sync'ed at start of frame when '0'	
		[6]	sync_ref_lines	0x1	1	Update of ref_lines will not be sync'ed at start of frame when '0'	
		[8]	blank_roi_switch	0x1	1	Blank first frame after ROI switching	
		[9]	blank_subsampling_ss	0x1	1	Blank first frame after subsampling mode switching '0': No blanking '1': Blanking	
		[10]	exposure_sync_mode	0x0	0	When '0', exposure configurations are sync'ed at the start of FOT. When '1', exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered snapshot – master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'.	
15	207		ref_lines	0x0000	0	Reference Line Configuration	RW
		[7:0]	ref_lines	0x00	0	Number of Reference Lines 0–255	
36	228		roi_active0_1	0x0001	1	Active ROI Selection	RW
		[7:0]	roi_active1	0x01	1	Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active	
48	240		x_resolution	0x00A2 [0x007C]	162 [124]	Sequencer Status	Status
		[7:0]	x_resolution	0x000A2 [0x007C]	162 [124]	Sensor x resolution	
49	241		y_resolution	0x0800 [0x04F0]	2048 [1264]	Sequencer Status	Status
		[12:0]	y_resolution	0x0800 [0x04F0]	2048 [1264]	Sensor y resolution	
50	242		mult_timer_status	0x0000	0	Sequencer Status	Status
		[15:0]	mult_timer	0x0000	0	Mult Timer Status (Master Snapshot Shutter only)	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
51	243		reset_length_status	0x0000	0	Sequencer Status	Status
		[15:0]	reset_length	0x0000	0	Current Reset Length (not in Slave mode)	
52	244		exposure_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure	0x0000	0	Current Exposure Time (not in Slave mode)	
53	245		exposure_ds_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure_ds	0x0000	0	Current Exposure Time (not in Slave mode)	
54	246		exposure_ts_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure_ts	0x0000	0	Current Exposure Time (not in Slave mode)	
55	247		gain_status	0x0000	0	Sequencer Status	Status
		[4:0]	mux_gainsw	0x00	0	Current Column Gain Setting	
		[12:5]	afe_gain	0x00	0	Current AFE Programmable Gain	
56	248		digital_gain_status	0x0000	0	Sequencer Status	Status
		[11:0]	db_gain	0x000	0	Digital Gain	
		[12]	dual_slope	0x0	0	Dual Slope Enabled	
		[13]	triple_slope	0x0	0	Triple Slope Enabled	
61	253		roi_aec_configuration0	0x0000	0	AEC ROI Configuration	RW
		[7:0]	x_start	0x00	0	AEC ROI X Start Configuration (used for AEC statistics when roi_aec_enable='1')	
		[15:8]	x_end	0x00	0	AEC ROI X End Configuration (used for AEC statistics when roi_aec_enable='1')	
62	254		roi_aec_configuration1	0x0000	0	AEC ROI Configuration	RW
		[12:0]	y_start	0x0000	0	AEC ROI Y Start Configuration (used for AEC statistics when roi_aec_enable='1')	
63	255		roi_aec_configuration2	0x0000	0	AEC ROI Configuration	RW
		[12:0]	y_end	0x0000	0	AEC ROI Y End Configuration (used for AEC statistics when roi_aec_enable='1')	
Sequencer ROI [Block Offset: 256]							
0	256		roi0_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
1	257		roi0_configuration1	0x0000	0	ROI Configuration	RW

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[12:0]	y_start	0x0000	0	Y Start Configuration	
2	258		roi0_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
3	259		roi1_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
4	260		roi1_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
5	261		roi1_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
6	262		roi2_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
7	263		roi2_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
8	264		roi2_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
9	265		roi3_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
10	266		roi3_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
11	267		roi3_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
12	268		roi4_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
13	269		roi4_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
14	270		roi4_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
15	271		roi5_configuration0	0xA100	41216	ROI Configuration	RW

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
16	272		roi5_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
17	273		roi5_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
18	274		roi6_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
19	275		roi6_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
20	276		roi6_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
21	277		roi7_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
22	278		roi7_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
23	279		roi7_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
24	280		roi8_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
25	281		roi8_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
26	282		roi8_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
27	283		roi9_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
28	284		roi9_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
29	285		roi9_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
30	286		roi10_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
31	287		roi10_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
32	288		roi10_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
33	289		roi11_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
34	290		roi11_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
35	291		roi11_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
36	292		roi12_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
37	293		roi12_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
38	294		roi12_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
39	295		roi13_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
40	296		roi13_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
41	297		roi13_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
42	298		roi14_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
43	299		roi14_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
44	300		roi14_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
45	301		roi15_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	

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Table 27. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15:8]	x_end	0xA1	161	X End Configuration	
46	302		roi15_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
47	303		roi15_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	

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Selectable Pin−Out

The PYTHON sensor has a built−in possibility to route some of the internal signals to different pads at the side of the chip.

The pin−out is controlled by glob_config in the chip_configuration register, located at address 2. The two possible pin outs in the 84 pin package are listed in Table 28. By default, 0x3 setting is selected.

Table 28. ALTERNATIVE PIN OUT OPTIONS

glob_config = 0x3	glob_config = 0x1	84−pin LCC	128−pad LGA
doutn1	clock_outn	8	D4
doutp1	clock_outp	9	D5
clock_outn	doutn1	14	G4
clock_outp	doutp1	15	G5
syncn	doutn6	29	H4
syncp	doutp6	30	H5
doutn6	syncn	35	L4
doutp6	syncp	36	L5

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Pin List

The PYTHON 2000 and PYTHON 5000 image sensors are available in LVDS output configuration (P1−SN/SE/FN, P3−SN/SE). The LVDS I/Os comply to the TIA/EIA−644−A Standard and the CMOS I/Os have 3.3 V signal level. Table 29 and Table 30 show the pin list for the LCC−84 and LGA−128 packages respectively.

Table 29. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LCC−84 PINS

Package Pin No.	Pin Name	I/O Type	Direction	Description
1	vdd_33	Supply		3.3 V Supply
2	nc			For test purposes only. Do not connect
3	mosi	CMOS	Input	SPI Master Out − Slave In
4	miso	CMOS	Output	SPI Master In − Slave Out
5	sck	CMOS	Input	SPI Input Clock
6	gnd_18	Supply		1.8 V Ground
7	vdd_18	Supply		1.8 V Supply
8	doutn1	LVDS	Output	LVDS Data Output Channel #1 (Negative), Not connected for P3−SN/SE
9	doutp1	LVDS	Output	LVDS Data Output Channel #1 (Positive), Not connected for P3−SN/SE
10	doutn0	LVDS	Output	LVDS Data Output Channel #0 (Negative)
11	doutp0	LVDS	Output	LVDS Data Output Channel #0 (Positive)
12	nc			For test purposes only. Do not connect
13	nc			For test purposes only. Do not connect
14	clock_outn	LVDS	Output	LVDS Clock Output (Negative)
15	clock_outp	LVDS	Output	LVDS Clock Output (Positive)
16	doutn2	LVDS	Output	LVDS Data Output Channel #2 (Negative)
17	doutp2	LVDS	Output	LVDS Data Output Channel #2 (Positive)
18	doutn3	LVDS	Output	LVDS Data Output Channel #3 (Negative), Not connected for P3−SN/SE
19	doutp3	LVDS	Output	LVDS Data Output Channel #3 (Positive), Not connected for P3−SN/SE
20	gnd_18	Supply		Supply 1.8 V Ground
21	vdd_18	Supply		Supply 1.8 V Supply
22	nc			For test purposes only. Do not connect
23	vdd_33	Supply		Supply 3.3 V Supply
24	gnd_33	Supply		Supply 3.3 V Ground
25	doutn4	LVDS	Output	LVDS Data Output Channel #4 (Negative)
26	doutp4	LVDS	Output	LVDS Data Output Channel #4 (Positive)
27	doutn5	LVDS	Output	LVDS Data Output Channel #5 (Negative), Not connected for P3−SN/SE
28	doutp5	LVDS	Output	LVDS Data Output Channel #5 (Positive), Not connected for P3−SN/SE
29	syncn	LVDS	Output	LVDS Sync Channel Output (Negative)
30	syncp	LVDS	Output	LVDS Sync Channel Output (Positive)
31	nc			For test purposes only. Do not connect
32	nc			For test purposes only. Do not connect
33	doutn7	LVDS	Output	LVDS Data Output Channel #7 (Negative), Not connected for P3−SN/SE
34	doutp7	LVDS	Output	LVDS Data Output Channel #7 (Positive), Not connected for P3−SN/SE

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Table 29. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LCC−84 PINS

Package Pin No.	Pin Name	I/O Type	Direction	Description
35	doutn6	LVDS	Output	LVDS Data Output Channel #6 (Negative)
36	doutp6	LVDS	Output	LVDS Data Output Channel #6 (Positive)
37	vdd_33	Supply		Supply 3.3 V Supply
38	gnd_33	Supply		Supply 3.3 V Ground
39	gnd_18	Supply		Supply 1.8 V Ground
40	vdd_18	Supply		Supply 1.8 V Supply
41	lvds_clock_in n	LVDS	Input	LVDS Clock Input (Negative)
42	lvds_clock_in p	LVDS	Input	LVDS Clock Input (Positive)
43	nc			For test purposes only. Do not connect
44	clk_pll	CMOS	Input	Reference Clock Input for PLL
45	vdd_18	Supply		1.8 V Supply
46	gnd_18	Supply		Supply 1.8 V Ground
47	ibias_master	Analog		Master Bias Reference
48	nc			For test purposes only. Do not connect
49	vdd_33	Supply		3.3 V Supply
50	gnd_33	Supply		3.3 V Ground
51	nc			For test purposes only. Do not connect
52	nc			For test purposes only. Do not connect
53	nc			For test purposes only. Do not connect
54	nc			For test purposes only. Do not connect
55	nc			For test purposes only. Do not connect
56	nc			For test purposes only. Do not connect
57	vdd_pix	Supply		Pixel Array Supply
58	gnd_colpc	Supply		Pixel Array Ground
59	nc			For test purposes only. Do not connect
60	vdd_pix	Supply		Pixel Array Supply
61	gnd_colpc	Supply		Pixel Array Ground
62	gnd_33	Supply		3.3 V Ground
63	vdd_33	Supply		3.3 V Supply
64	nc			For test purposes only. Do not connect
65	gnd_colpc	Supply		Pixel Array Ground
66	vdd_pix	Supply		Pixel Array Supply
67	gnd_colpc	Supply		Pixel Array Ground
68	vdd_pix	Supply		Pixel Array Supply
69	nc			For test purposes only. Do not connect
70	trigger0	CMOS	Input	Trigger Input #0
71	trigger1	CMOS	Input	Trigger Input #1
72	nc			For test purposes only. Do not connect
73	nc			For test purposes only. Do not connect
74	nc			For test purposes only. Do not connect
75	nc			For test purposes only. Do not connect
76	nc			For test purposes only. Do not connect

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Table 29. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LCC−84 PINS

Package Pin No.	Pin Name	I/O Type	Direction	Description
77	trigger2	CMOS	Input	Trigger Input #2
78	monitor0	CMOS	Output	Monitor Output #0
79	vdd_33	Supply		Supply 3.3 V supply
80	gnd_33	Supply		Supply 3.3 V Ground
81	monitor1	CMOS	Output	Monitor Output #1
82	reset_n	CMOS	Input	Sensor Reset (Active Low)
83	ss_n	CMOS	Input	SPI Slave Select.
84	gnd_33	Supply		Supply 3.3 V Ground

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Table 30. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LGA−128 PADS

Package Pad No	Pin Name	I/O Type	Direction	Description
A1	gnd	Supply		Supply Ground
A2	gnd	Supply		Supply Ground
A3	nc			For test purposes only. Do not connect
A4	nc			For test purposes only. Do not connect
A5	nc			For test purposes only. Do not connect
A6	nc			For test purposes only. Do not connect
A7	nc			For test purposes only. Do not connect
A8	nc			For test purposes only. Do not connect
A9	nc			For test purposes only. Do not connect
A10	nc			For test purposes only. Do not connect
A11	nc			For test purposes only. Do not connect
A12	nc			For test purposes only. Do not connect
A13	gnd	Supply		Supply Ground
A14	gnd	Supply		Supply Ground
B1	gnd	Supply		Supply Ground
B2	gnd	Supply		Supply Ground
B3	gnd	Supply		Supply Ground
B4	gnd	Supply		Supply Ground
B5	gnd	Supply		Supply Ground
B6	gnd	Supply		Supply Ground
B7	gnd	Supply		Supply Ground
B8	gnd	Supply		Supply Ground
B9	gnd	Supply		Supply Ground
B10	gnd	Supply		Supply Ground
B11	gnd	Supply		Supply Ground
B12	gnd	Supply		Supply Ground
B13	gnd	Supply		Supply Ground
B14	gnd	Supply		Supply Ground
C1	nc			For test purposes only. Do not connect
C2	gnd	Supply		Supply Ground
C3	gnd	Supply		Supply Ground
C4	doutn0	LVDS	Output	LVDS Data Output Channel #0 (Negative)
C5	doutp0	LVDS	Output	LVDS Data Output Channel #0 (Positive)
C6	sck	CMOS	Input	SPI Input Clock
C7	mosi	CMOS	Input	SPI Master Out − Slave In
C8	ss_n	CMOS	Input	SPI Slave Select.
C9	reset_n	CMOS	Input	Sensor Reset (Active Low)
C10	monitor1	CMOS	Output	Monitor Output #1
C11	monitor0	CMOS	Output	Monitor Output #0
C12	gnd	Supply		Supply Ground
C13	gnd	Supply		Supply Ground

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Table 30. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LGA−128 PADS

Package Pad No	Pin Name	I/O Type	Direction	Description
C14	nc			For test purposes only. Do not connect
D1	nc			For test purposes only. Do not connect
D2	gnd	Supply		Supply Ground
D3	vdd_18	Supply		Supply 1.8 V Supply
D4	doutn1	LVDS	Output	LVDS Data Output Channel #1 (Negative), Not connected for P3−SN/SE
D5	doutp1	LVDS	Output	LVDS Data Output Channel #1 (Positive), Not connected for P3−SN/SE
D6	vdd_18	Supply		Supply 1.8 V Supply
D7	miso	CMOS	Output	SPI Master In − Slave Out
D8	gnd	Supply		Supply Ground
D9	vdd_33	Supply		Supply 3.3 V Supply
D10	vdd_33	Supply		Supply 3.3 V Supply
D11	trigger2	CMOS	Input	Trigger Input #2
D12	trigger1	CMOS	Input	Trigger Input #1
D13	gnd	Supply		Supply Ground
D14	nc			For test purposes only. Do not connect
E1	nc			For test purposes only. Do not connect
E2	gnd	Supply		Supply Ground
E3	vdd_18	Supply		Supply 1.8 V Supply
E4	doutn2	LVDS	Output	LVDS Data Output Channel #2 (Negative)
E5	doutp2	LVDS	Output	LVDS Data Output Channel #2 (Positive)
E6	gnd	Supply		Supply Ground
E7	gnd	Supply		Supply Ground
E8	gnd	Supply		Supply Ground
E9	gnd	Supply		Supply Ground
E10	gnd	Supply		Supply Ground
E11	gnd	Supply		Supply Ground
E12	trigger0	CMOS	Input	Trigger Input #0
E13	gnd	Supply		Supply Ground
E14	nc			For test purposes only. Do not connect
F1	nc			For test purposes only. Do not connect
F2	gnd	Supply		Supply Ground
F3	vdd_18	Supply		Supply 1.8 V Supply
F4	doutn3	LVDS	Output	LVDS Data Output Channel #3 (Negative), Not connected for P3−SN/SE
F5	doutp3	LVDS	Output	LVDS Data Output Channel #3 (Positive), Not connected for P3−SN/SE
F6	nc			For test purposes only. Do not connect
F7	nc			For test purposes only. Do not connect
F8	nc			For test purposes only. Do not connect
F9	nc			For test purposes only. Do not connect

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Table 30. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LGA−128 PADS

Package Pad No	Pin Name	I/O Type	Direction	Description
F10	gnd	Supply		Supply Ground
F11	gnd_colpc	Supply		pc Supply Pixel Array Ground
F12	vdd_pix	Supply		Supply Pixel Array Supply
F13	gnd	Supply		Supply Ground
F14	nc			For test purposes only. Do not connect
G1	nc			For test purposes only. Do not connect
G2	gnd	Supply		Supply Ground
G3	vdd_18	Supply		Supply 1.8 V Supply
G4	clock_outn	LVDS	Output	LVDS Clock Output (Negative)
G5	clock_outp	LVDS	Output	LVDS Clock Output (Positive)
G6	nc			For test purposes only. Do not connect
G7	nc			For test purposes only. Do not connect
G8	nc			For test purposes only. Do not connect
G9	nc			For test purposes only. Do not connect
G10	gnd	Supply		Supply Ground
G11	gnd_colpc	Supply		pc Supply Pixel Array Ground
G12	vdd_pix	Supply		Supply Pixel Array Supply
G13	gnd	Supply		Supply Ground
G14	nc			For test purposes only. Do not connect
H1	nc			For test purposes only. Do not connect
H2	gnd	Supply		Supply Ground
H3	vdd_33	Supply		Supply 3.3 V Supply
H4	syncn	LVDS	Output	LVDS Sync Channel Output (Negative)
H5	syncp	LVDS	Output	LVDS Sync Channel Output (Positive)
H6	nc			For test purposes only. Do not connect
H7	nc			For test purposes only. Do not connect
H8	nc			For test purposes only. Do not connect
H9	nc			For test purposes only. Do not connect
H10	gnd	Supply		Supply Ground
H11	gnd	Supply		Supply Ground
H12	vdd_33	Supply		Supply 3.3 V Supply
H13	gnd	Supply		Supply Ground
H14	nc			For test purposes only. Do not connect
J1	nc			For test purposes only. Do not connect
J2	gnd	Supply		Supply Ground
J3	vdd_18	Supply		Supply 1.8 V Supply
J4	doutn4	LVDS	Output	LVDS Data Output Channel #4 (Negative)
J5	doutp4	LVDS	Output	LVDS Data Output Channel #4 (Positive)
J6	nc			For test purposes only. Do not connect
J7	nc			For test purposes only. Do not connect
J8	nc			For test purposes only. Do not connect

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Table 30. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LGA−128 PADS

Package Pad No	Pin Name	I/O Type	Direction	Description
J9	nc			For test purposes only. Do not connect
J10	gnd	Supply		Supply Ground
J11	gnd_colpc	Supply		pc Supply Pixel Array Ground
J12	vdd_pix	Supply		Supply Pixel Array Supply
J13	gnd	Supply		Supply Ground
J14	nc			For test purposes only. Do not connect
K1	nc			For test purposes only. Do not connect
K2	gnd	Supply		Supply Ground
K3	vdd_18	Supply		Supply 1.8 V Supply
K4	doutn5	LVDS	Output	LVDS Data Output Channel #5 (Negative), Not connected for P3−SN/SE
K5	doutp5	LVDS	Output	LVDS Data Output Channel #5 (Positive), Not connected for P3−SN/SE
K6	gnd	Supply		Supply Ground
K7	gnd	Supply		Supply Ground
K8	gnd	Supply		Supply Ground
K9	gnd	Supply		Supply Ground
K10	gnd	Supply		Supply Ground
K11	gnd_colpc	Supply		pc Supply Pixel Array Ground
K12	vdd_pix	Supply		Supply Pixel Array Supply
K13	gnd	Supply		Supply Ground
K14	nc			For test purposes only. Do not connect
L1	nc			For test purposes only. Do not connect
L2	gnd	Supply		Supply Ground
L3	vdd_18	Supply		Supply 1.8 V Supply
L4	doutn6	LVDS	Output	LVDS Data Output Channel #6 (Negative)
L5	doutp6	LVDS	Output	LVDS Data Output Channel #6 (Positive)
L6	vdd_18	Supply		Supply 1.8 V Supply
L7	lvds_clock_inp	LVDS	Input	LVDS Clock Input (Positive)
L8	gnd	Supply		Supply Ground
L9	gnd	Supply		Supply Ground
L10	gnd	Supply		Supply Ground
L11	vdd_33	Supply		Supply 3.3 V Supply
L12	gnd	Supply		Supply Ground
L13	gnd	Supply		Supply Ground
L14	nc			For test purposes only. Do not connect
M1	nc			For test purposes only. Do not connect
M2	gnd	Supply		Supply Ground
M3	gnd	Supply		Supply Ground
M4	doutn7	LVDS	Output	LVDS Data Output Channel #7 (Negative), Not connected for P3−SN/SE

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Table 30. PIN LIST FOR P1−SN/SE/FN, P3−SN/SE FOR LGA−128 PADS

Package Pad No	Pin Name	I/O Type	Direction	Description
M5	doutp7	LVDS	Output	LVDS Data Output Channel #7 (Positive), Not connected for P3−SN/SE
M6	vdd_33	Supply		Supply 3.3 V Supply
M7	lvds_clock_in n	LVDS	Input	LVDS Clock Input (Negative)
M8	clk_pll	CMOS	Input	Reference Clock Input for PLL
M9	vdd_18	Supply		Supply 1.8 V Supply
M10	gnd	Supply		Supply Ground
M11	ibias_master	Analog		Master Analog Master Bias Reference
M12	gnd	Supply		Supply Ground
M13	gnd	Supply		Supply Ground
M14	nc			For test purposes only. Do not connect
N1	gnd	Supply		Supply Ground
N2	gnd	Supply		Supply Ground
N3	gnd	Supply		Supply Ground
N4	gnd	Supply		Supply Ground
N5	gnd	Supply		Supply Ground
N6	gnd	Supply		Supply Ground
N7	gnd	Supply		Supply Ground
N8	gnd	Supply		Supply Ground
N9	gnd	Supply		Supply Ground
N10	gnd	Supply		Supply Ground
N11	gnd	Supply		Supply Ground
N12	gnd	Supply		Supply Ground
N13	gnd	Supply		Supply Ground
N14	gnd	Supply		Supply Ground
P1	gnd	Supply		Supply Ground
P2	gnd	Supply		Supply Ground
P3	nc			For test purposes only. Do not connect
P4	nc			For test purposes only. Do not connect
P5	nc			For test purposes only. Do not connect
P6	nc			For test purposes only. Do not connect
P7	nc			For test purposes only. Do not connect
P8	nc			For test purposes only. Do not connect
P9	nc			For test purposes only. Do not connect
P10	nc			For test purposes only. Do not connect
P11	nc			For test purposes only. Do not connect
P12	nc			For test purposes only. Do not connect
P13	gnd	Supply		Supply Ground
P14	gnd	Supply		Supply Ground

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Table 31. MECHANICAL SPECIFICATION FOR LCC−84 PINS AND LGA−128 PADS

Parameter	Description	Min	Typ	Max	Units
Die (with Pin 1 to the left center)	Die thickness		725		μm
	Die Size		14.7 x 14.25		mm^2
	Die center, X offset to the center of package	−50	0	50	μm
	Die center, Y offset to the center of the package	−50	0	50	μm
	Die position, tilt to the Die Attach Plane	−1	0	1	deg
	Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides)	−1	0	1	deg
	Optical center referenced from die/package center (X−dir) PYTHON 5 MP		−231.38		μm
	Optical center referenced from die/package center (X−dir) PYTHON 2 MP		−154.58		μm
	Optical center referenced from die/package center (Y−dir) PYTHON 5 MP / 2 MP		1697.17		μm
	Distance from bottom of the package to top of the die surface	1.145	1.25	1.405	mm
	Distance from top of the die surface to top of the glass lid	0.745	1.13	1.495	mm
Glass Lid Specification	XY size		19 x 19		mm
	Thickness	0.45	0.55	0.65	mm
	Spectral response range	400		1000	nm
	Transmission of glass lid (refer to Figure 48)		92		%
Glass Lid Material	D263 Teco				
Mechanical Shock	JESD22−B104C; Condition G			2000	g
Vibration	JESD22−B103B; Condition 1			2000	Hz
Mounting Profile	Reflow profile according to J−STD−020D.1			260	°C
CTE	Coefficient of Thermal expansion of the LCC Package Coefficient of Thermal expansion of the LGA Package		7.6 7.1		μm/°C

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Table 32. OPTICAL CENTER INFORMATION FOR THE PYTHON 5000/2000 IN LCC−84 PINS AND LGA−128 PADS

		PYTHON5000		PYTHON2000	
	References*	**X (μm)**	**Y (μm)**	**X (μm)**	**Y (μm)**
Die Outer Coordinates	D1	0	14250	0	14250
	D2	14700	14250	14700	14250
	D3	14700	0	14700	0
	D4	0	0	0	0
Die Center	CD	7350	7125	7350	7125
Active Area Coordinates	A1	878.63	13756.57	878.63	13756.57
	A2	13358.63	13756.57	13358.63	13756.57
	A3	13358.63	3887.77	13358.63	3887.77
	A4	878.63	3887.77	878.63	3887.77
Active Area Center	AA	7118.63	8822.17	7195.43	8822.17
	Pitch	4.8	4.8	4.8	4.8
	# Pixels	2600	2056	2600	2056
	# Dummy	8	8	616	792
	# Active Pixels	2592	2048	1984	1264
	Act_A1	897.83	13737.37	2433.83	11855.77
	Act_A2	13339.43	13737.37	11957.03	11855.77
	Act_A3	13339.43	3906.97	11957.03	5788.57
	Act_A4	897.83	3906.97	2433.83	5788.57

*Refer to Figure 46 below.

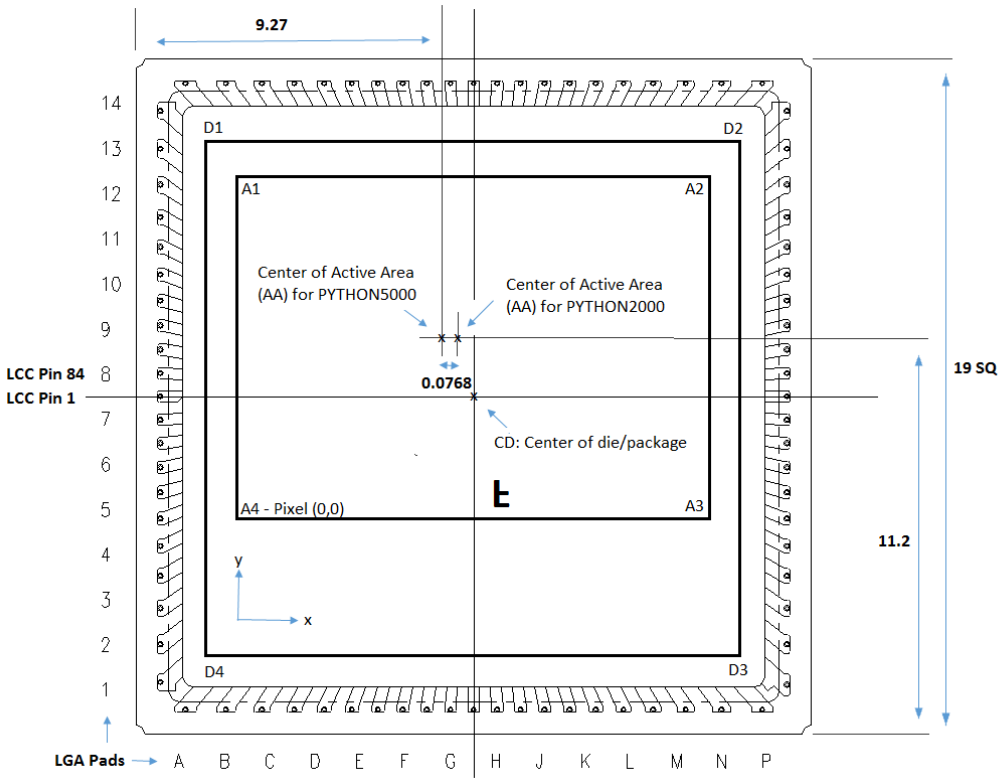

Figure 46. Optical Center Information for PYTHON 5000/2000 for LCC−84 Pins and LGA−128 Pads

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Packing and Tray Specification

The PYTHON packing specification with **onsemi** packing labels is packed as follows:

Table 33. PACKING AND TRAY INFORMATION FOR P1−SN/SE/FN, P3−SN/SE

Package Size (mm)				Tray		Restraint		Box
Package	Length	Width	Thickness*	Tray	Quantity / Tray	Strap	Bag	Tray Quantity
LCC−84 pin	19	19	2.58	KS−87054 1	42	Rubber band	Double bagged using MBB and pink ESD bag	5 trays + 1 cover tray
LGA−128 pin								

*Includes package, glass and glue attach thickness.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

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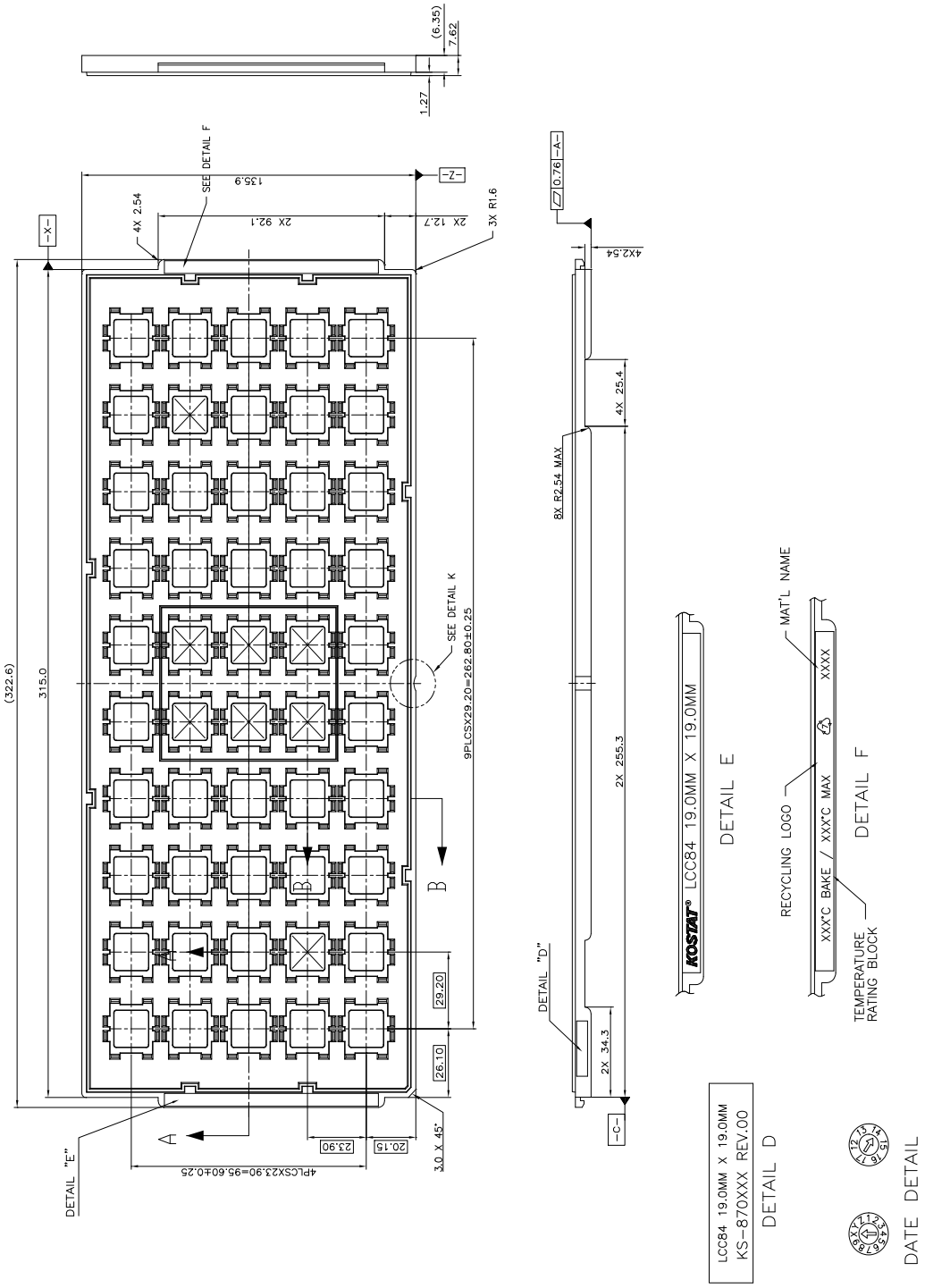

Figure 47. Packing and Tray Configuration

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Glass Lid

The PYTHON 2000 and PYTHON 5000 sensor uses a glass lid without any coatings. Figure 48 shows the transmission characteristics of the glass lid.

As shown in Figure 48, no infrared attenuating color filter glass is used. A filter must be provided in the optical path when color devices are used (source: http://www.pgo−online.com).

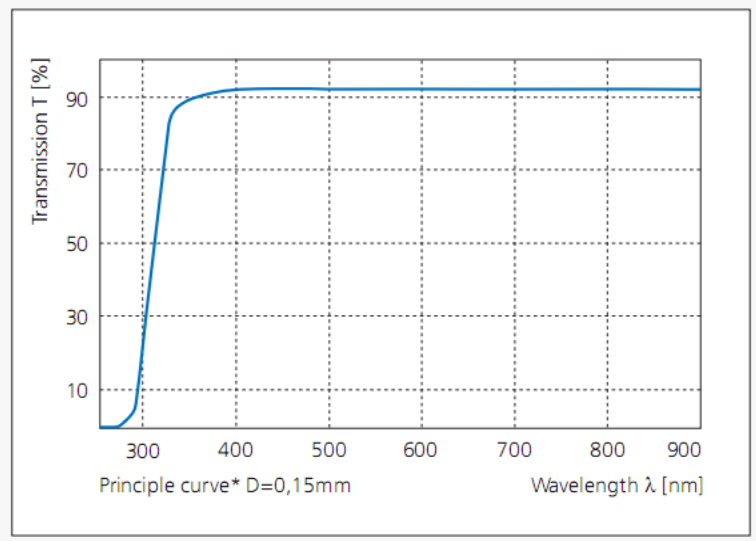

Figure 48. Transmission Characteristics of the Glass Lid

Protective Film Option (−QTI Versions)

For certain size and speed options, the sensor can be delivered with a protective foil that is intended to be removed after assembly. The dimensions of the foil are as illustrated in Figure 49 with the tab aligned towards one corner of the package as illustrated in Figure 50.

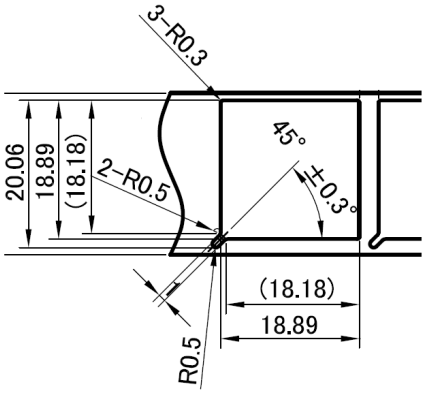

Figure 49. Dimensions of the Tape

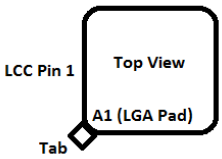

Figure 50. Location of the Pull Tab in Reference to LCC−Pin 1 and LGA−Pad A1

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SPECIFICATIONS AND USEFUL REFERENCES

The following references are available to customers under NDA at the **onsemi** Image Sensor Portal:

- Product Acceptance Criteria
- Product Qualification Report
- PYTHON Developer's Guide AND9362/D

Material Composition is available at: http://www.onsemi.com/PowerSolutions/MaterialComposition.do?searchParts=PYTHON5000

Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

For information on acronyms and a glossary of terms used, please download *Image Sensor Terminology* (TND6116/D) from www.onsemi.com.

Return Material Authorization (RMA)

Refer to the **onsemi** RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

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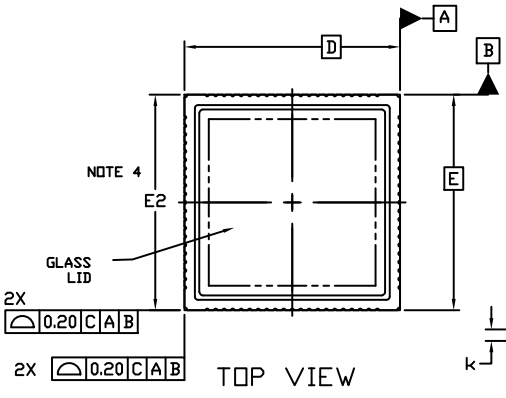
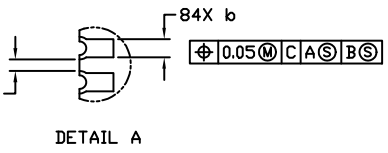
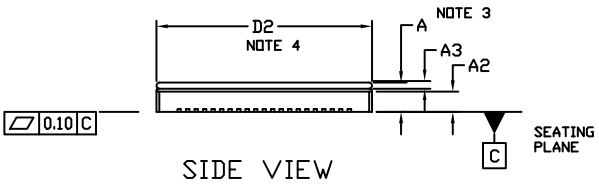
LCC84, 19x19
CASE 115BC
ISSUE A

DATE 26 JUN 2015



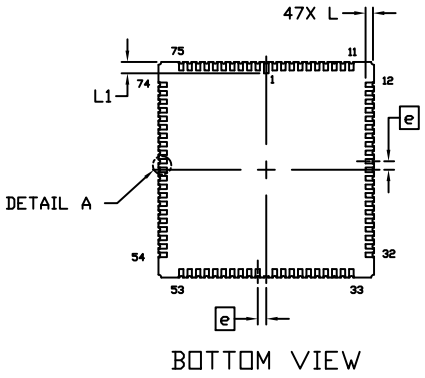


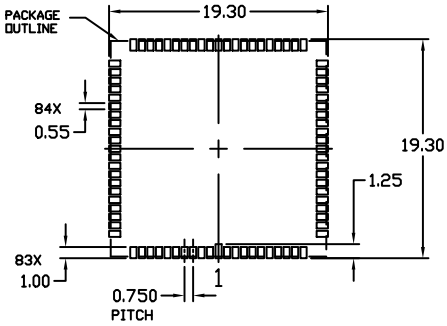


NOTES:

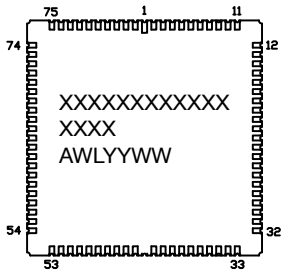
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE LID IS DEFINED BY DIMENSIONS D2 AND E2 AND HAS A MAXIMUM ALLOWABLE SHIFT OF 0.60 BEYOND DIMENSIONS D AND E.

DIM	MILLIMETERS	
	MIN.	MAX.
A	2.08	2.74
A2	1.78 REF	
A3	0.55 REF	
b	0.32	0.48
D	19.00 BSC	
D2	19.00 REF	
E	19.00 BSC	
E2	19.00 REF	
e	0.75 BSC	
k	0.12	---
L	0.62	0.88
L1	1.00 REF	





GENERIC MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

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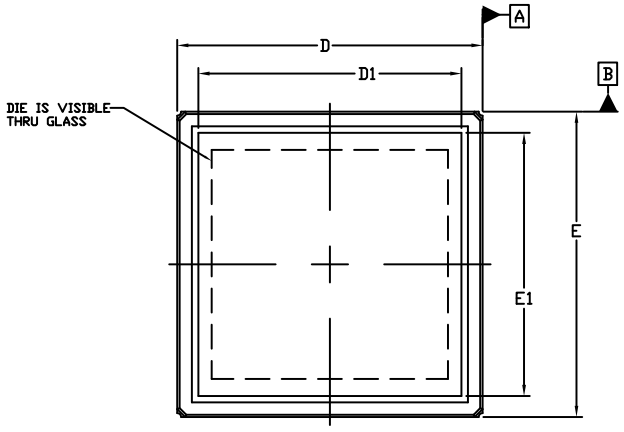
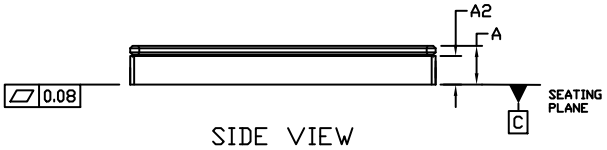
LBGA128 19x19
CASE 715AB
ISSUE O

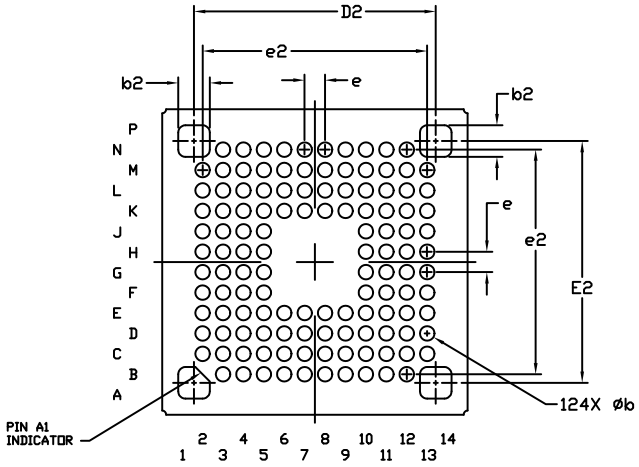
DATE 05 JUL 2016



TOP VIEW



SIDE VIEW

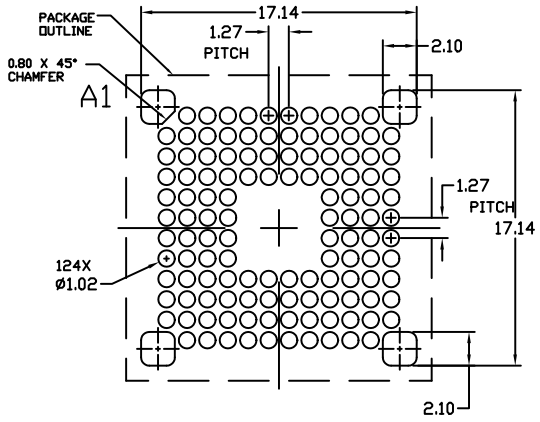


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	2.74
A2	1.78 REF	
b	0.80	1.00
b2	1.87	2.07
D	18.87	19.13
D1	16.37 REF	
D2	14.94	15.14
E	18.87	19.13
E1	16.37 REF	
E2	14.94	15.14
e	1.22	1.32
e2	13.86	14.08



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