# LDO Regulator, 150 mA, 38 V, 1 μA I$_Q$, with PG

# NCV8730

The NCV8730 device is based on unique combination of features – very low quiescent current, fast transient response and high input and output voltage ranges. The NCV8730 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Quiescent current of only 1 μA makes this device ideal solution for battery-powered, always-on systems. Several fixed output voltage versions are available as well as the adjustable version.

The device (version B) implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

Internal short circuit and over temperature protections saves the device against overload conditions.

## Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage:
  - 1.2 V to 24 V (FIX)
  - 1.2 V to 37 V (ADJ)
- Capable of Sourcing 200 mA Peak Output Current
- Very Low Quiescent Current: 1 μA typ.
- Low Dropout: 290 mV typ. at 150 mA, 3.3 V Version
- Output Voltage Accuracy ±1%
- Power Good Circuit (Version B)
- Stable with Small 1 μF Ceramic Capacitors
- Built-in Soft Start Circuit to Suppress Inrush Current
- Over-Current and Thermal Shutdown Protections
- Available in Small TSOP-5 and WDFNW6 (2x2) Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
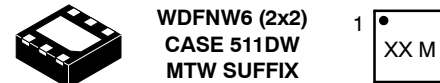- These Devices are Pb-Free and are RoHS Compliant

## Typical Applications

- Body Control Modules
- LED Lighting
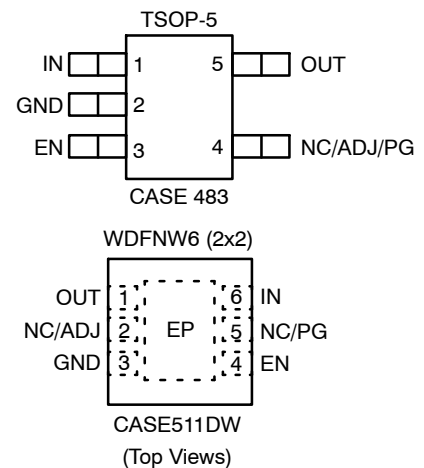- On Board Charger
- General Purpose Automotive

## MARKING DIAGRAMS
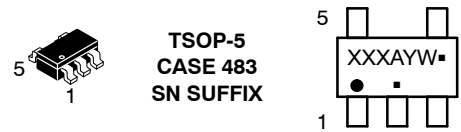
**TSOP-5**
**CASE 483**
**SN SUFFIX**

XXXAYW■

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

**WDFNW6 (2x2)**
**CASE 511DW**
**MTW SUFFIX**

XX M

XX = Specific Device Code
M = Date Code

## PIN ASSIGNMENTS

TSOP-5

| IN | 1 | 5 | OUT |
| GND | 2 | | |
| EN | 3 | 4 | NC/ADJ/PG |

CASE 483

WDFNW6 (2x2)

| OUT | 1 | | 6 | IN |
| NC/ADJ | 2 | EP | 5 | NC/PG |
| GND | 3 | | 4 | EN |

CASE511DW

(Top Views)

## ORDERING INFORMATION

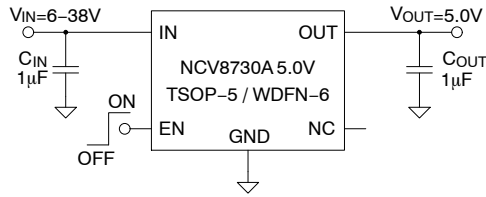# NCV8730

## TYPICAL APPLICATION SCHEMATICS
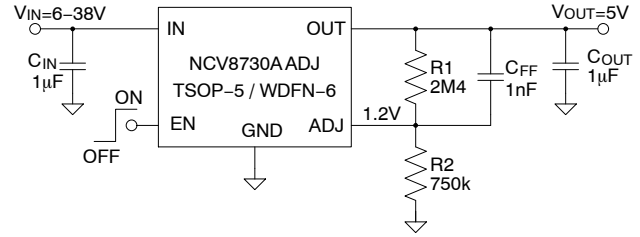


Figure 1. Fixed Output Voltage Application (No PG)



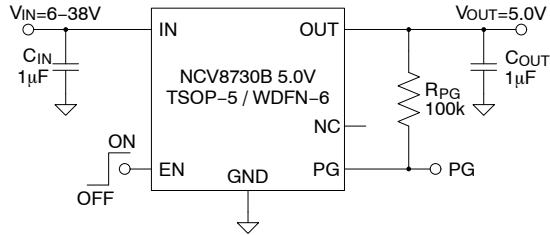Figure 2. Adjustable Output Voltage Application (No PG)



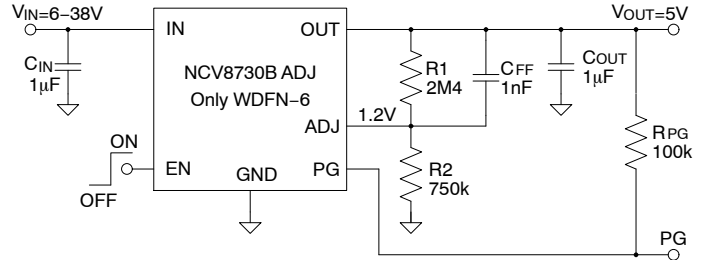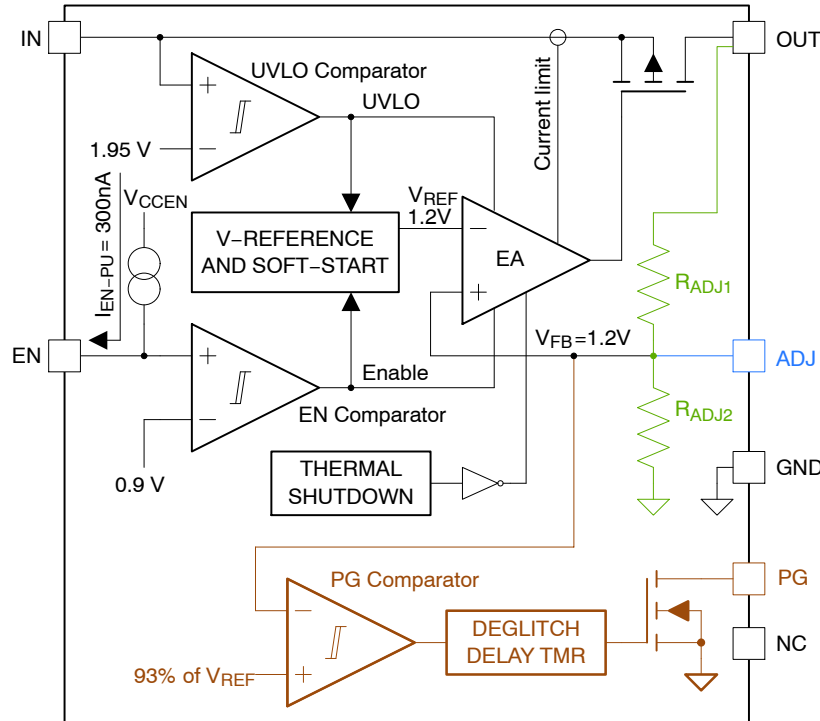Figure 3. Fixed Output Voltage Application with PG



Figure 4. Adjustable Output Voltage Application with PG

$$V_{OUT} = V_{ADJ} \cdot \left( 1 + \frac{R_1}{R_2} \right) + I_{ADJ} \cdot R_1$$

## SIMPLIFIED BLOCK DIAGRAM



Note: Blue objects are valid for ADJ version
Green objects are valid for FIX version
Brown objects are valid for B version (with PG)

Figure 5. Internal Block Diagram

# NCV8730

**PIN DESCRIPTION – TSOP-5 package**

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | IN | Power supply input pin. |
| 2 | GND | Ground pin. |
| 3 | EN | Enable input pin (high – enabled, low – disabled). If this pin is connected to IN pin or if it is left unconnected (pull-up resistor is not required) the device is enabled. |
| 4 | ADJ/PG/NC | **ADJ** (ADJ device version only):<br>• Adjust input pin. Could be connected to the output resistor divider or to the output pin directly.<br>**PG** (FIX device versions with PG functionality):<br>• Power good output pin. High level for power ok, low level for fail. If not used, could be left unconnected or shorted to GND.<br>**NC** (FIX device versions without PG functionality):<br>• Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation. |
| 5 | OUT | Output pin. |

**PIN DESCRIPTION – WDFN-6 package**

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT | Output pin. |
| 2 | NC/ADJ | **ADJ** (ADJ device version only):<br>• Adjust input pin. Could be connected to the output resistor divider or to the output pin directly.<br>**NC** (all FIX device versions):<br>• Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation. |
| 3 | GND | Ground pin. |
| 4 | EN | Enable input pin (high – enabled, low – disabled). If this pin is connected to IN pin or if it is left unconnected (pull-up resistor is not required) the device is enabled. |
| 5 | NC/PG | **PG** (ADJ/FIX device versions with PG functionality):<br>• Power good output pin. High level for power ok, low level for fail. If not used, could be left unconnected or shorted to GND.<br>**NC** (ADJ/FIX device versions without PG functionality):<br>• Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation. |
| 6 | IN | Power supply input pin. |
| EP | EPAD | Exposed pad pin. Should be connected to the GND plane. |

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| VIN Voltage (Note 1) | $V_{IN}$ | −0.3 to 40 | V |
| VOUT Voltage | $V_{OUT}$ | ADJ version & FIX versions $V_{OUT-NOM}$ > 5.0 V:<br>   −0.3 to [($V_{IN}$ + 0.3) or 40 V; whichever is lower]<br>FIX versions $V_{OUT-NOM}$ ≤ 5.0 V:<br>   −0.3 to [($V_{IN}$ + 0.3) or 6.0 V; whichever is lower] | V |
| EN Voltage | $V_{EN}$ | −0.3 to ($V_{IN}$ + 0.3) | V |
| ADJ Voltage | $V_{FB/ADJ}$ | −0.3 to 5.5 | V |
| PG Voltage | $V_{PG}$ | −0.3 to ($V_{IN}$ + 0.3) | V |
| Output Current | $I_{OUT}$ | Internally limited | mA |
| PG Current | $I_{PG}$ | 3 | mA |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| Storage Temperature | $T_{STG}$ | −55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2000 | V |
| ESD Capability, Charged Device Model (Note 2) | $ESD_{CDM}$ | 1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.
1.  Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2.  This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001, EIA/JESD22-A114 (AEC-Q100-002)
    ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002, EIA/JESD22-C101 (AEC Q100-011D)

**THERMAL CHARACTERISTICS** (Note 3)

| Characteristic | Symbol | WDFNW6 2x2 | TSOP-5 | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction-to-Air | $R_{thJA}$ | 67 | 178 | °C/W |
| Thermal Resistance, Junction-to-Case (top) | $R_{thJCt}$ | 89 | 93 | °C/W |
| Thermal Resistance, Junction-to-Case (bottom) | $R_{thJCb}$ | 11 | N/A | °C/W |
| Thermal Resistance, Junction-to-Board (top) | $R_{thJBt}$ | 44 | 53 | °C/W |
| Thermal Characterization Parameter, Junction-to-Case (top) | $Psi_{JCt}$ | 4.6 | 18 | °C/W |
| Thermal Characterization Parameter, Junction-to-Board [FEM] | $Psi_{JB}$ | 44 | 53 | °C/W |

3.  Measured according to JEDEC board specification (board 1S2P, Cu layer thickness 1 oz, Cu area 650 mm$^2$, no airflow). Detailed description of the board can be found in JESD51-7.

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = $V_{OUT-NOM}$ + 1 V and $V_{IN}$ ≥ 2.7 V, $V_{EN}$ = 1.2 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF (effective capacitance − Note 4), $T_J$ = −40 °C to 125 °C, ADJ tied to OUT, unless otherwise specified) (Note 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Recommended Input Voltage | | $V_{IN}$ | 2.7 | – | 38 | V |
| Output Voltage Accuracy | $T_J$ = 25 °C | $V_{OUT}$ | −1 | – | 1 | % |
| | $T_J$ = −40 °C to +125 °C | | −1 | – | 2 | |
| ADJ Reference Voltage | ADJ version only | $V_{ADJ}$ | – | 1.2 | – | V |
| ADJ Input Current | $V_{ADJ}$ = 1.2 V | $I_{ADJ}$ | −0.1 | 0.01 | 0.1 | μA |
| Line Regulation | $V_{IN}$ = $V_{OUT-NOM}$ + 1 V to 38 V and $V_{IN}$ ≥ 2.7 V | $\Delta V_{O(\Delta VI)}$ | – | – | 0.2 | %$V_{OUT}$ |
| Load Regulation | $I_{OUT}$ = 0.1 mA to 150 mA | $\Delta V_{O(\Delta IO)}$ | – | – | 0.4 | %$V_{OUT}$ |
| Quiescent Current (version A) | $V_{IN}$ = $V_{OUT-NOM}$ + 1 V to 38 V, $I_{OUT}$ = 0 mA | $I_Q$ | – | 1.3 | 2.5 | μA |
| Quiescent Current (version B) | $V_{IN}$ = $V_{OUT-NOM}$ + 1 V to 38 V, $I_{OUT}$ = 0 mA | | – | 1.8 | 3.0 | |
| Ground Current | $I_{OUT}$ = 150 mA | $I_{GND}$ | – | 325 | 450 | μA |

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = $V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, $V_{EN}$ = 1.2 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF (effective capacitance − Note 4), $T_J$ = −40 °C to 125 °C, ADJ tied to OUT, unless otherwise specified) (Note 5) (continued)

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Shutdown Current (Note 9) | $V_{EN}$ = 0 V, $I_{OUT}$ = 0 mA, $V_{IN}$ = 38 V | | $I_{SHDN}$ | – | 0.35 | 1.5 | μA |
| Output Current Limit | $V_{OUT}$ = $V_{OUT-NOM}$ − 100 mV | | $I_{OLIM}$ | 200 | 280 | 450 | mA |
| Short Circuit Current | $V_{OUT}$ = 0 V | | $I_{OSC}$ | 200 | 280 | 450 | mA |
| Dropout Voltage (Note 6) | $I_{OUT}$ = 150 mA | | $V_{DO}$ | – | 290 | 480 | mV |
| Power Supply Ripple Rejection | $V_{IN}$ = $V_{OUT-NOM}$ + 2 V $I_{OUT}$ = 10 mA | 10 Hz | PSRR | – | 80 | – | dB |
| | | 10 kHz | | – | 70 | – | |
| | | 100 kHz | | – | 42 | – | |
| | | 1 MHz | | – | 48 | – | |
| Output Voltage Noise | f = 10 Hz to 100 kHz | FIX–3.3 V | $V_N$ | – | 195 | – | μ$V_{RMS}$ |
| | | FIX–5.0 V | | – | 240 | – | |
| | | FIX–15.0 V | | – | 460 | – | |
| | | ADJ set to 5.0 V $C_{FF}$ = 100 pF | | – | 132 | – | |
| | | ADJ set to 5.0 V $C_{FF}$ = 10 nF | | – | 82 | – | |
| EN Threshold | $V_{EN}$ rising | | $V_{EN-TH}$ | 0.7 | 0.9 | 1.05 | V |
| EN Hysteresis | $V_{EN}$ falling | | $V_{EN-HY}$ | 0.01 | 0.1 | 0.2 | V |
| EN Internal Pull-up Current | $V_{EN}$ = 1 V, $V_{IN}$ = 5.5 V | | $I_{EN-PU}$ | 0.01 | 0.3 | 1.0 | μA |
| EN Input Leakage Current | $V_{EN}$ = 30 V, $V_{IN}$ = 30 V | | $I_{EN-LK}$ | −1.0 | 0.05 | 1.0 | μA |
| Start-up time (Note 7) | $V_{OUT-NOM} \leq$ 3.3 V | | $t_{START}$ | 100 | 250 | 500 | μs |
| | $V_{OUT-NOM}$ > 3.3 V | | | 300 | 600 | 1000 | |
| Internal UVLO Threshold | Ramp $V_{IN}$ up until output is turned on | | $V_{IUL-TH}$ | 1.6 | 1.95 | 2.6 | V |
| Internal UVLO Hysteresis | Ramp $V_{IN}$ down until output is turned off | | $V_{IUL-HY}$ | 0.05 | 0.2 | 0.3 | V |
| PG Threshold (Note 8) | $V_{OUT}$ falling | | $V_{PG-TH}$ | 90 | 93 | 96 | % |
| PG Hysteresis (Note 8) | $V_{OUT}$ rising | | $V_{PG-HY}$ | 0.1 | 2.5 | 4.0 | % |
| PG Deglitch Time (Note 8) | | | $t_{PG-DG}$ | 75 | 160 | 270 | μs |
| PG Delay Time (Note 8) | | | $t_{PG-DLY}$ | 120 | 320 | 600 | μs |
| PG Output Low Level Voltage (Note 8) | $I_{PG}$ = 1 mA | | $V_{PG-OL}$ | – | 0.2 | 0.4 | V |
| PG Output Leakage Current (Note 8) | $V_{PG}$ = 30 V | | $I_{PG-LK}$ | – | 0.01 | 1.0 | μA |
| Thermal Shutdown Temperature | Temperature rising from $T_J$ = +25 °C | | $T_{SD}$ | – | 165 | – | °C |
| Thermal Shutdown Hysteresis | Temperature falling from $T_{SD}$ | | $T_{SDH}$ | – | 20 | – | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A$ = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
6. Dropout measured when the output voltage falls 100 mV below the nominal output voltage. Limits are valid for all voltage versions with nominal output voltage higher than or equal to 2.5 V. For lower output voltage versions the dropout test is not applied because the input voltage during the test would fall below the minimum input voltage 2.7 V.
7. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.
8. Applicable only to version B (device option with power good output). PG threshold and PG hysteresis are expressed in percentage of nominal output voltage.
9. Shutdown current includes EN Internal Pull-up Current.

## TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 1.0$ μF, ADJ tied to OUT, $T_J = 25$ °C, unless otherwise specified
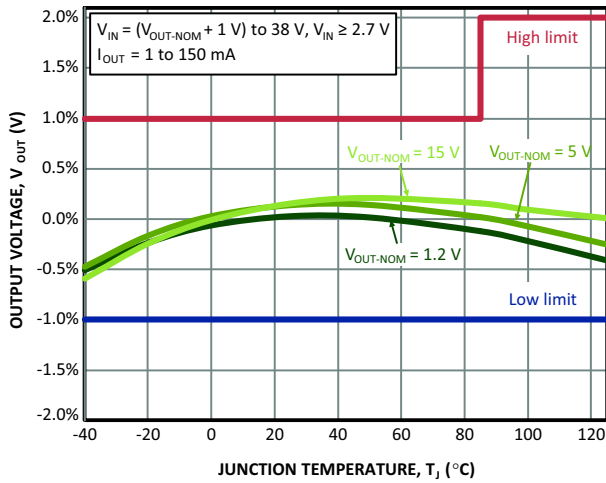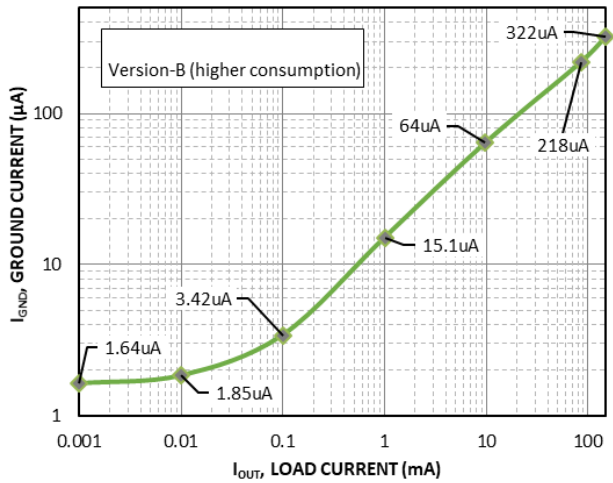


Figure 6. Output Voltage vs. Temperature



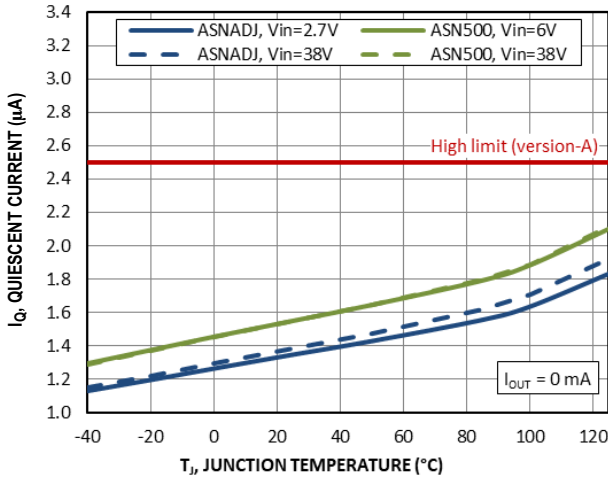Figure 7. Ground Current vs. Load
(NCP730-5.0V, Version-B)



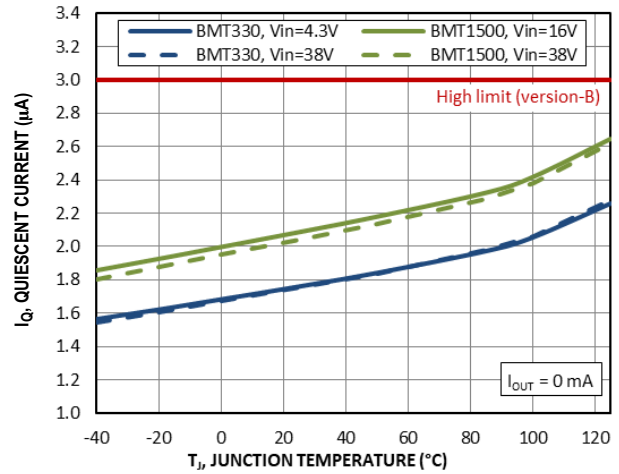Figure 8. Quiescent Current vs. Temperature
(Version-A)



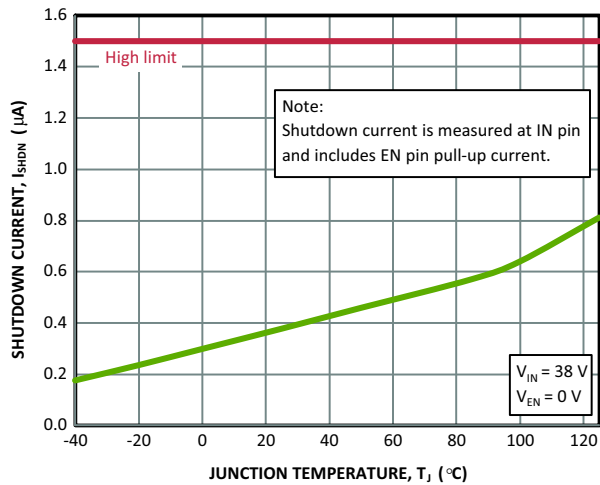Figure 9. Quiescent Current vs. Temperature
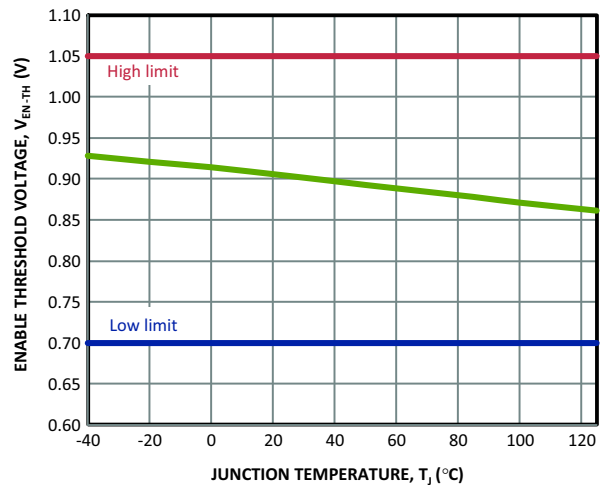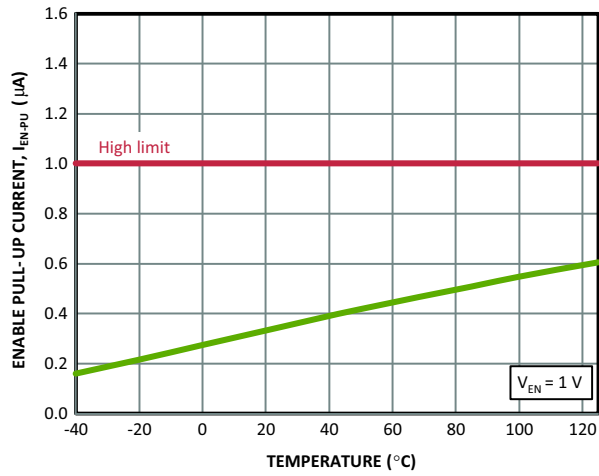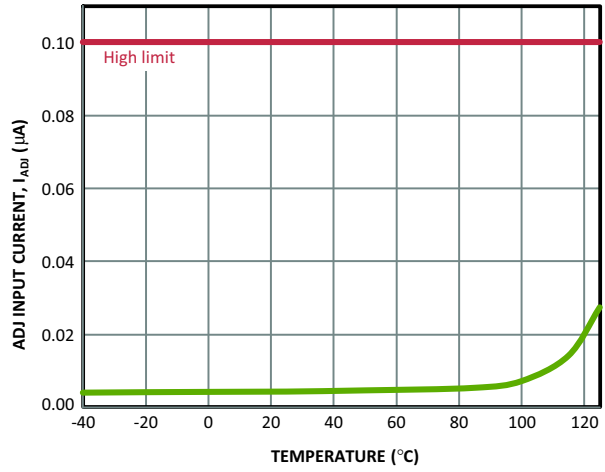(Version-B)



Figure 10. Shutdown Current vs. Temperature



Figure 11. Enable Threshold Voltage vs.
Temperature

## TYPICAL CHARACTERISTICS

$V_{IN}$ = $V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, $V_{EN}$ = 1.2 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1.0 µF, ADJ tied to OUT, $T_J$ = 25 °C, unless otherwise specified

**Figure 12. Enable Internal Pull-Up Current vs. Temperature**

**Figure 13. ADJ Input Current vs. Temperature**
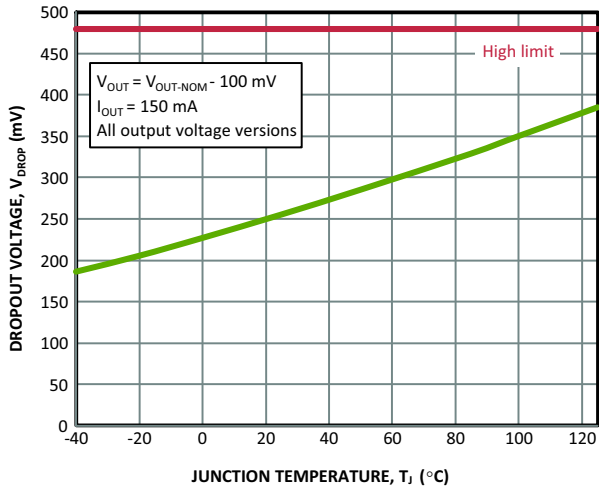
**Figure 14. Dropout Voltage vs. Temperature**
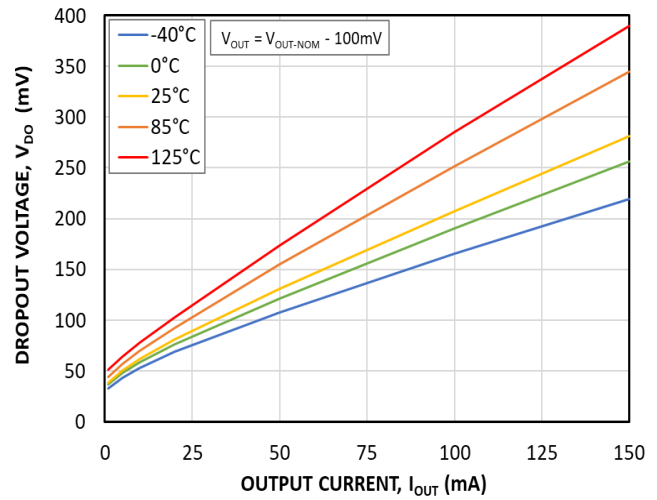
**Figure 15. Dropout Voltage vs. Output Current**
(all $V_{OUT}$ device options)
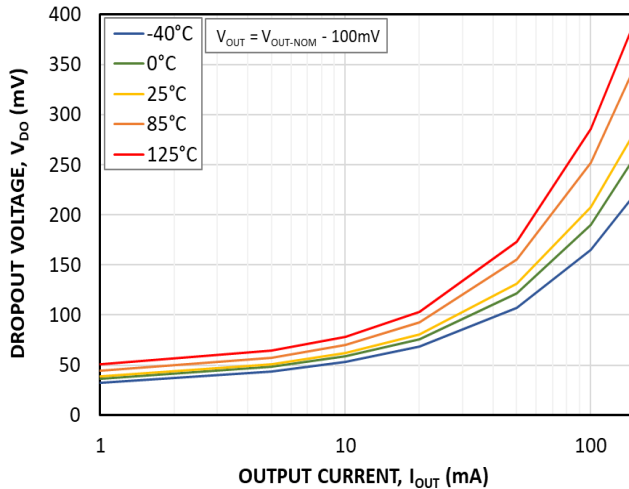
**Figure 16. Dropout Voltage vs. Output Current (log)**
(all $V_{OUT}$ device options)

## TYPICAL CHARACTERISTICS

$V_{IN}$ = $V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, $V_{EN}$ = 1.2 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1.0 μF, ADJ tied to OUT, $T_J$ = 25 °C, unless otherwise specified
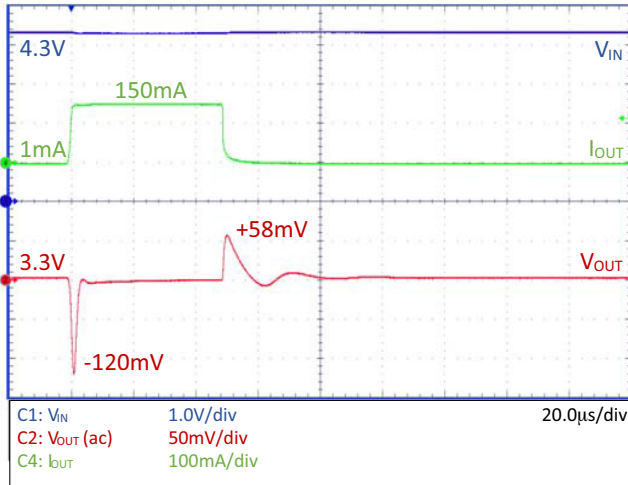


**Figure 17. Load Transient – NCV8730–3.3 V, $C_{OUT}$ = 1 μF**
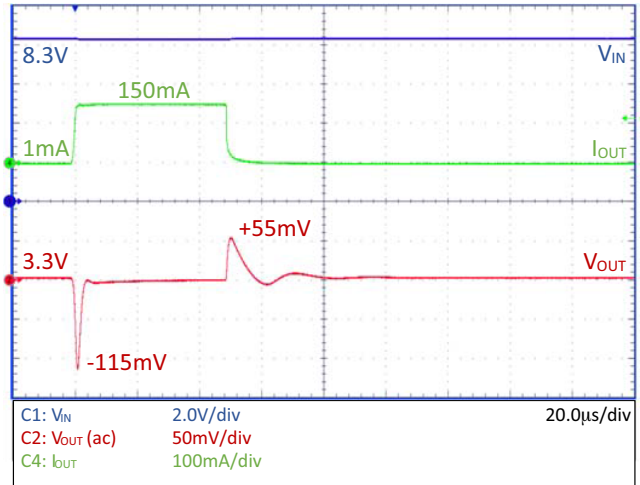


**Figure 18. Load Transient – NCV8730–3.3 V, $C_{OUT}$ = 1 μF**
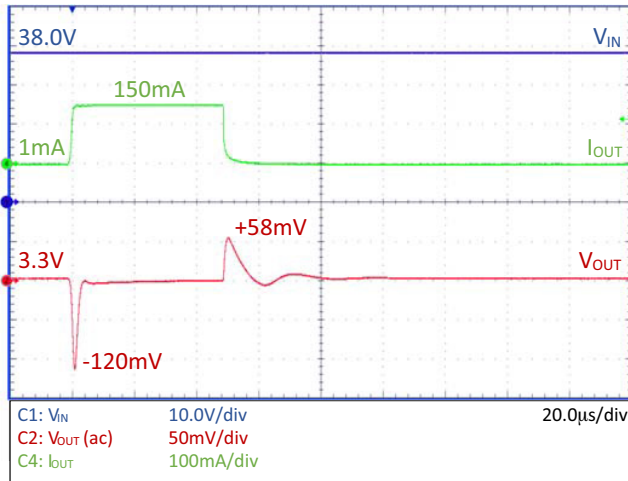


**Figure 19. Load Transient – NCV8730–3.3 V, $C_{OUT}$ = 1 μF**
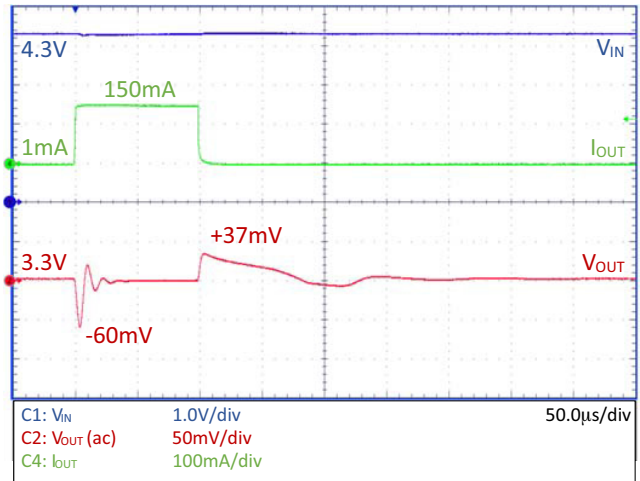


**Figure 20. Load Transient – NCV8730–3.3 V, $C_{OUT}$ = 10 μF**
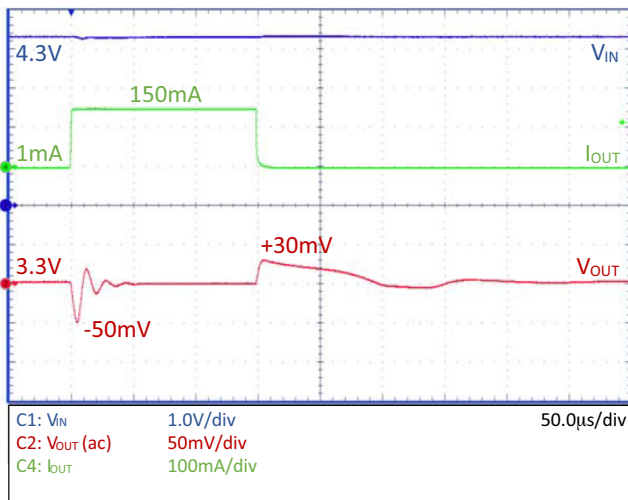


**Figure 21. Load Transient – NCV8730–3.3 V, $C_{OUT}$ = 22 μF**
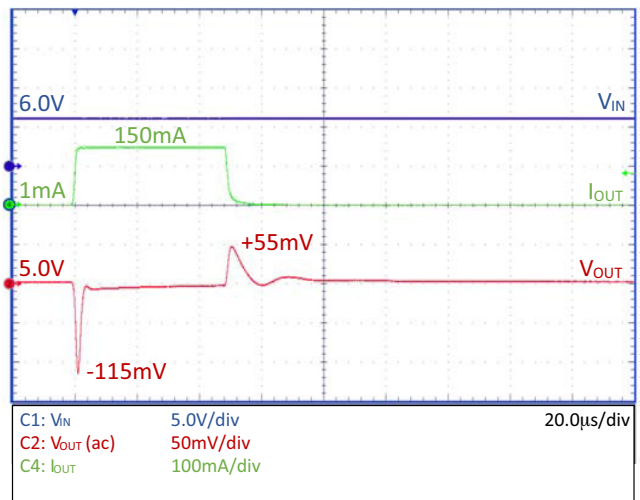


**Figure 22. Load Transient – NCV8730–5.0 V, $C_{OUT}$ = 1 μF**

## TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 1.0$ μF, ADJ tied to OUT, $T_J = 25$ °C, unless otherwise specified

**Figure 23. Load Transient – NCV8730–5.0 V,
$C_{OUT} = 1$ μF**
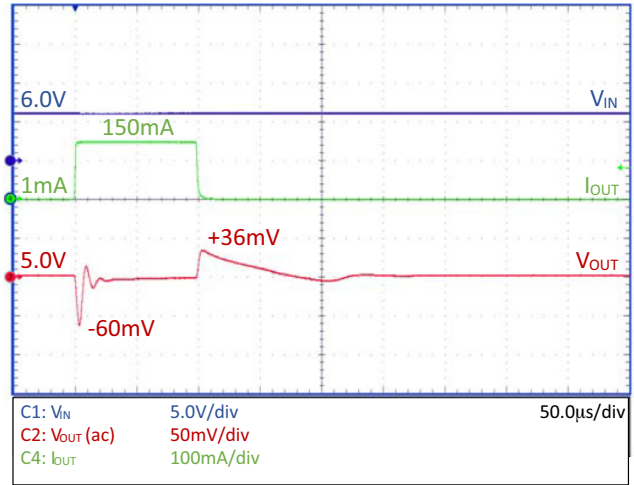
**Figure 24. Load Transient – NCV8730–5.0 V,
$C_{OUT} = 10$ μF**
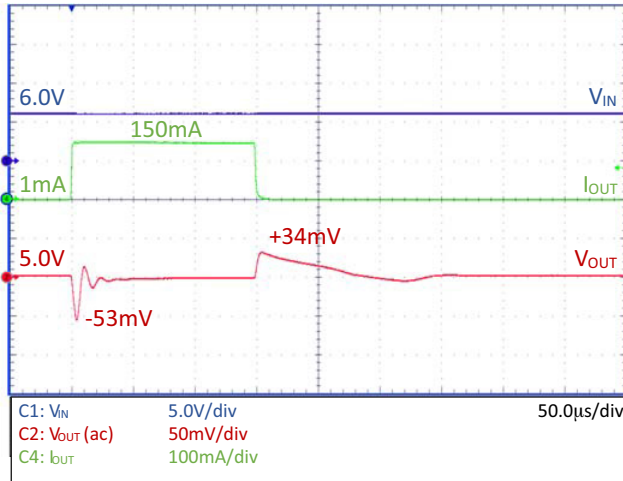
**Figure 25. Load Transient – NCV8730–5.0 V,
$C_{OUT} = 22$ μF**
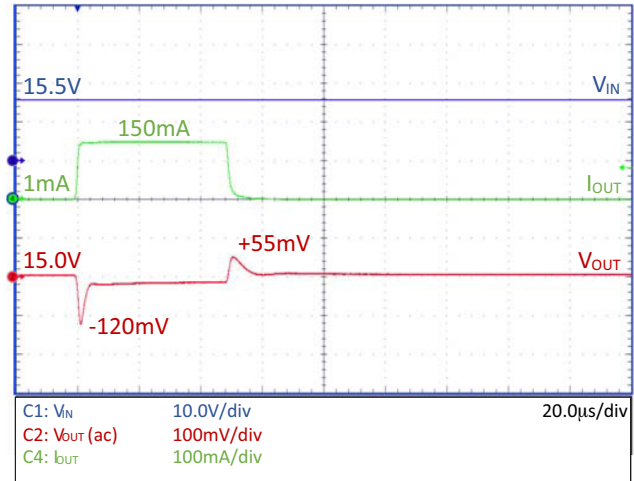
**Figure 26. Load Transient – NCV8730–15.0 V,
$C_{OUT} = 1$ μF**

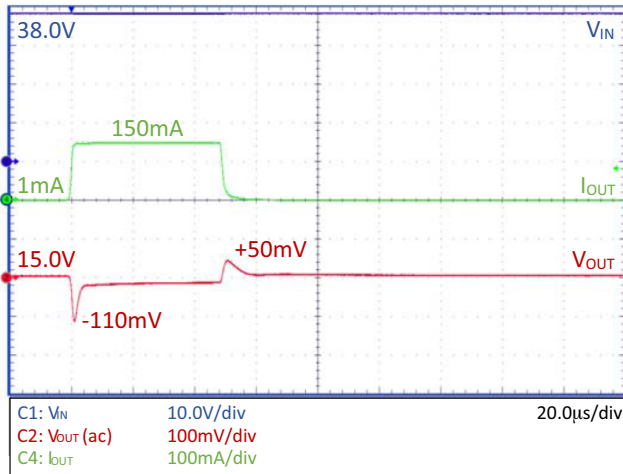**Figure 27. Load Transient – NCV8730–15.0 V,
$C_{OUT} = 1$ μF**

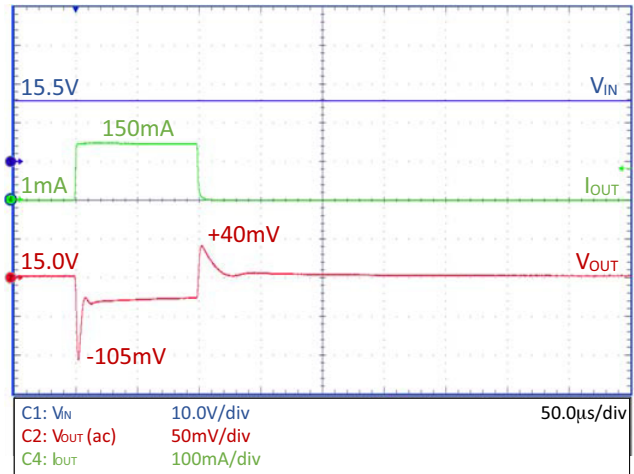**Figure 28. Load Transient – NCV8730–15.0 V,
$C_{OUT} = 10$ μF**

## TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 1.0$ µF, ADJ tied to OUT, $T_J = 25$ °C, unless otherwise specified



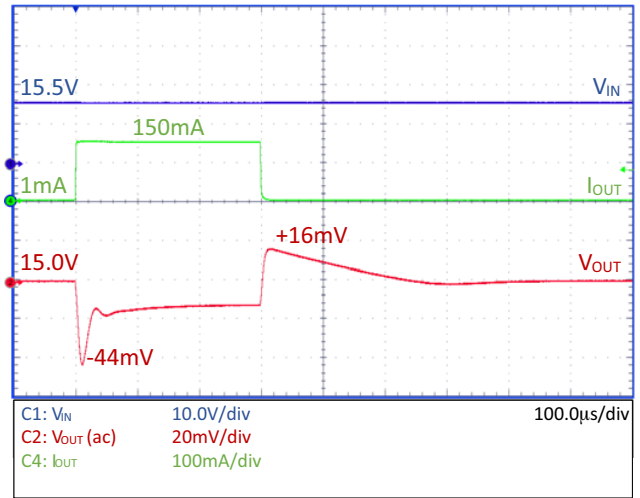**Figure 29. Load Transient – NCV8730–15.0 V, $C_{OUT}$ = 22 µF**



**Figure 30. Load Transient – NCV8730–15.0 V, $C_{OUT}$ = 50 µF**



**Figure 31. Line Transient – NCP730–3.3 V**



**Figure 32. Line Transient – NCP730–3.3 V**
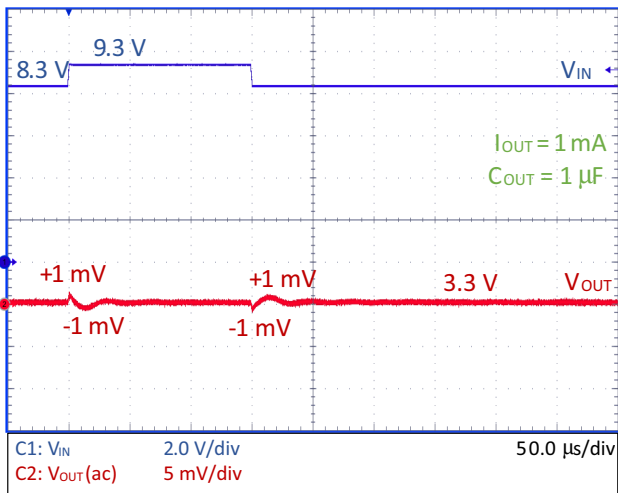


**Figure 33. Line Transient – NCP730–3.3 V**



**Figure 34. Line Transient – NCP730–3.3 V**

## TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 1.0$ μF, ADJ tied to OUT, $T_J = 25$ °C, unless otherwise specified
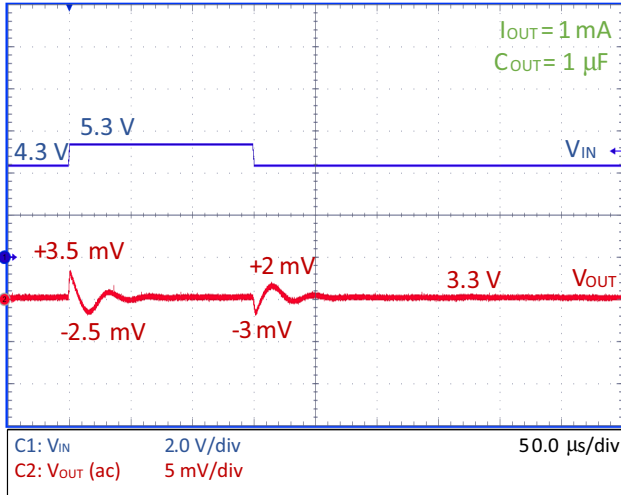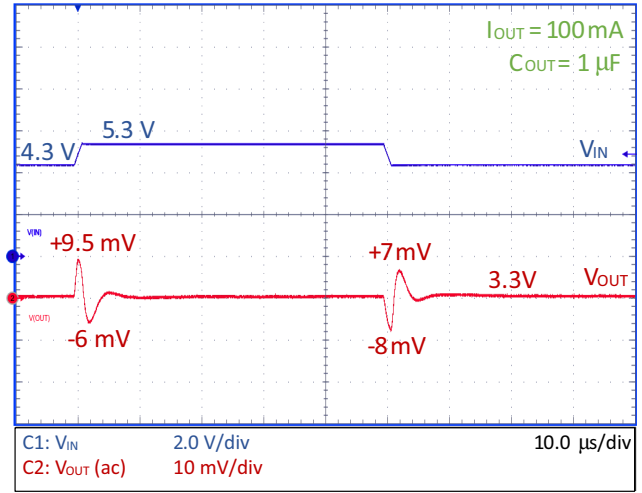


**Figure 35. Line Transient – NCP730–3.3 V**
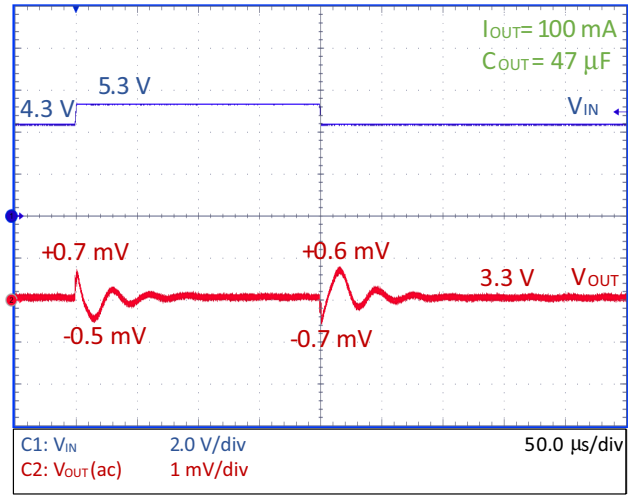


**Figure 36. Line Transient – NCP730–3.3 V**
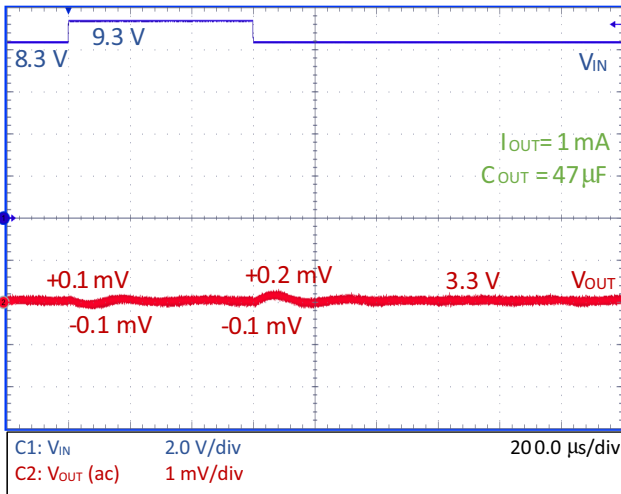


**Figure 37. Line Transient – NCP730–3.3 V**


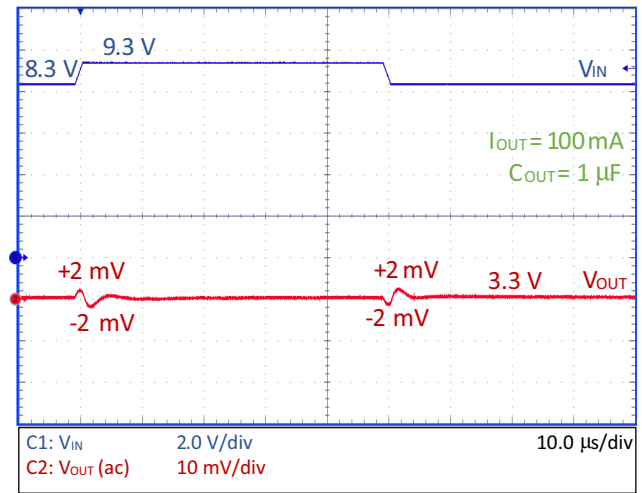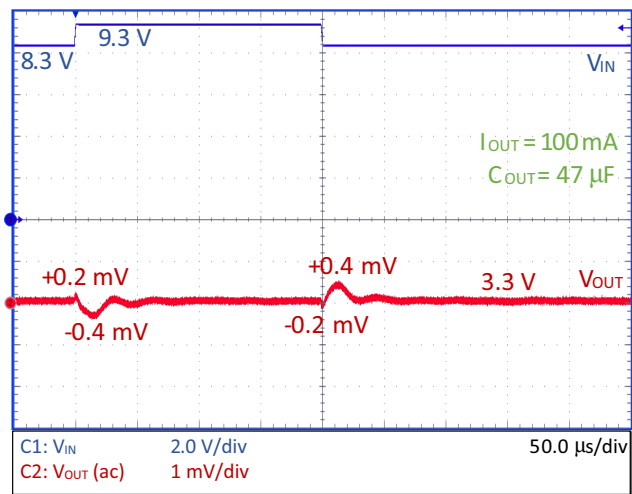
**Figure 38. Line Transient – NCP730–3.3 V**
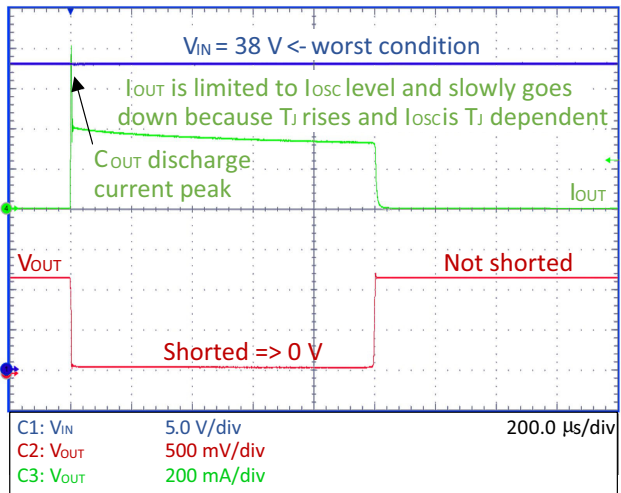


**Figure 39. Output Short (1 ms) –
NCP730-ADJ–1.2 V**
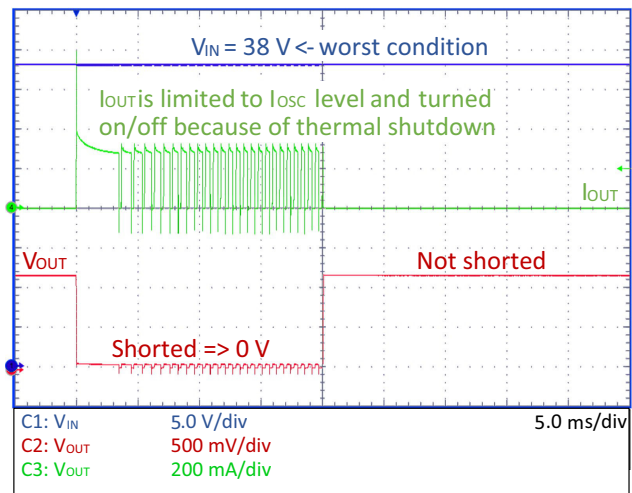


**Figure 40. Output Short (20 ms) –
NCP730-ADJ–1.2 V**

## TYPICAL CHARACTERISTICS

$V_{IN}$ = $V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, $V_{EN}$ = 1.2 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1.0 μF, ADJ tied to OUT, $T_J$ = 25 °C, unless otherwise specified



**Figure 41. PSRR – NCV8730–3.3 V, $C_{OUT}$ = 1 μF, $I_{OUT}$ = 10 mA**
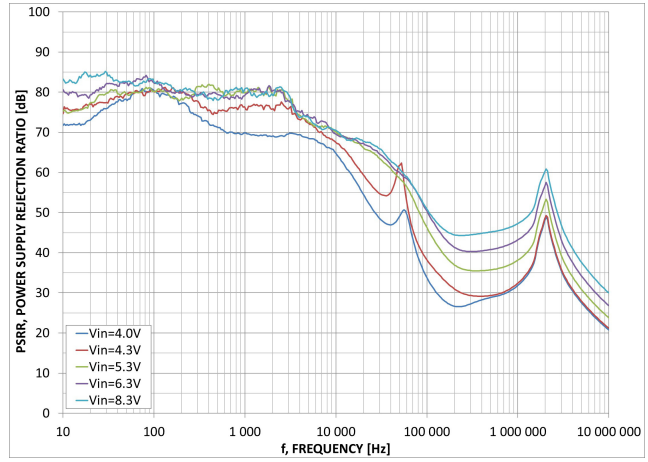


**Figure 42. PSRR – NCV8730–3.3 V, $C_{OUT}$ = 1 μF, $I_{OUT}$ = 100 mA**
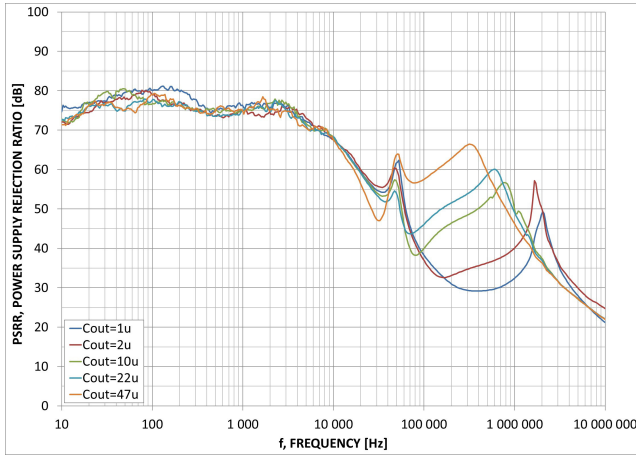


**Figure 43. PSRR – NCV8730–3.3 V, $V_{IN}$ = 4.3 V, $I_{OUT}$ = 100 mA**
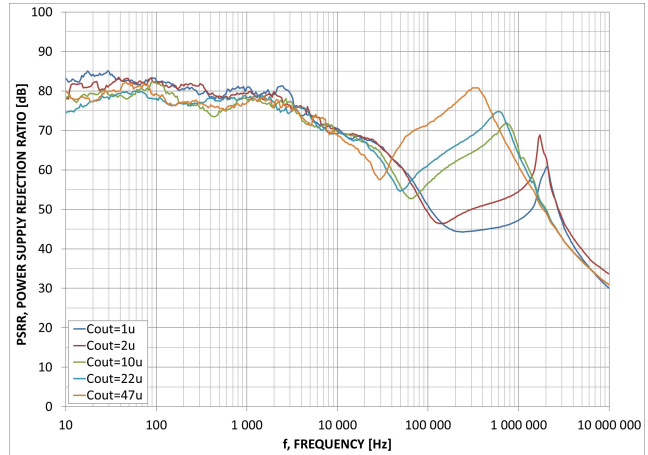


**Figure 44. PSRR – NCV8730–3.3 V, $V_{IN}$ = 8.3 V, $I_{OUT}$ = 100 mA**
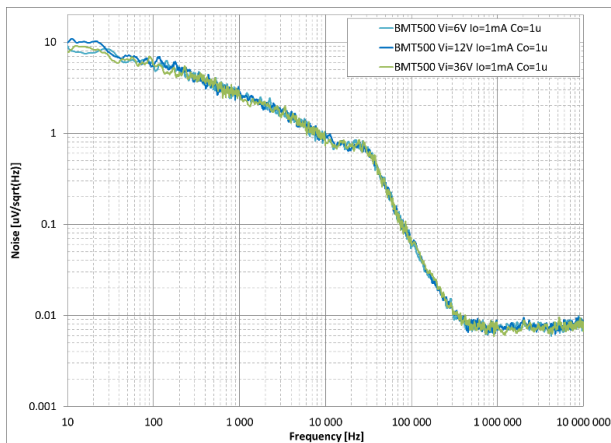


**Figure 45. Noise – FIX – 5.0 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1 μF, Different $V_{IN}$**
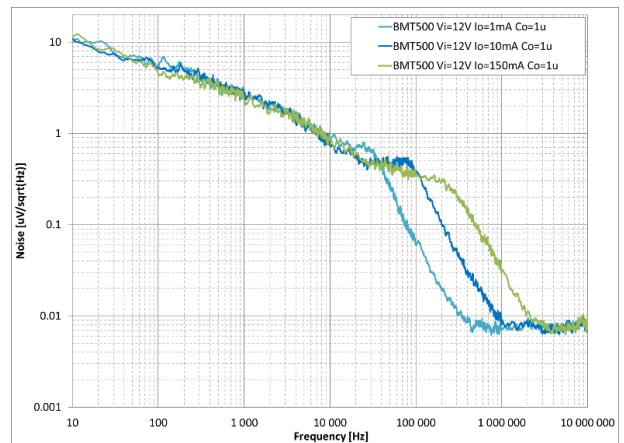


**Figure 46. Noise – FIX – 5.0 V, $C_{OUT}$ = 1 μF, Different $I_{OUT}$**

## TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT\text{-}NOM} + 1\ V$ and $V_{IN} \geq 2.7\ V$, $V_{EN} = 1.2\ V$, $I_{OUT} = 1\ mA$, $C_{OUT} = 1.0\ \mu F$, ADJ tied to OUT, $T_J = 25\ °C$, unless otherwise specified
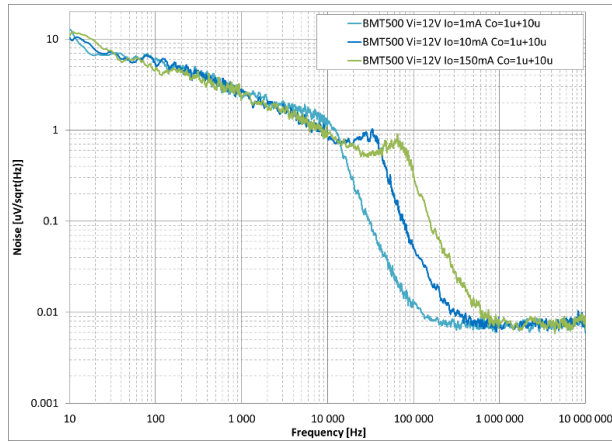


**Figure 47. Noise – FIX – 5.0 V,**
$C_{OUT} = 1\ \mu F + 10\ \mu F$, **Different** $I_{OUT}$
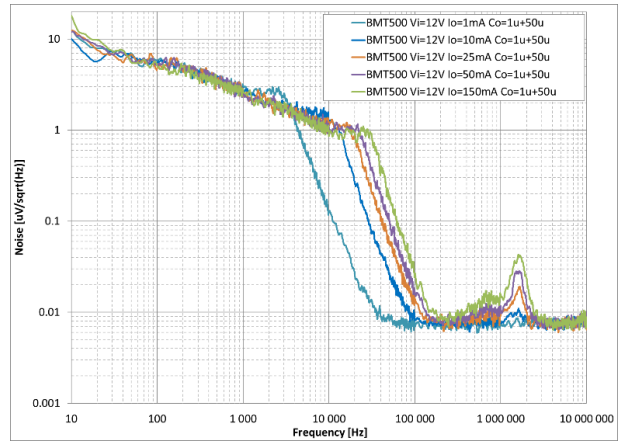


**Figure 48. Noise – FIX – 5.0 V,**
$C_{OUT} = 1\ \mu F + 50\ \mu F$, **Different** $I_{OUT}$
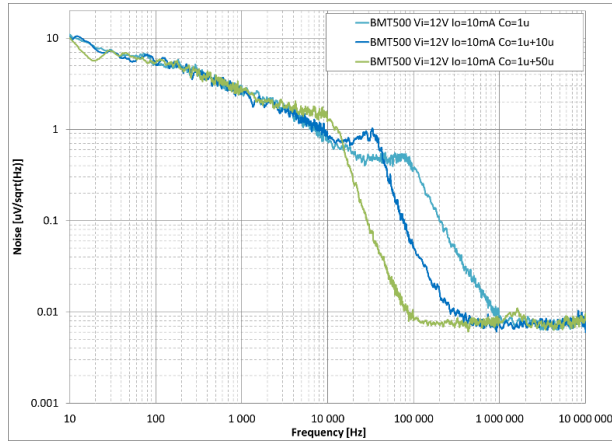


**Figure 49. Noise – FIX – 5.0 V, $I_{OUT} = 10\ mA$,**
**Different** $C_{OUT}$
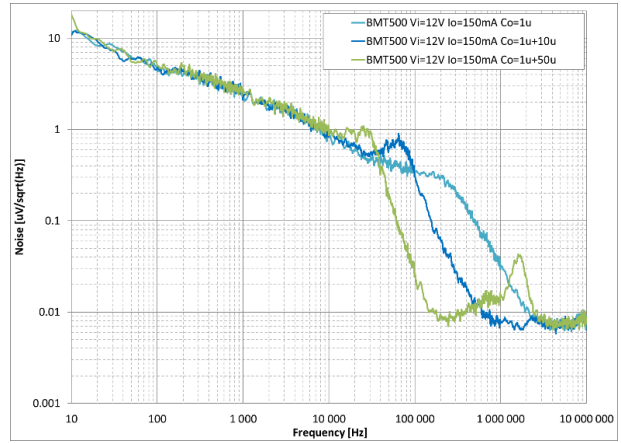


**Figure 50. Noise – FIX – 5.0 V, $I_{OUT} = 150\ mA$,**
**Different** $C_{OUT}$
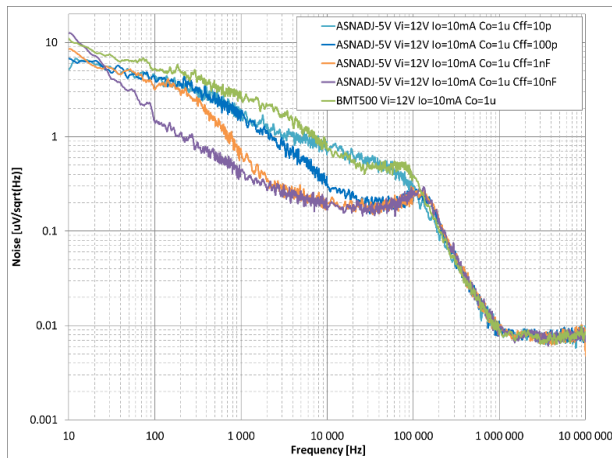


**Figure 51. Noise – ADJ-set–5.0 V with**
**Different $C_{FF}$ and FIX – 5.0 V**
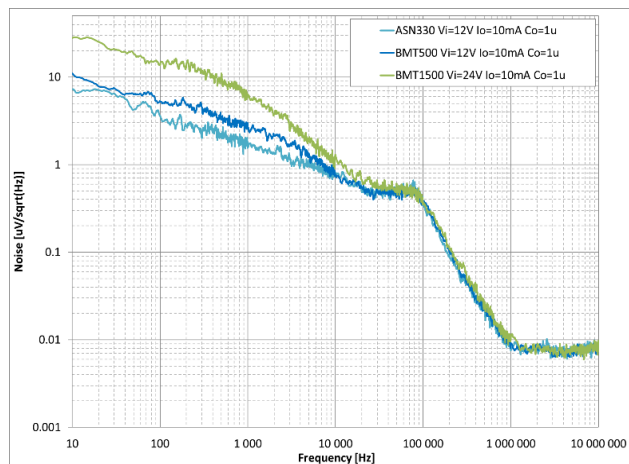


**Figure 52. Noise – FIX, $I_{OUT} = 10\ mA$,**
$C_{OUT} = 1\ \mu F$, **Different** $V_{OUT}$

## APPLICATIONS INFORMATION

### Input Capacitor Selection ($C_{IN}$)

Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater (max. value is not limited). This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes. When a large load transients (like 1 mA to 150 mA) happens in the application the input power source of the LDO needs to provide enough power and the input voltage must not go below the level defined by this equation: $V_{IN} = V_{OUT-NOM} + V_{DO}$ otherwise the output voltage drop will be significantly higher (because LDO will enter the dropout state). In some cases when power supply powering the LDO has a poor load transient response or when there is a long connection between LDO and its power source then capacitance of input capacitor needs to be high enough to cover the LDO's input voltage drop caused by load transient and maintains its value above the $V_{IN} = V_{OUT-NOM} + V_{DO}$ level (then $C_{IN}$ could be in range of hundreds of μF).

### Output Capacitor Selection ($C_{OUT}$)

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor's effective capacitance in range from 1 μF to 100 μF and ESR from 1 mΩ to 200 mΩ. The ceramic X7R or X5R type is recommended due to its low capacitance variations over the specified temperature range and low ESR. When selecting the output capacitor the changes with temperature and DC bias voltage needs to be taken into account. Especially for small package size capacitors such as 0402 or smaller the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR.

### Output Voltage

NCV8730 is available in two version from output voltage point of view. One is fixed output voltage version (FIX version) and the other one is adjustable output voltage version (ADJ version).

The ADJ version has ADJ pin, which could be connected to the OUT pin directly, just to compensate voltage drop across the internal bond wiring and PCB traces or could be connected to the middle point of the output voltage resistor divider for adjustment. When it is connected to the OUT pin the output voltage of the circuit is simply the same as the nominal output voltage of the LDO. At this case, without ADJ resistor divider, the LDO should be loaded by at least 200 nA (by the application or added pre-load resistor). When connected to the resistor divider the output voltage could be computed as the ADJ reference voltage (1.2 V) multiplied by the resistors divider ratio, see following equation.

$$V_{OUT} = V_{ADJ} \cdot \left( 1 + \frac{R_1}{R_2} \right) + I_{ADJ} \cdot R_1 \quad \text{(eq. 1)}$$

Where:
$V_{OUT}$ is output voltage of the circuit with resistor divider.
$V_{ADJ}$ is the LDO's ADJ reference voltage.
$I_{ADJ}$ is the LDO's ADJ pin input current.
$R_1$ and $R_2$ are resistors of output resistor divider.

At the classical "old style" regulators like LM317 etc. the resistors where small (100 Ω – 10 kΩ) to make regulator stable at light loads (divider was also a pre-load function). On NCV8730, which is very low quiescent current LDO regulator (1 μA), we need to care about current consumption of surrounding circuitry so we need to set the current through resistor divider flowing from $V_{OUT}$ through $R_1$ and $R_2$ to GND, as low as possible.

On the other hand, the parasitic leakage current flowing into ADJ pin ($I_{ADJ}$) causes $V_{OUT}$ voltage error (given by $I_{ADJ} \cdot R_1$). The $I_{ADJ}$ is temperature dependent so it is changing and we cannot compensate it in application, we just can minimize the influence by setting of $R_1$ value low, what is in opposite to maximizing its value because of current consumption.

So when selecting the $R_1$ and $R_2$ values we need to find a compromise between desired $V_{OUT}$ error (temperature dependent) and total circuit quiescent current.

If we want to simplify this task, we can say the $I_{R2}$ should be 100-times higher than $I_{ADJ}$ at expected $T_J$ temperature range. If we chose the ratio "$I_{R2}$ to $I_{ADJ}$" higher (for example more than 100 as stated before), the $\Delta V_{OUT}$ error caused by $I_{ADJ}$ change over temperature would be lower and opposite, if the ratio "$I_{R2}$ to $I_{ADJ}$" is smaller, the error would be bigger.

In limited $T_J$ temperature range −40 °C to +85 °C the $I_{ADJ}$ is about 10-times smaller than in the full temperature range −40 °C to +125 °C (see typical characteristics graph of $I_{ADJ}$ over temperatures), so we can use bigger $R_1$, $R_2$ values, as could be seen at next examples.

<u>Example 1:</u>
Desired $V_{OUT}$ voltage is 5.0 V. Computed maximal $T_J$ in application (based on max. power dissipation and cooling) is 85 °C. Than $I_{ADJ}$ at 85 °C is about: $I_{ADJ85} = 10$ nA.

**Figure 53. ADJ Output Voltage Schematic – Example 1**

We chose:

$$I_{R2} = 100 \cdot I_{ADJ85} = 100 \cdot 10E{-}9 = 1 \text{ μA}$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{1E{-}6} = 1.2 \text{ MΩ}$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ85} + I_{R2}} = \frac{5 - 1.2}{10E{-}9 + 1E{-}6}$$
$$= \frac{3.8}{1.01E{-}6} = 3.762 \text{ MΩ}$$

Verification:

For low temperature ($T_J = 25$ °C) the $I_{ADJ25} = 1$ nA:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 1E{-}9 \cdot 3.762E6$$
$$= 4.966 \text{ V}$$

For maximal temperature ($T_J = 85$ °C) the $I_{ADJ85} = 10$ nA:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 10E{-}9 \cdot 3.762E6$$
$$= 5.000 \text{ V}$$

Output voltage error for temperatures 85 °C to 25 °C is:

$$\Delta V_{OUT} = \frac{V_{OUT85} - V_{OUT25}}{V_{OUT85}} \cdot 100$$

$$= \frac{5.000 - 4.966}{5.000} \cdot 100 = 0.68\%$$

Total circuit quiescent current at $T_J = 25$ °C is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E{-}6 + 1.01E{-}6 = 2.31 \text{ μA}$$

We can see that current consumption of external resistor divider is almost the same as quiescent current of LDO.

Example 2:

Desired $V_{OUT}$ voltage is 5.0 V. Computed maximal $T_J$ in application (based on max. power dissipation and cooling) is in this case higher, 125 °C, to show the difference. Than maximal $I_{ADJ}$ at 125 °C is $I_{ADJ125} = 100$ nA (based on Electrical characteristics table).
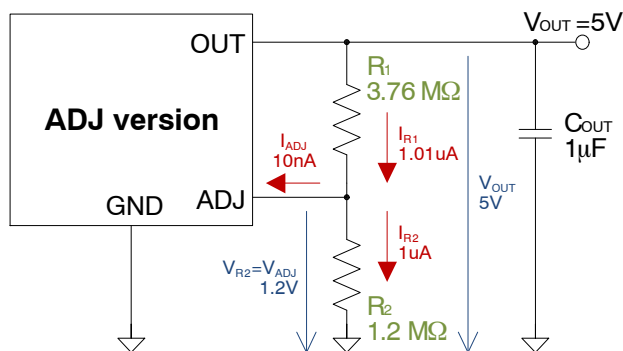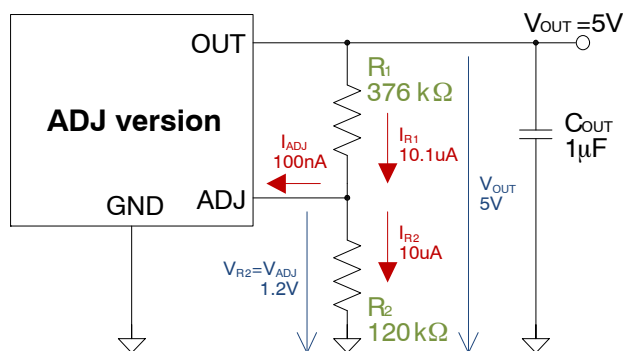


**Figure 54. ADJ Output Voltage Schematic – Example 2**

We chose:

$$I_{R2} = 100 \cdot I_{ADJ125} = 100 \cdot 100E{-}9 = 10 \text{ μA}$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{10E{-}6} = 120 \text{ kΩ}$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ125} + I_{R2}} = \frac{5 - 1.2}{100E{-}9 + 10E{-}6}$$
$$= \frac{3.8}{10.1E{-}6} = 376.2 \text{ kΩ}$$

Verification:

For low temperature ($T_J = 25$ °C) the $I_{ADJ25} = 1$ nA:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_{ADJ1}}{R_{ADJ2}}\right) + I_{ADJ} \cdot R_{ADJ1}$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 1E{-}9 \cdot 376.2E3$$
$$= 4.962 \text{ V}$$

For maximal temperature ($T_J = 125$ °C) the $I_{ADJ125} = 100$ nA:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 100E{-}9 \cdot 376.2E3$$
$$= 5.000 \text{ V}$$

Output voltage error for temperatures 125 °C to 25 °C is:

$$\Delta V_{OUT} = \frac{V_{OUT125} - V_{OUT25}}{V_{OUT125}} \cdot 100$$

$$= \frac{5.000 - 4.962}{5.000} \cdot 100 = 0.76\%$$

Total circuit quiescent current at $T_J = 25$ °C is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E{-}6 + 10.1E{-}6 = 11.4 \text{ μA!!!}$$

We can see that error of $V_{OUT}$ voltage is almost the same as in example 1 (because we have used the same "$I_{R2}$ to $I_{ADJ}$" ratio = 100x) but the application quiescent current is almost 10-times higher (because of 10-times higher divider current).

**C_FF Capacitor**

Even the NCV8730 is very low quiescent current device, both the load transients over/under shoots and settling times are excellent. See the Typical characteristics graphs.

At adjustable application, the external resistor divider with input ADJ pin capacity and ADJ pin PCB trace capacity to GND makes a low pass filter what negatively affects the dynamic behavior of the LDO. On the next picture is shown how this unwanted side effect could be compensated by adding of feed-forward capacitor $C_{FF}$ across $R_1$ resistor.
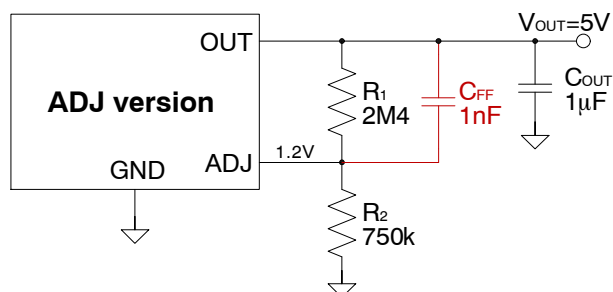


**Figure 55. ADJ Output Voltage Schematic – $C_{FF}$ Capacitor**

The value of the $C_{FF}$ depends on $R_1$ and $R_2$ resistor values. When $R_1$, $R_2$ values are in hundreds of kiloohms, proposed $C_{FF}$ value is 1 nF, as shown on picture above, for the best dynamic performance. Generally, the value could be in range from 0 to 10 nF.

On next three pictures is shown the $C_{FF}$ capacitor influence to dynamic parameters.
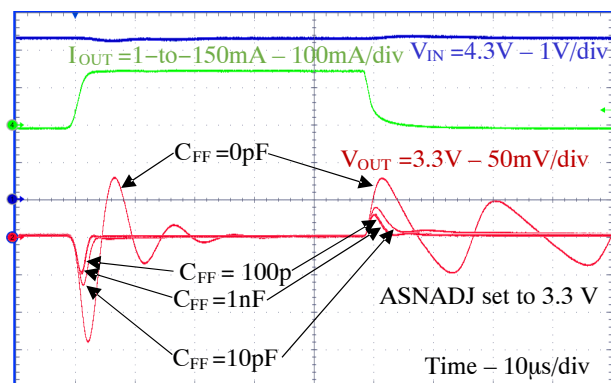


**Figure 56. Load Transient – Different $C_{FF}$**
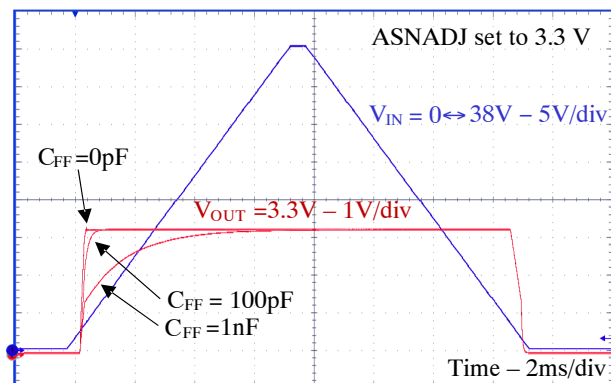


**Figure 57. Startup Timing – Different $C_{FF}$**
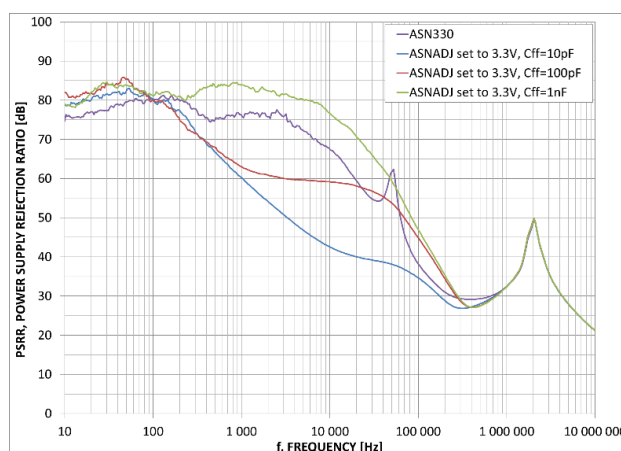


**Figure 58. PSRR – Different $C_{FF}$**
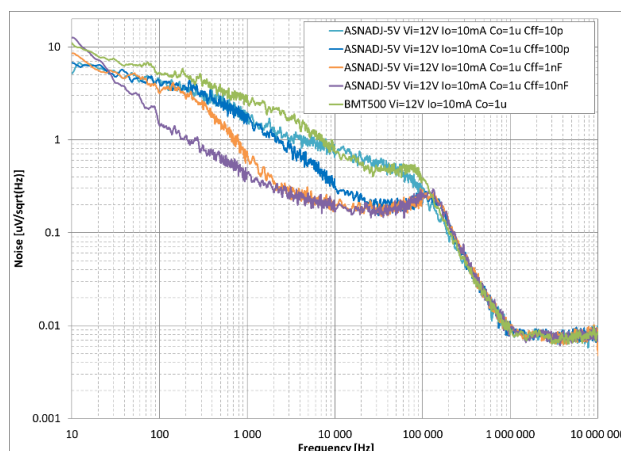


**Figure 59.**

**Startup**

In the NCV8730 device there are two main internal signals which triggers the startup process, the under-voltage lockout (UVLO) signal and enable signal. The first one comes from UVLO comparator, which monitors if the IN pin voltages is high enough, while the second one comes from EN pin comparator. Both comparators have embedded hysteresis to be insensitive to input noise.

Not only the comparator but also the pull-up current source is connected to EN pin. Current source is sourcing $I_{EN-PU} = 300$ nA current flowing out of the chip what ensures the level on the pin is high enough when it is left floating. The comparator compares the EN pin voltage with internal reference level 0.9 V (typ.). Hysteresis is 100 mV (typ.).

The UVLO comparator threshold voltage is 1.95 V (typ.) and hysteresis is 200 mV (typ.).
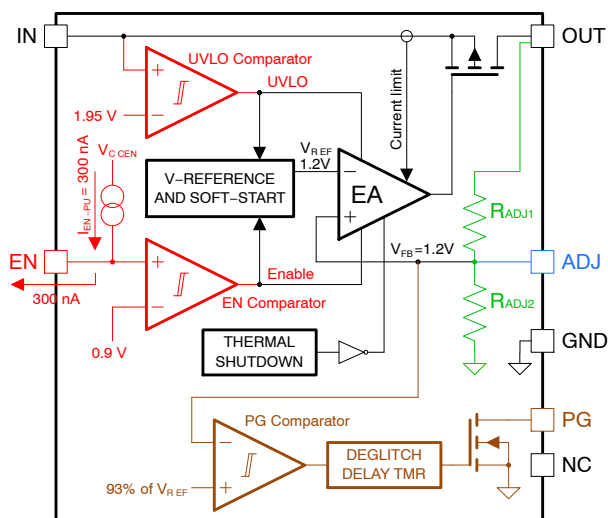
**Figure 60. Internal Block Diagram – EN Pin**

### Startup by IN Pin Voltage

When the LDO is started by IN pin voltage rise, it is turned ON when the voltage is higher than UVLO threshold level. This is the case of both following application circuits, the first one with EN pin floating and the second one with EN pin connected to IN pin.

When the EN pin is floating (left unconnected) its voltage, after the LDO is powered, rises to $V_{CCEN}$ level (2.5 V – 4.5 V, $V_{IN}$ dependent) as the internal current source pulls the pin voltage up. $V_{CCEN}$ voltage level on EN pin is higher than EN comparator threshold so the LDO is turned ON.
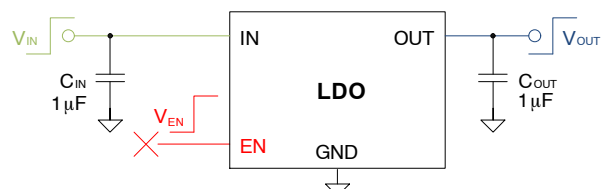


**Figure 61. Circuit – Floating EN Pin**
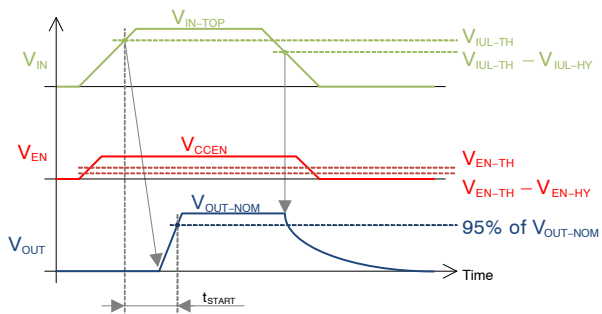


**Figure 62. Startup Timing – Floating EN Pin**

It is also possible to connect EN pin directly to IN pin in the whole input voltage range. The startup sequence is very similar to previous case, the only difference is that the EN pin voltage is not clamped to $V_{CCEN}$ level but it is the same as $V_{IN}$ voltage.
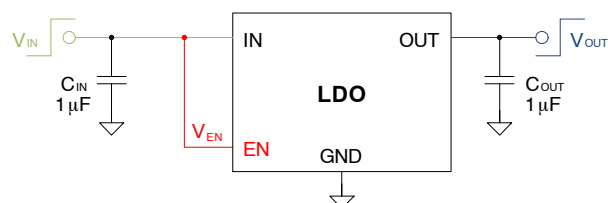


**Figure 63. Circuit – EN Pin Connected to IN Pin**
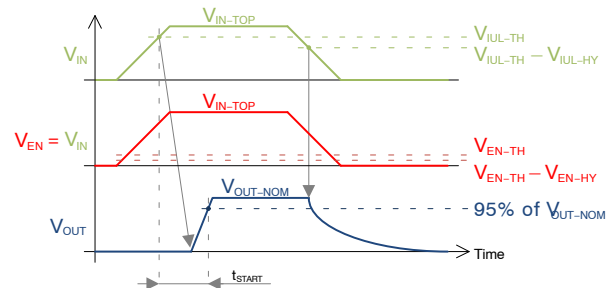


**Figure 64. Startup Timing – EN Pin Connected to IN Pin**

Startup time in both cases above is measured from the point where IN pin voltage reaches $V_{IUL-TH}$ value to point when OUT pin voltage reaches 95% of its nominal value.

The reason why the LDO is started by the UVLO signal and not by the enable signal is the fact that the UVLO signal turns to valid state later then the enable. (EN pin voltage reaches the $V_{EN-TH}$ level prior the IN pin voltage reaches the $V_{IUL-TH}$ level).

### Startup by EN Pin Voltage

When $V_{IN}$ voltage in the application is settled above the $V_{IUL-TH}$ level and control voltage to the EN pin is applied, the level higher than $V_{EN-TH}$ enables the LDO and the level lower than ($V_{EN-TH} - V_{EN-HY}$) disables it.

Startup time is measured from point where $V_{EN}$ voltage reaches $V_{EN-TH}$ value to point when $V_{OUT}$ voltage reaches 95% of its nominal value.
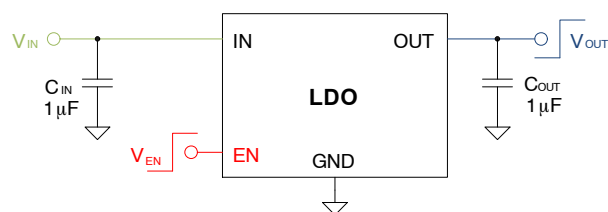


**Figure 65. Circuit – LDO Controlled by $V_{EN}$**



**Figure 66. Timing – $V_{EN}$ Startup**

**Startup by IN Pin Voltage − Delayed**

The startup time triggered by IN pin voltage rise could be delayed by adding of EN pin capacitor ($C_{EN}$). The startup sequence is following − after the $V_{IN}$ voltage is applied, the charging of $C_{EN}$ capacitor by internal pull-up current ($I_{EN-PU}$) is started. When the $C_{EN}$ capacitor voltage ($V_{CEN}$) reaches EN comparator's threshold voltage ($V_{EN-TH}$) the LDO is enabled. Charging of $C_{EN}$ continues up to the $V_{CCEN}$ level (2.5 V − 4.5 V, $V_{IN}$ dependent) wi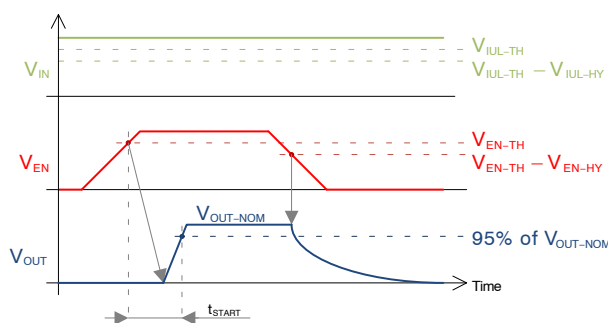th no following effect. The steepness of the LDO's output voltage rise (soft-start time) is not affected by using of $C_{EN}$ capacitor. The additional delay time ($t_{CEN-DELAY}$) could be computed by:

$$t_{CEN-DELAY} = C_{EN} \cdot \frac{V_{EN-TH}}{I_{EN-PU}} = C_{EN} \cdot \frac{0.9\ V}{300\ nA} \quad \text{(eq. 2)}$$

The total startup time ($t_{START-CEN}$) with connected $C_{EN}$ capacitor is a sum of normal startup time ($t_{START}$) and additional delay time caused by $C_{EN}$ capacitor ($t_{CEN-DELAY}$):

$$t_{START-CEN} = t_{START} + t_{CEN-DELAY} \quad \text{(eq. 3)}$$

Value of the $C_{EN}$ capacitor could be in range from 0 to several microfarads. Capacitor's leakage current must be negligible to internal pull-up current $I_{EN-PU}$, otherwise the charging will be affected and adding of $R_{EN}$ resistor from IN to EN pin will be needed.
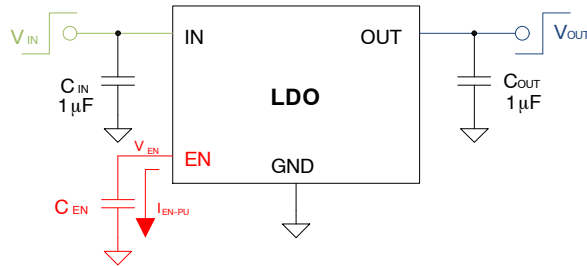


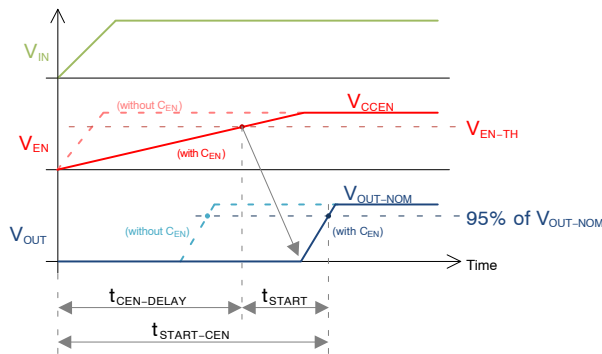**Figure 67. Circuit − $C_{EN}$ Delayed $V_{IN}$ Startup**



**Figure 68. Timing − $C_{EN}$ Delayed $V_{IN}$ Startup**

**Startup by Transistor at EN Pin**

If the LDO needs to be controlled by transistor or generally by open collector / open drain circuit as shown at the next picture, the control behavior is inverted. High control signal makes the EN pin voltage low and low control

signal makes it high because the transistor is connected as signal invertor.

In this application we need to care about transistor's leakage current which must be negligible compared to the internal pull-up current $I_{EN-PU} = 300\ nA$ otherwise additional pull-up resistor $R_{EN}$ will be needed. The maximum value of the EN resistor $R_{EN-MAX}$ is computed from maximal external transistor leakage current (over desired temperature range) $I_{T-LK-MAX}$ and minimal input voltage $V_{IN-MIN}$:

$$R_{EN-MAX} = \frac{V_{IN-MIN}}{I_{T-LK-MAX}} \quad \text{(eq. 4)}$$

For safe, select the EN resistor value $R_{EN}$ lower enough to computed $R_{EN-MAX}$.

When $R_{EN}$ is used the overall application shutdown current is increased because the current through $R_{EN}$ resistor ($I_{REN}$) is added to input shutdown current of the LDO ($I_{SD(LDO)}$). The total application shutdown current ($I_{SD(TOT)}$) is:

$$I_{SD(TOT)} = I_{SD(LDO)} + I_{REN} \quad \text{(eq. 5)}$$

$$I_{REN} = \frac{\left(V_{IN} - V_{T-DS}\right)}{R_{EN}}$$

Where $V_{T-DS}$ is the drain to source voltage of the transistor (given by $R_{DSON}$ and $I_{REN}$).

The overall application quiescent current when $R_{EN}$ is used is influenced only by the transistor's leakage current $I_{T-LK}$.

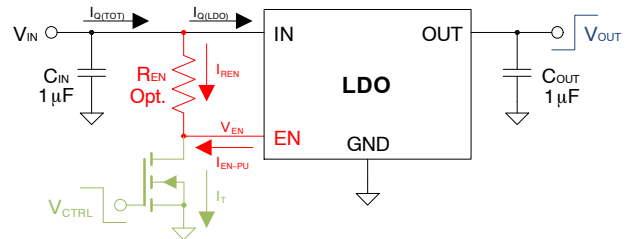$$I_{Q(TOT)} = I_{Q(LDO)} + I_{T-LK} \quad \text{(eq. 6)}$$
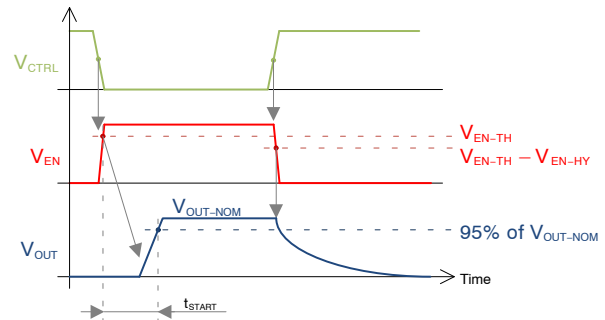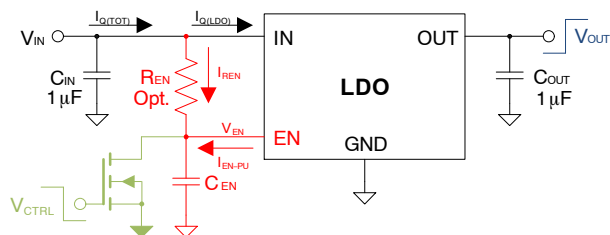


**Figure 69. Circuit − EN Pin Controlled by Transistor**



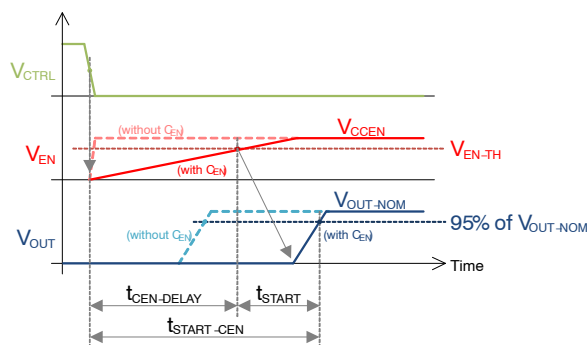**Figure 70. Startup Timing − EN Pin Controlled by Transistor**

**Startup by Transistor at EN Pin – Delayed**

The startup time triggered by EN pin voltage rise, could be delayed the same way as IN pin triggered startup, by adding of $C_{EN}$ capacitor. The startup sequence is following – when the external NMOS control voltage ($V_{CTRL}$) is high the $C_{EN}$ capacitor connected to the EN pin is shorted to GND and LDO is disabled. After the $V_{CTRL}$ is turned low the charging of $C_{EN}$ capacitor by the internal pull-up current source ($I_{EN-PU}$) starts. When the $C_{EN}$ capacitor voltage ($V_{CEN}$, which is the $V_{EN}$ in fact) reaches EN comparator's threshold voltage ($V_{ENTH}$) the LDO is enabled. Charging of $C_{EN}$ then continues up to the $V_{CCEN}$ level (2.5 V – 4.5 V, $V_{IN}$ dependent) with no following effect. The steepness of the LDO's output voltage rise (soft-start time) is not affected by using of $C_{EN}$ capacitor. The additional delay time ($t_{CEN-DELAY}$) could be computed by eq. 2 and the total delayed startup time with $C_{EN}$ capacitor ($t_{START-CEN}$) by eq. 3. What has been said about the $C_{EN}$ capacitor selection at previous paragraphs is applicable here as well.

Also in this application we need to care about transistor's leakage current which must be negligible compared to the internal pull-up current $I_{EN-PU} = 300$ nA otherwise additional pull-up resistor $R_{EN}$ will be needed. Same rules and computations as stated in previous paragraph about $R_{EN}$ are applicable here. Note that $R_{EN}$ would influence the speed of $C_{EN}$ capacitor charging.



**Figure 71. Circuit – EN Pin with $C_{EN}$ Controlled by Transistor**



**Figure 72. Startup Timing – EN Pin with $C_{EN}$ Controlled by Transistor**

**Enable Input as Inaccurate IN Pin UVLO**

The EN input pin on NCV8730 device is specified by threshold voltage and hysteresis both with minimum and maximum value, what allows using EN comparator as adjustable input voltage UVLO function. To set the $V_{IN}$

UVLO threshold value, the external resistor divider from IN pin to EN pin, is needed.

Note that the specification of EN pin threshold voltage (0.7 V to 1.05 V over full operating temperature range) is not as precise as threshold voltage on dedicated UVLO devices. The reason is the EN circuit has to have ultra-low current consumption (NCV8730 $I_{SHDN}$ is 350 nA typ. even while $I_{EN-PU}$ is 300 nA typ. so EN comparator is powered by less than 50 nA typ.). We need to count with that when thinking about the IN pin UVLO design. Below is the application example to show what precision we can get.
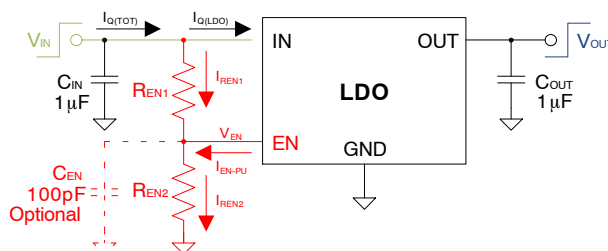


**Figure 73. Circuit – IN Voltage UVLO by EN Pin**

The two main equations for IN pin threshold computation are:

$$R_{EN1} = \frac{V_{IN-UVLO-TH} - V_{EN-TH}}{I_{REN1}} \quad \text{(eq. 7)}$$

$$R_{EN2} = \frac{V_{EN-TH}}{I_{REN1} + I_{EN-PU}}$$

From that, we can get:

$$V_{IN-UVLO-TH} = V_{EN-TH} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - R_{EN1} \cdot I_{EN-PU} \quad \text{(eq. 8)}$$

We can see that IN pin UVLO threshold is EN pin threshold multiplied by the resistor divider ratio as expected but it is unwillingly affected by $I_{EN-PU}$ pull-up current. As the $I_{EN-PU}$ current could vary up to the 1 μA max., we need to choose the $I_{REN1}$ current several times higher to make the $I_{EN-PU}$ influence negligible. The good practice could be to choose $I_{REN1}$ at least 10-times higher than $I_{EN-PU}$ (the bigger the better for the accuracy).

An optional component in this application is $C_{EN}$ capacitor. Its main function is filtering out the spurious signals coming from IN power supply and the minor function is to delay the startup as described in section before. The value of $C_{EN}$ for filtering purpose could be in range from 10 pF to 10 nF. The time constant of this filter is given by:

$$t_{FILTER} = C_{EN} \cdot \frac{R_{EN1} \cdot R_{EN2}}{R_{EN1} + R_{EN2}} \quad \text{(eq. 9)}$$

The side effect of the UVLO divider is increased overall power consumption. At no load state, the quiescent current $I_{Q(TOT)}$ of the application is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} \quad \text{(eq. 10)}$$

So if we select the $I_{REN1}$ value at least 10-times higher than $I_{EN-PU-MAX}$ (1 μA), then the UVLO divider current is

almost 10-times higher than typical LDO's quiescent current (1.3 μA).

IN voltage UVLO application example:

Desired $V_{OUT}$ voltage is 5 V, the LDO's input voltage in normal state is 12 V. We want to turn-off the LDO's output voltage when input voltage is below 10 V (max.).

First, choose the $I_{REN1}$ current as 10-times the maximum $I_{EN-PU}$ current:

$$I_{REN1} = 10 \cdot I_{EN-PU} = 10 \cdot 1 \text{ μA} = 10 \text{ μA} \quad \text{(eq. 11)}$$

Then, to obtain $R_{EN1}$ and $R_{EN2}$ values for maximal $V_{IN-UVLO-TH} = 10$ V, we need to put maximum value of $V_{EN-TH}$ (1.05 V) and minimum value of $I_{EN-PU}$ (0 μA) into the equations for $R_{EN1}$ and $R_{EN2}$:

$$\text{(eq. 12)}$$
$$R_{EN1} = \frac{V_{IN-UVLO-TH} - V_{EN-TH}}{I_{REN1}} = \frac{10\text{ V} - 1.05\text{ V}}{10 \text{ μA}} = 895 \text{ kΩ}$$

$$R_{EN2} = \frac{V_{EN-TH}}{I_{REN1} + I_{EN-PU}} = \frac{1.05}{10 \text{ μA} + 0 \text{ μA}} = 105 \text{ kΩ}$$

The resulting $V_{IN-UVLO-TH}$ limits will be:

$$\text{(eq. 13)}$$
$$V_{IN-UVLO-TH-MIN} = V_{EN-TH-MIN} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - R_{EN1} \cdot I_{EN-PU-MAX}$$

$$V_{IN-UVLO-TH-MIN} = 0.7 \cdot \left(1 + \frac{895 \text{ kΩ}}{105 \text{ kΩ}}\right) - 895 \text{ kΩ} \cdot 1 \text{ μA}$$

$$V_{IN-UVLO-TH-MIN} = 5.77 \text{ V}$$

$$V_{IN-UVLO-TH-MAX} = V_{EN-TH-MAX} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - R_{EN1} \cdot I_{EN-PU-MIN}$$

$$V_{IN-UVLO-TH-MAX} = 1.05 \cdot \left(1 + \frac{895 \text{ kΩ}}{105 \text{ kΩ}}\right) - 895 \text{ kΩ} \cdot 0 \text{ μA}$$

$$V_{IN-UVLO-TH-MAX} = 10.0 \text{ V}$$

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} = 1.3 \text{ μA} + 10 \text{ μA} = 11.3 \text{ μA}$$

When higher $I_{REN1}$ is selected the $V_{IN-UVLO-TH-MIN}$ would be slightly near the target value, the $V_{IN-UVLO-TH-MAX}$ would stay the same but the $I_{Q(TOT)}$ would be significantly higher:

$$I_{REN1} = 100 \cdot I_{EN-PU} = 100 \cdot 1 \text{ μA} = 100 \text{ μA} \quad \text{(eq. 14)}$$

We would get:

$$R_{EN1} = 89.5 \text{ kΩ} \quad \text{(eq. 15)}$$

$$R_{EN2} = 10.5 \text{ kΩ}$$

$$V_{IN-UVLO-TH-MIN} = 6.58 \text{ V}$$

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} = 1.3 \text{ μA} + 100 \text{ μA} = 101.3 \text{ μA}$$

We can see the IN pin UVLO threshold precision computed above (5.77 V or 6.58 V min. / 10.0 V max.) is not too high because the EN pin threshold and EN pin internal pull-up current specifications are not so tight as on dedicated UVLO devices but at some applications this precision could fit the needs.

**Output Current Limit**

Output current is internally limited to 280 mA typ. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is 90% of $V_{OUT-NOM}$). If the output voltage is shorted to ground, the device continues with current limitation at the same current level. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Minimal output current limit value is 200 mA what could be used to cover current demand peaks, higher than the LDO's nominal output current (150 mA).

**Inrush Current**

At every application, the startup sequence needs a special care because during power-up the bypass capacitors connected to the power rail are charged from zero to input voltage level, what generates a current spike, so called inrush current. The size of such current spike depends on the voltage transient slope (the faster the bigger spike), on the total impedance of the loop from the power source to bypass capacitor (traces impedance, power source internal impedance and capacitor impedance; the lower the bigger spike) and on the capacitor value (the higher the bigger spike).

This inrush current during startup could cause power source's overcurrent event, damage of PCB traces, power line fuses blowing or spurious signal generation in surrounding application parts.

For a simplified case when total impedance between input power source and bypass capacitor is zero, we can use following equation to compute the inrush current, based just on voltage transient slope (dV/dt) and the capacitor value:

$$i_{INRUSH} = C \cdot \frac{dV}{dt} \quad \text{(eq. 16)}$$

Example – when the voltage changes from 0 V to 24 V in 10 μs and bypass capacitor is 10 μF, the inrush current is:

$$i_{INRUSH} = 10 \text{ μF} \cdot \frac{24 \text{ V} - 0 \text{ V}}{10 \text{ μs}} = 24 \text{A} \quad \text{(eq. 17)}$$

Of course, this is the worst case when impedances in the circuit are zero, but it shows why we need to care about startup and what defines the inrush current value. We can see the inrush current is lower when capacitance and voltage change are smaller or transition time is longer.

In most cases, the capacitor value and the input voltage change are defined by the application so then the only thing we can do is to slow down the input voltage transition time. We can do it directly by changing input voltage rise time by soft-start circuit (related to Equation 16) or indirectly by adding a current limit block, which in combination with the capacitor will do the same (slower the input voltage rise), see the following equation:

$$t_{START} = C \cdot \frac{dV}{I_{LIMIT}} \quad \text{(eq. 18)}$$

We see that voltage transition time ($t_{START}$) is given by bypass capacitor value (C), by the voltage change (dV) and by current limit value ($I_{LIMIT}$) of added current limit block.

Now back to LDO application. Here we can see two different inrush current spikes. The first one is caused by the LDO's input capacitor ($C_{IN}$) charging from zero to the input voltage level. It happens when the previous power block (for example DC/DC) starts providing the input voltage to the LDO circuit. The maximum level of this inrush current is given by Equation 16. It doesn't matter if LDO is enabled or disabled as this inrush current spike is related only to $C_{IN}$ and it can't be suppressed by the LDO, it is matter of previous power block. This inrush current spike is shown at Figure 75, point (1).

The second inrush current spike is generated by the LDO's output capacitor ($C_{OUT}$) charging from zero to nominal output voltage level. It happens when the LDO is enabled by any way (by driving EN pin or by internal UVLO when EN pin is connected to IN pin). This inrush current is limited by the LDO's soft-start and current limit functions.

Soft-start function limits the speed of the output voltage rise to avoid possible latch-up of application circuit caused by high dV/dt what naturally suppresses input inrush current (related to Equation 16).

The current limit function, used to guard the LDO and application against the overcurrent, is also used during the LDO's startup to limit the input inrush current.

Now focus onto the NCV8730 device. At the next picture we can see both, soft-start and current limit functions have been implemented, shown in red. At this device, the startup current limit level is the same as the normal operation current limit level (specified at the parametric table).
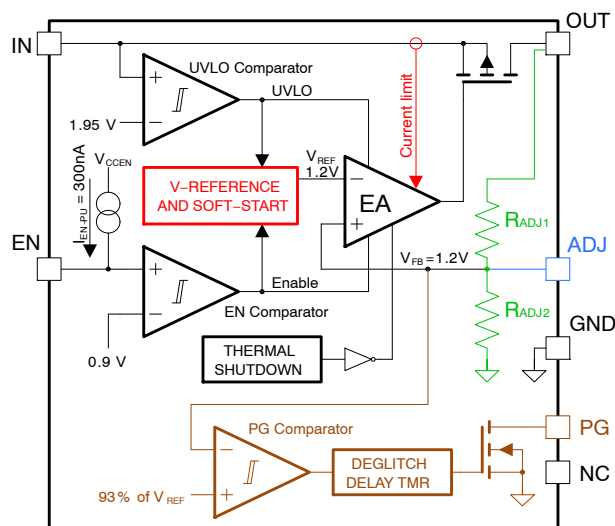


**Figure 74.**

A few practical notes. If the LDO's output capacitor value is small (for example 1 μF), then soft-start limited output voltage rise is slow enough to suppress the inrush current (output capacitor charging current, generated by $dV_{OUT}/dt$, based on Equation 16, is significantly smaller than the

current limit value). While at the case of big output capacitor (for example 47 μF), the soft-start time is not slow enough and the input current needs to be limited by the current limit function.

Next picture shows both startup cases – with small (1 μF) and big (47 μF) output capacitors. Startup is caused by IN voltage rise, EN pin is connected to IN pin and device voltage version is 5.0 V.
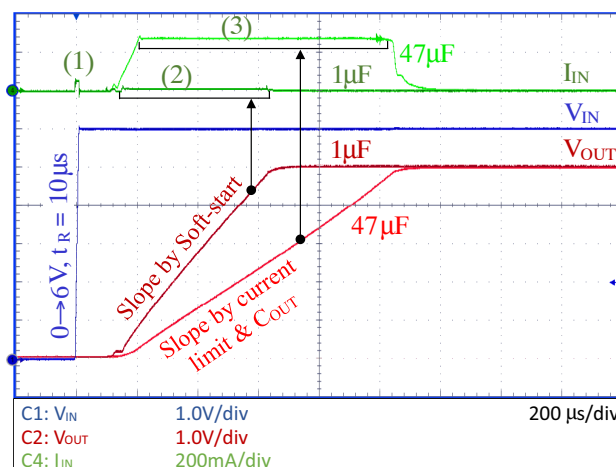


**Figure 75.**

With the $C_{OUT} = 1$ μF, the inrush current (seen at $I_{IN}$ signal at point-2) is almost zero, its level is defined by soft-start time which is about 550 μs (from the picture).

$$i_{INRUSH} = C_{OUT} \cdot \frac{\Delta V_{OUT}}{t_{START}}$$

(eq. 19)

$$i_{INRUSH-1\mu F} = 1 \text{ μF} \cdot \frac{5 \text{ V} - 0 \text{ V}}{550 \text{ μs}} = 9 \text{ mA}$$

With the $C_{OUT} = 47$ μF, the inrush current should be 47-times higher than in case of 1 μF:

$$i_{INRUSH-47\mu F} = 47 \text{ μF} \cdot \frac{5 \text{ V} - 0 \text{ V}}{500 \text{ μs}} = 470 \text{ mA}$$   (eq. 20)

Therefore, in this case the current limit is activated and limits the $C_{OUT}$ charging current to about 280 mA (from the picture, point-3). This leads to enlarging of startup time to:

$$t_{START} = C_{OUT} \cdot \frac{\Delta V_{OUT}}{I_{LIMIT}}$$

(eq. 21)

$$t_{START} = 47 \text{ μF} \cdot \frac{5 \text{ V} - 0 \text{ V}}{270 \text{ mA}} = 870 \text{ μs}$$

One additional thing could be seen at the picture above and it is a small current spike highlighted as a point-1 at the $I_{IN}$ curve. It is the inrush current caused by input voltage transient (from 0 V to 6 V in 10 μs) and input capacitor $C_{IN} = 100$ nF. As stated before, for this current spike is responsible the prior power source, not the LDO (in this case the test equipment which generates the $V_{IN}$ transient). The $C_{IN}$ inrush current amplitude is:

$$i_{INRUSH\_POINT-1} = 100 \text{ nF} \cdot \frac{6 \text{ V} - 0 \text{ V}}{10 \text{ μs}} = 60 \text{ mA}$$   (eq. 22)

**Power Supply Rejection Ratio**

The LDO features high power supply rejection ratio even it is very low quiescent current device. See the Typical characteristics section for the graphs over different conditions.

The PSRR at higher frequencies (from about 100 kHz) can be tuned by the selection of $C_{OUT}$ capacitor, applied input voltage and proper PCB layout (minimizing impedance from load to $C_{OUT}$).

**PG Output**

Version B of the NCP730 device contains PG circuit for the $V_{OUT}$ voltage level monitoring. Internally it is combined from PG comparator, deglitch/delay timer and output NMOS transistor (highlighted by red color at picture below). At both, ADJ and FIX versions, the PG comparator compares internal feedback signal voltage ($V_{FB}$) with the 93% of $V_{REF}$ (typ.) what makes the function independent to the output voltage absolute value (it always compares set $V_{OUT}$ with 93% of its nominal value).

If PG is used at ADJ device version and CFF capacitor is used as well, then $C_{FF}$ must be small enough (10 − 33 pF when R1, R2 are in range of hundreds of kilo ohms) otherwise the PG output will show "power ok state" sooner than the output voltage reaches the PG threshold value. It is because the $C_{FF}$ slows down the output voltage rise time while ADJ pin voltage, what is the PG comparator input, remains fast. Note that any AC voltage change at OUT pin goes into ADJ pin through the $C_{FF}$ (what is the main reason of $C_{FF}$ in fact − to speed up regulator reactions), but for PG operation it makes this kind of issue that voltage at ADJ pin is already on the target level ($V_{REF}$) while OUT voltage is still rising. This issue is a natural behavior for any adjustable regulator so it is not an issue just for this particular device.
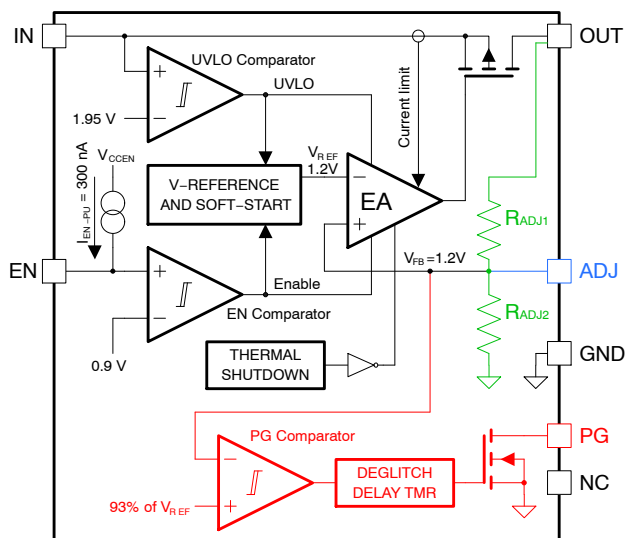


Note: Blue objects are valid for ADJ version
Green objects are valid for FIX version
Red objects are valid for B version (with PG)

**Figure 76. Power Good Output Block Diagram**

The PG output turns into high impedance state (Hi-Z) to show "power ok state" when the $V_{OUT}$ voltage rises above the PG threshold level ($V_{PG-TH}$ + $V_{PG-HY}$) after delay time ($t_{PG-DLY}$) and turns into short to GND level to show "power fail state" when the $V_{OUT}$ falls below the level ($V_{PG-TH}$) after deglitch time ($t_{PG-DG}$).

The PG threshold voltage is 93% of $V_{OUT-NOM}$ (typ.) and the hysteresis is 2% of $V_{OUT-NOM}$ (typ.).

Because the PG output is open drain type it needs to be connected by external pull resistor to a voltage level, which defines the PG pin voltage at time when it is in Hi-Z state. It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's $V_{OUT}$ level. Below are the connections examples.
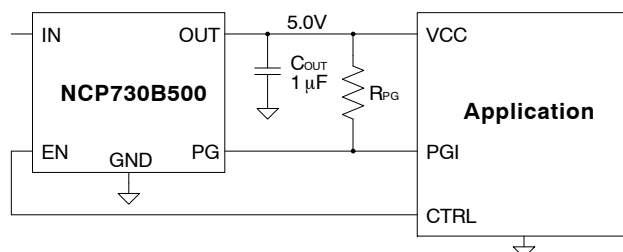


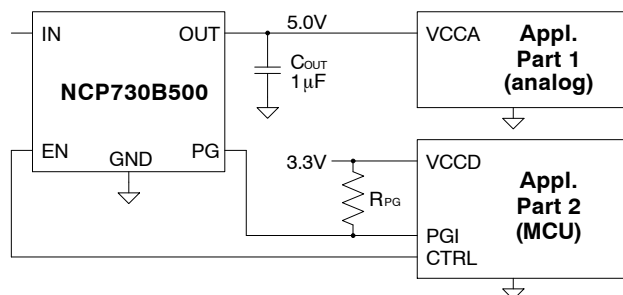**Figure 77. Circuit Example – PG Connected to LDO's Output**



**Figure 78. Circuit Example – PG Connected to Application Power Supply**

Following timing diagrams show the situation when LDO falls out of regulation 3 times (output voltage drops down from nominal value) because of (for example) insufficient IN pin voltage.

Note that the $V_{PG}$ voltage at "power ok state" follows the voltage where the $R_{PG}$ is connected because the PG output is in Hi-Z state and just $R_{PG}$ connection point defines the $V_{PG}$ level. In the first example when $R_{PG}$ is connected to LDO's output, the $V_{PG}$ follows the LDO's $V_{OUT}$ including the drops. In the second example the $R_{PG}$ is connected to LDO independent power rail (3.3 V) so the $V_{PG}$ is not following the LDO's output voltage.
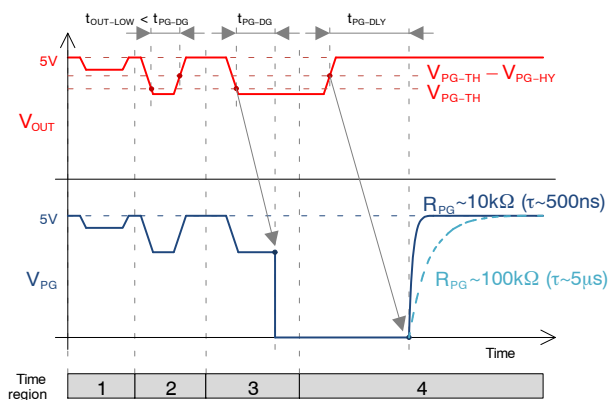
**Figure 79. Timing – PG Connected to LDO's Output**
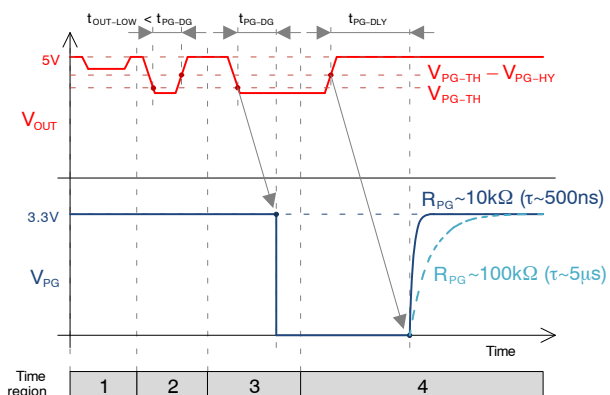


**Figure 80. Timing – PG Connected to Application Power Supply 3.3 V**

The timing diagrams have been divided into 4 time regions to show different situations:

In region-1, the $V_{OUT}$ drop is not deep enough so the PG output shows "power ok state".

In region-2, the $V_{OUT}$ drop is deeper and crosses the $V_{PG-TH}$ threshold level but the duration of the drop is shorter then PG deglitch time ($t_{PG-DG}$ = 160 μs typ.) so the PG output still shows "power ok state". Note that the deglitch time has been intentionally implemented to filter out spurious output voltage drops (caused for example by fast load transients etc.).

In both two first regions the $V_{PG}$ is high and follows the voltage level where the $R_{PG}$ resistor is connected to ($V_{LDO(OUT)}$ or $V_{CCD}$).

In region-3, the $V_{OUT}$ drop is deep enough and the duration is longer then $t_{PG-DG}$ deglitch time so the PG output is shorted to GND pin and shows power fail state.

In region-4, the $V_{OUT}$ returns back to its nominal value. When it crosses the level ($V_{PG-TH} - V_{PG-HY}$) the PG output turns from short to GND into Hi-Z state, not immediately, but after the PG delay time ($t_{PG-DLY}$ = 320 μs typ.). The PG delay ensures that low PG pulse, showing "power fail state", is always longer than the $t_{PG-DLY}$ time and then could be caught by the application circuit (for example by MCU).

**$R_{PG}$ Value Selection**

As shown on the Figure 79 and Figure 80 in the time region-4, the steepness of PG signal return to high level depends on the $R_{PG}$ pull-up resistance (with relation to capacitance of LDO's PG output, parasitic capacitance of PG signal PCB traces and the application circuit PGI input capacitance. The lower $R_{PG}$ resistance the faster PG return to high level.

At the most applications, the PG return speed to high level is not a concern, mainly because of the fact that the LDO already delays the PG return by the $t_{PG-DLY}$ time (320 μs typ.) intentionally so the returning speed itself is negligible.

The next view to the $R_{PG}$ value is the power consumption at "power fail state" when the current from the supply flows through the $R_{PG}$ to the grounded PG pin. This is just a case of the power fail state so probably not a concern too.

At the electrical characteristics table we can find the parameter "PG Output Low Level Voltage ($V_{PG-OL}$)" which defines the drop across the PG internal transistor when it sinks current 1 mA. We can take this current condition (1 mA) as a maximal PG current ($I_{PG-MAX}$) for the $R_{PG-MIN}$ computation (as we know the PG drop at this level, 0.4 V max.). If the application input current $I_{PGI}$ is negligible to $I_{RPG}$ we can compute the $R_{PGI-MIN}$ by:

$$R_{PG-MIN} = \frac{V_{CC-RPG}}{I_{PG-MAX}} \quad \text{(eq. 23)}$$

And, for example, when $R_{PG}$ is connected to 3.3 V power rail:

$$R_{PG-MIN} = \frac{V_{CC-RPG}}{I_{PG-MAX}} = \frac{3.3\ V}{1\ mA} = 3.3\ k\Omega \quad \text{(eq. 24)}$$
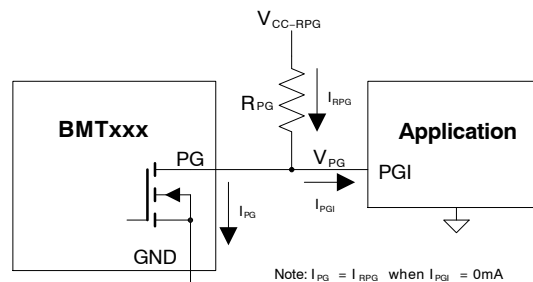


**Figure 81. Circuit Example for $R_{PG}$ Value Selection**

From the opposite side, $R_{PG}$ is limited to its maximum value, based on: maximum PG leakage current $I_{PG-LK-MAX}$, maximum threshold voltage of the application input $V_{PGI-TH-MAX}$ and maximum application input leakage current $I_{PGI-LK-MAX}$. Then:

$$R_{PG-MAX} = \frac{V_{CC-RPG} - V_{PGI-TH-MAX}}{I_{PG-LK-MAX} + I_{PGI-LK-MAX}} \quad \text{(eq. 25)}$$

For example, when $R_{PG}$ is connected to 3.3 V power rail, max. threshold voltage of the application input is 1.3 V and application input leakage current is 3 μA max.:

$$R_{PG-MAX} = \frac{V_{CC-RPG} - V_{PGI-TH-MAX}}{I_{PG-LK-MAX} + I_{PGI-LK-MAX}} \qquad \text{(eq. 26)}$$

$$= \frac{3.3\ V - 1.3\ V}{1\ \mu A + 3\ \mu A} = 500\ k\Omega$$

Based on results above, the $R_{PG}$ value could be selected in range from 3.3 kΩ to 500 kΩ to fit the example application.

**PG and OUT Pin Voltages during Startup/Shutdown**

At the picture below an example of NCP730BMT500 measured startup waveform is shown. EN pin was shorted to IN pin, PG output was connected to OUT pin by resistor $R_{PG}$ = 10 kOhm, OUT was loaded by $R_{LOAD}$ = 50 Ohm, $C_{IN}$ and $C_{OUT}$ were 1 μF both. Slow input voltage rise and fall times have been used to show LDO's overall behavior.

At the point 0 the input voltage starts to rise from 0 to 6 V, LDO is in shutdown (because $V_{IN}$ is below its UVLO threshold) and output voltage is 0 V. At the point 1 the $V_{IN}$ voltage reaches UVLO threshold level and LDO starts charging of output capacitor. $V_{OUT}$ rising speed is defined by internal soft-start function. At the point 2 the $V_{OUT}$

voltage reaches almost the $V_{IN}$ voltage as it rises faster and LDO gets into dropout. The difference between $V_{IN}$ and $V_{OUT}$ is the dropout voltage $V_{DO}$ as shown in the zoomed window. At the point 3 the $V_{OUT}$ reaches PG threshold plus PG hysteresis level ($V_{PG-TH} + V_{PG-HY}$ = 93% + 2% = 95% of $V_{OUT-NOM}$) and from this point LDO counts the power good delay time ($t_{PG-DLY}$). This delay time prolongs the low state of PG signal for easier detection of power fault (it defines minimum PG low time in fact). After this delay, the PG pin rises to high level showing that $V_{OUT}$ is ok. At the point 4 the $V_{OUT}$ reaches its nominal value (5.0 V) as the $V_{IN}$ starts to be higher than ($V_{OUT-NOM} + V_{DO}$) and LDO gets into regulation where it stays until point 5, where the $V_{IN}$ starts to be too low and LDO returns to dropout again. At the point 6 the $V_{OUT}$ drops below the PG threshold level (93% of $V_{OUT-NOM}$) and LDO starts counting the power good deglitch time ($t_{PG-DG}$) which filters fast $V_{OUT}$ undershoots (caused for example by line/load transient responses). After this delay, the PG output is shorted to 0 V level to highlight "power fail" state. At the point 7, the $V_{IN}$ voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.
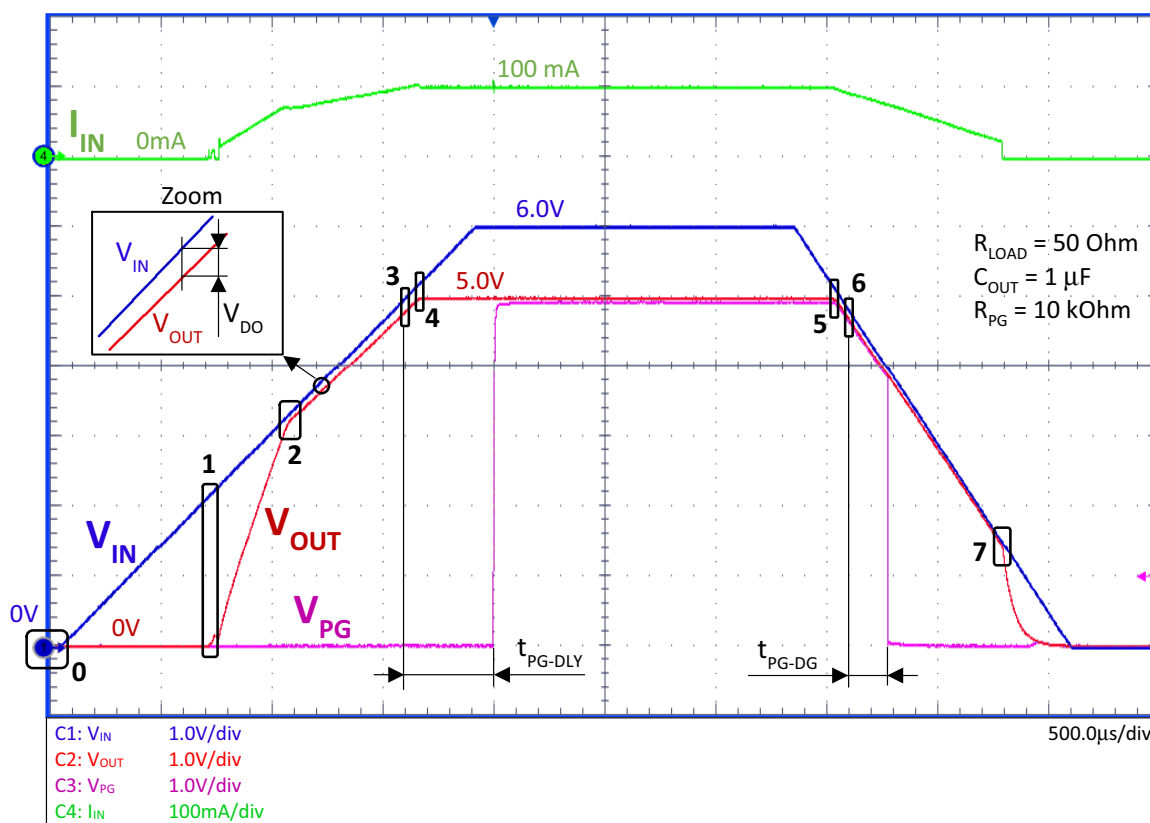


**Figure 82. Startup/Shutdown Example – NCP730BMT500**

**Thermal Shutdown**

When the LDO's die temperature exceeds the thermal shutdown threshold value the device is internally disabled. The IC will remain in this state until the die temperature decreases by the thermal shutdown hysteresis value. Once the IC temperature falls this way, the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

**Power Dissipation**

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} = \frac{125 - T_A}{\theta_{JA}} \text{ [W]} \qquad \text{(eq. 27)}$$

Where: $(T_J - T_A)$ is the temperature difference between the junction and ambient temperatures and $\theta_{JA}$ is the thermal resistance (dependent on the PCB as mentioned above).

For reliable operation junction temperature should be less than +125 °C.

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \text{ [W]} \quad \text{(eq. 28)}$$

Where: $I_{GND}$ is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and NC pin to a large ground planes helps to dissipate the heat from the chip.

The relation of $\theta_{JA}$ and $P_{D(MAX)}$ to PCB copper area and Cu layer thickness could be seen on the Figures 83 and 84.
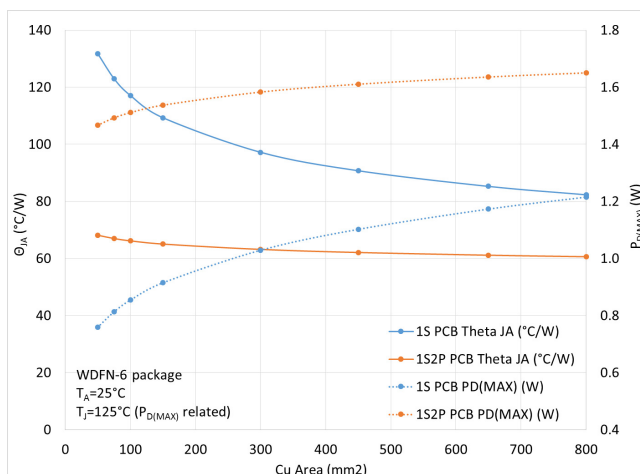


**Figure 83. $\theta_{JA}$ and $P_{D(MAX)}$ vs. Copper Area**
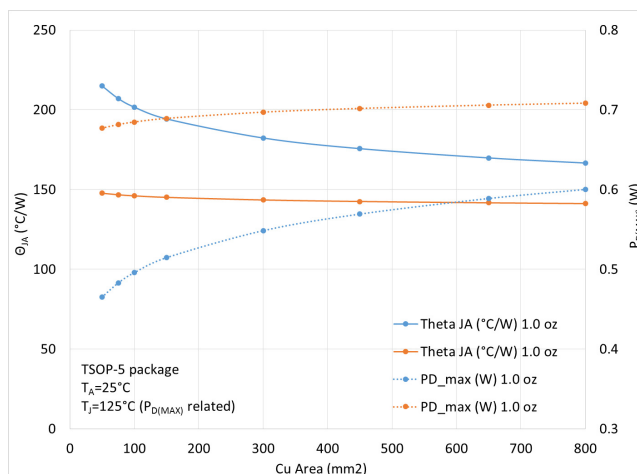


**Figure 84. $\theta_{JA}$ and $P_{D(MAX)}$ vs. Copper Area**
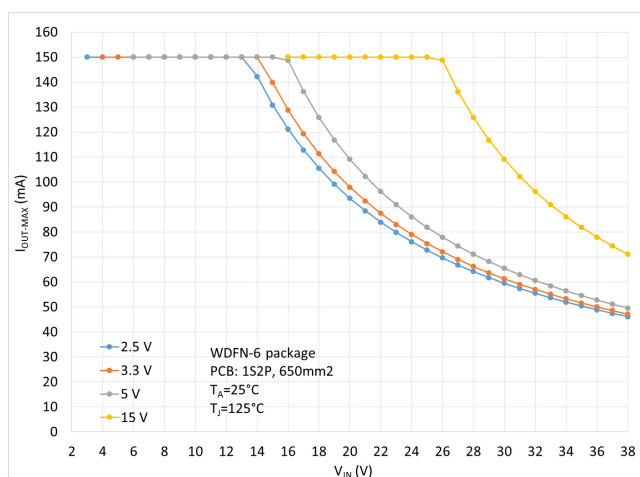


**Figure 85. Maximum Output Current vs. Input Voltage**
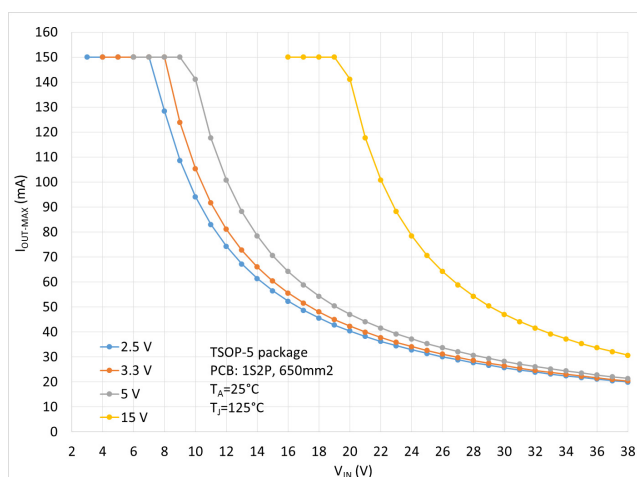


**Figure 86. Maximum Output Current vs. Input Voltage**

**PCB Layout Recommendations**

To obtain good LDO's stability, transient performance and good regulation characteristics place $C_{IN}$ and $C_{OUT}$ capacitors as close as possible to the device pins and make the PCB traces wide, short and place capacitors to the same layer as the LDO is (to avoid connection through vias). The same rules should be applied to the connections between $C_{OUT}$ and the load – the less parasitic impedance the better transients and regulation at the point of load.

To minimize the solution size, use 0402 or 0201 capacitor sizes with appropriate effective capacitance in mind.

Regarding high impedance ADJ pin, prevent capacitive coupling of the trace to any switching signals in the circuitry.

Adequate input power filtering is always a good practice. For load transients the input capacitor value must be high enough to cover the current demands especially if the power source is connected by long traces/wires with high impedance.

**Demo Boards**

Below are the main part of the schematics and top/bottom board layout pictures of the NCV8730 demo boards for various packages. These boards have been used during evaluation to capture the data shown in this datasheet like: transients, PSRR, startups etc. At some of these pictures are shown details of PCB traces surrounding the LDO including $C_{IN}$, $C_{OUT}$, resistor divider $R_1/R_2$, feed forward capacitor $C_{FF}$ and IN/OUT-FORCE/SENSE connections.

Generally, when testing LDOs dynamic performance on demo board which is connected to laboratory power supply typically by long cables, the device needs additional input capacitor. This capacitor covers the voltage drop generated by the load current transients at the impedance of long connection cables (note this is very different to normal application where the distance of the LDO to its power source is short).

Besides the LDO application circuit, each demo board includes some supporting staff, the same at all boards:

- Positions for optional through hole SMB connectors at IN, OUT and EN pins (Molex 73100-0258 or compatible) mainly for line/load transients, PSRR, noise and startup testing the demo board includes.
- Edge connector where all these signal leads too (the appropriate receptacle type is SAMTEC MECF-20-01-L-DV-WT).
- Thermal management circuit (heating transistor and diodes as temperature sensors).
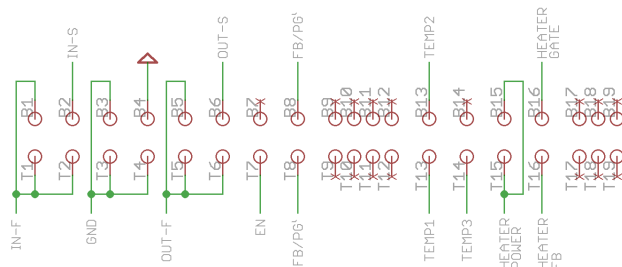


**Figure 87. Edge Connector Pinout (All Demo Boards)**
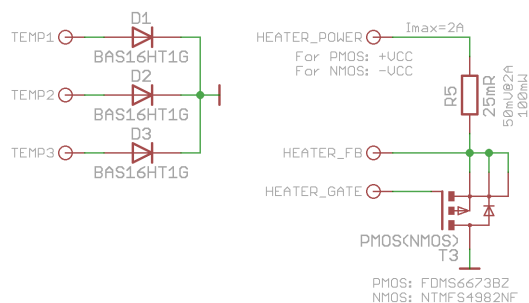


**Figure 88. Thermal Circuit (All Demo Boards)**

**NCV8730ASN/BSN (TSOP-5 package) Demo Board (2 layer PCB, rev. 1)**



| Vout-set | R1 | R2 | Ir1r2 | Suitable for |
|---|---|---|---|---|
| 3.3V | 1.3M | 750k | 1.6uA | -40 to 85 degC |
| 3.3V | 270k | 150k | 7.8uA | -40 to 125 degC |
| 5.0V | 2.4M | 750k | 1.6uA | -40 to 85 degC |
| 5.0V | 470k | 150k | 8.1uA | -40 to 125 degC |
| 15.0V | 10M | 1M/6.8M | 1.38uA | -40 to 85 degC |
| 15.0V | 2.3M | 200k | 6.0uA | -40 to 125 degC |
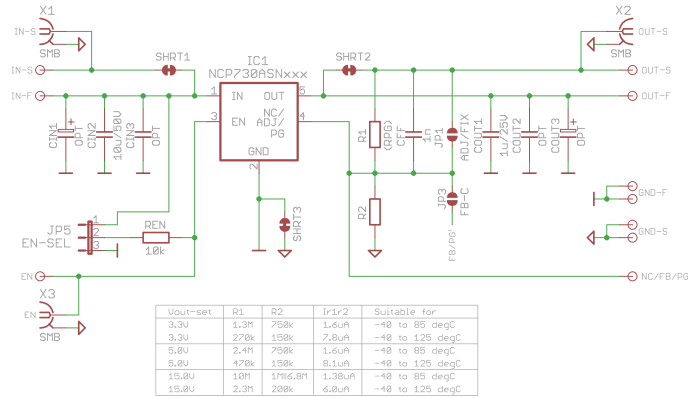
**Figure 89. TSOP-5 Demo Board (2 layer, rev. 1) – Schematics (Main Part)**
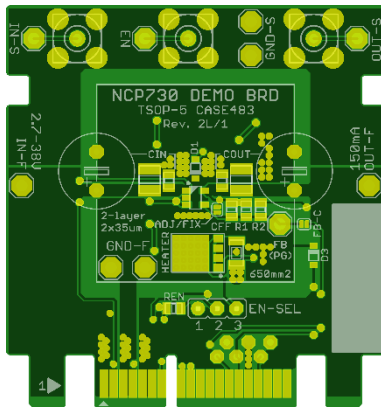


**Figure 90. NCV8730 Demo Board (2 layer, rev. 1) – PCB Top Layer**
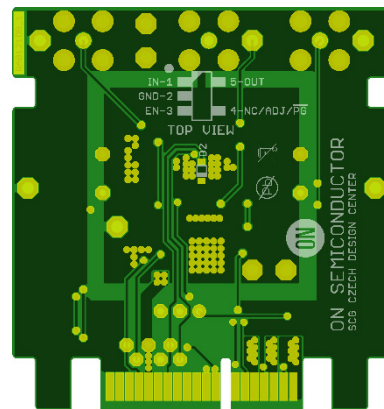


**Figure 91. TSOP-5 Demo Board (2 layer, rev. 1) – PCB Bottom Layer**
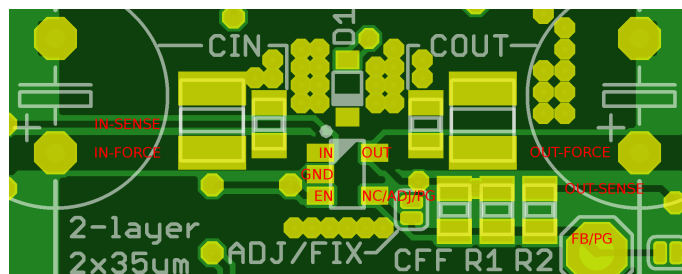


**Figure 92. TSOP-5 Demo Board (2 layer, rev. 1) – PCB Top Layer, Zoomed, Added Signal Labels**

**NCV8730AMT/BMT (WDFN-6 2x2 package) Demo Board (2 layer PCB, rev. 1)**
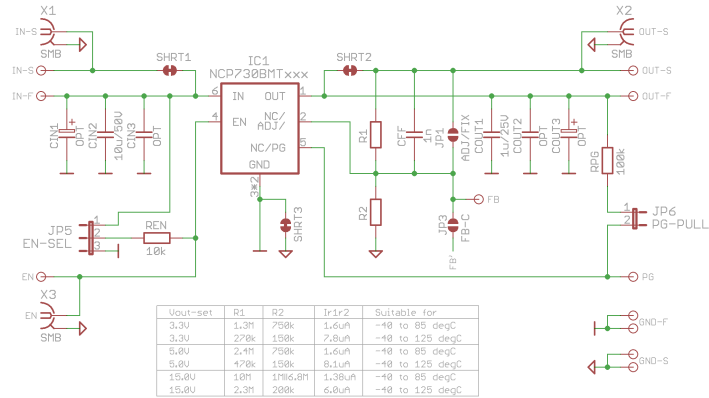


**Figure 93. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – Schematics (Main Part)**
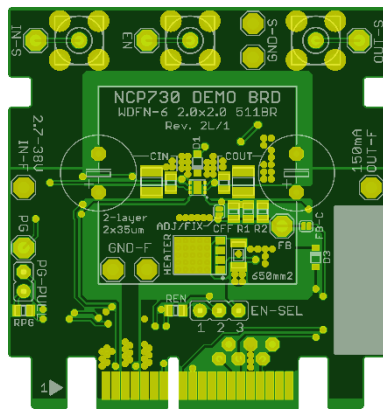


**Figure 94. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Top Layer**
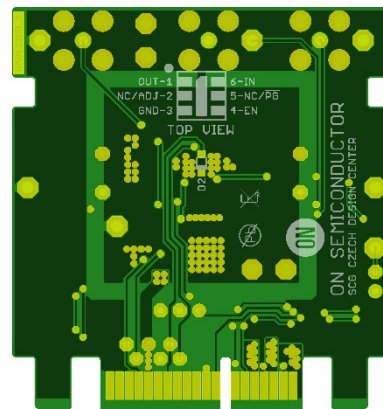


**Figure 95. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Bottom Layer**
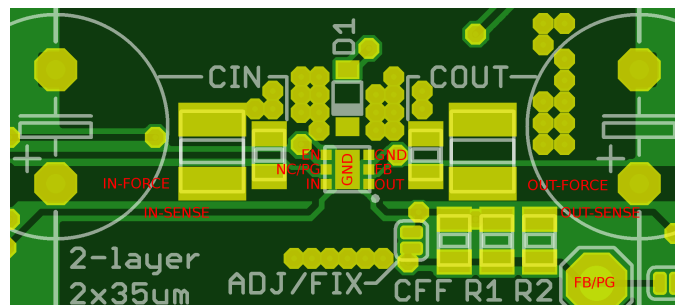


**Figure 96. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Top Layer, Zoomed, Added Signal Labels**

## ORDERING INFORMATION

| Part Number | Marking | Voltage Option ($V_{OUT-NOM}$) | Version | Package | Shipping |
|---|---|---|---|---|---|
| NCV8730ASNADJT1G | PA2 | ADJ | Without PG | TSOP-5 (Pb-Free) | 3000 / Tape & Reel |
| NCV8730ASN180T1G | PAH | 1.8 V | | | |
| NCV8730ASN330T1G | PAE | 3.3 V | | | |
| NCV8730ASN500T1G | PAG | 5.0 V | | | |
| NCV8730BMTWADJTBG | Q2 | ADJ | With PG | WDFNW6 2x2 (Pb-Free) | 3000 / Tape & Reel |
| NCV8730BMTW180TBG | QJ | 1.8 V | | | |
| NCV8730BMTW330TBG | QF | 3.3 V | | | |
| NCV8730BMTW500TBG | QG | 5.0 V | | | |
| NCV8730BMTW1500TBG | QH | 15.0 V | | | |

NOTE: To order any other package, voltage version or PG / non PG variant, please contact your **onsemi** representative.

# NCV8730

**REVISION HISTORY**

| Revision | Description of Changes | Date |
|---|---|---|
| 8 | Revision to adjusted text alignment and formatting for clarity, including bold emphasis on specified sections and added spacing between pin descriptions. <br> Updated pin-4 description to clearly indicate it can be ADJ, PG, or NC depending on the part version (OPN). | 12/09/2025 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.
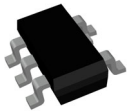
**TSOP−5 3.00x1.50x0.95, 0.95P**
CASE 483
ISSUE P

DATE 01 APR 2024
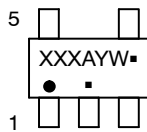
**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

TOP VIEW

SIDE VIEW

DETAIL A

END VIEW

DETAIL "A"
SCALE 2:1

| DIM | MILLIMETERS | | |
|-----|------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.900 | 1.000 | 1.100 |
| A1 | 0.010 | 0.055 | 0.100 |
| A2 | 0.950 REF. | | |
| b | 0.250 | 0.375 | 0.500 |
| c | 0.100 | 0.180 | 0.260 |
| D | 2.850 | 3.000 | 3.150 |
| E | 2.500 | 2.750 | 3.000 |
| E1 | 1.350 | 1.500 | 1.650 |
| e | 0.950 BSC | | |
| L | 0.200 | 0.400 | 0.600 |
| θ | 0° | 5° | 10° |

**GENERIC MARKING DIAGRAM***

**Analog**

XXXAYW▪

**Discrete/Logic**

XXX M▪

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DOCUMENT NUMBER: | 98ARB18753C | | |
|---|---|---|---|
| DESCRIPTION: | TSOP−5 3.00x1.50x0.95, 0.95P | | PAGE 1 OF 1 |

**WDFNW6 2x2, 0.65P**
CASE 511DW
ISSUE B

DATE 15 JUN 2018

SCALE 4:1



PIN ONE REFERENCE

TOP VIEW

DETAIL A

ALTERNATE CONSTRUCTION

DETAIL B

//  0.10  C

⬠ 0.08 C

NOTE 4

SIDE VIEW

SEATING PLANE

SECTION C-C

PLATED SURFACE

DETAIL A

6X L

E2

D2

6X b

⊕ 0.10 C A B
  0.05 C

NOTE 3

BOTTOM VIEW

EXPOSED COPPER

PLATED SURFACE

ALTERNATE CONSTRUCTION

DETAIL B

1.65

6X 0.48

1.65

0.95

2.30

6X 0.35

0.65 PITCH

PACKAGE OUTLINE

RECOMMENDED MOUNTING FOOTPRINT
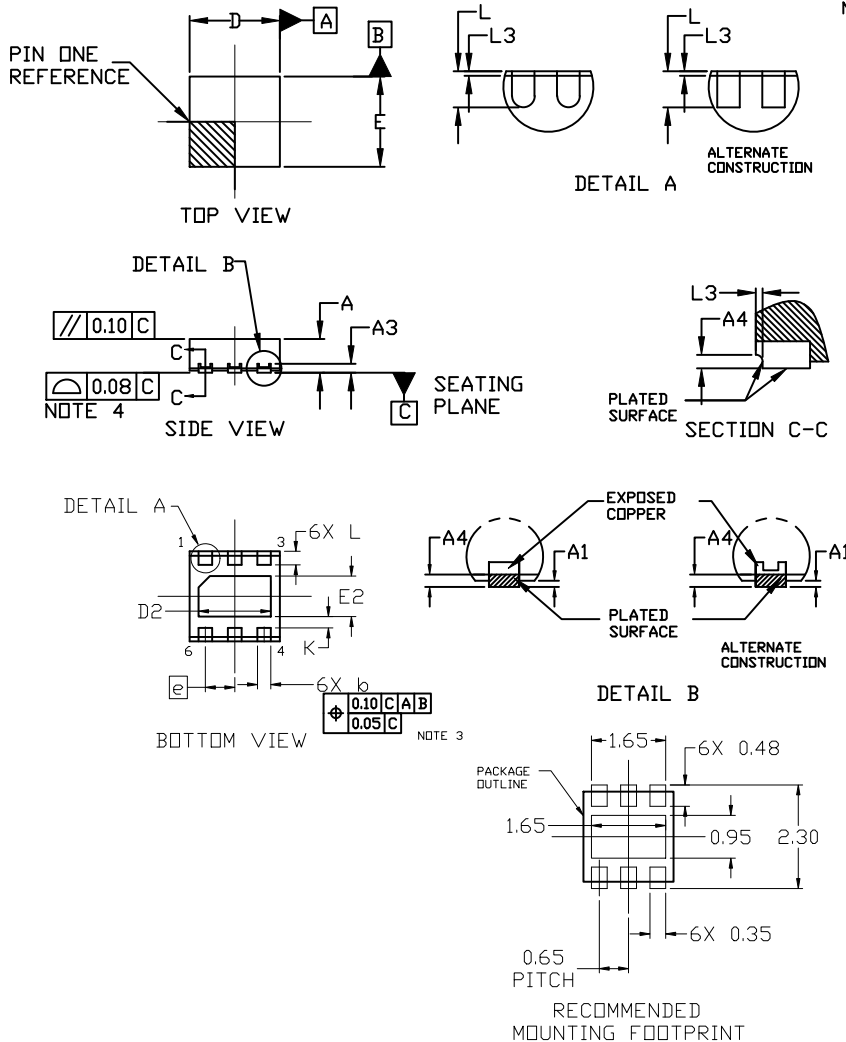
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

| DIM | MILLIMETERS | | |
| --- | --- | --- | --- |
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | --- | --- | 0.05 |
| A3 | 0.20 REF | | |
| A4 | 0.10 | --- | --- |
| b | 0.25 | 0.30 | 0.35 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.50 | 1.60 | 1.70 |
| E | 1.90 | 2.00 | 2.10 |
| E2 | 0.80 | 0.90 | 1.00 |
| e | 0.65 BSC | | |
| K | 0.25 REF | | |
| L | 0.25 | 0.30 | 0.35 |
| L3 | 0.05 REF | | |

## GENERIC MARKING DIAGRAM*

XXM■
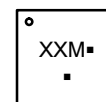
M = Month Code
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■ ", may or may not be present. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON79327G | | |
| --- | --- | --- | --- |
| DESCRIPTION: | WDFNW6 2x2, 0.65P | | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical–documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales

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