NCV8705

500 mA, Ultra-Low Quiescent Current, $I_Q$ 13 μA, Ultra-Low Noise, LDO Voltage Regulator

The NCV8705 is a low noise, low power consumption and low dropout Linear Voltage Regulator. With its excellent noise and PSRR specifications, the device is ideal for use in products utilizing RF receivers, imaging sensors, audio processors or any component requiring an extremely clean power supply. The NCV8705 uses an innovative Adaptive Ground Current circuit to ensure ultra low ground current during light load conditions.

Features
- Operating Input Voltage Range: 2.5 V to 5.5 V
- Available – Fixed Voltage Option: 0.8 V to 3.5 V
  Available – Adjustable Voltage Option: 0.8 V to 5.5 V−$V_{DROP}$
- Reference Voltage 0.8 V
- Ultra−Low Quiescent Current of Typ. 13 μA
- Ultra−Low Noise: 12 μVRMS from 100 Hz to 100 kHz
- Very Low Dropout: 230 mV Typical at 500 mA
- ±2% Accuracy Over Load/Line/Temperature
- High PSRR: 71 dB at 1 kHz
- Internal Soft−Start to Limit the Turn−On Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Active Output Discharge for Fast Turn−Off
- Wettable Flank Package Option Available
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- ADAS, Infotainment & Cluster, and Telematics
- General Purpose Automotive & Industrial
- Building & Factory Automation, Smart Meters

Figure 1. Typical Application Schematic
Figure 2. Simplified Schematic Block Diagrams
Table 1. PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No. – Fixed DFN8/DFNW8</th>
<th>Pin No. – Adjustable DFN8/DFNW8</th>
<th>Pin No. – Fixed WDFN6</th>
<th>Pin No. – Adjustable WDFN6</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>Power supply ground. Expose pad must be tied with GND pin. Soldered to the copper plane allows for effective heat dissipation.</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td>5</td>
<td>4</td>
<td>4</td>
<td>Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.</td>
</tr>
<tr>
<td>IN</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>6</td>
<td>Input pin. A small capacitor is needed from this pin to ground to assure stability.</td>
</tr>
<tr>
<td>N/C</td>
<td>2, 3, 6, 7</td>
<td>2, 6, 7</td>
<td>2, 5</td>
<td>5</td>
<td>Not connected. This pin can be tied to ground to improve thermal dissipation.</td>
</tr>
</tbody>
</table>

Table 2. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (Note 1)</td>
<td>VIN</td>
<td>−0.3 V to 6 V</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VOUT</td>
<td>−0.3 V to VIN + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>Enable Input</td>
<td>VEN</td>
<td>−0.3 V to VIN + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>Adjustable Input</td>
<td>VADJ</td>
<td>−0.3 V to VIN + 0.3 V</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>tSC</td>
<td>Indefinite</td>
<td>s</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>TJ(MAX)</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>TSTG</td>
<td>−55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Human Body Model (Note 2)</td>
<td>ESDHBM</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>ESD Capability, Machine Model (Note 2)</td>
<td>ESMM</td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
   - ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)
   - Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Characteristics, WDFN6 2x2 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Air</td>
<td>( \theta_{JA} )</td>
<td>116.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance Parameter, Junction–to–Board</td>
<td>( \psi_{JB} )</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Thermal Characteristics, DFN8 3x3 mm / DFNW8 3x3 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Air</td>
<td>( \theta_{JA} )</td>
<td>92.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance Parameter, Junction–to–Board</td>
<td>( \psi_{JB} )</td>
<td>35.1</td>
<td></td>
</tr>
</tbody>
</table>

3. Single component mounted on 1 oz, FR 4 PCB with 645 mm² Cu area.
Table 4. ELECTRICAL CHARACTERISTICS
−40°C ≤ TJ ≤ 125°C; V_IN = V_OUT(NOM) + 0.5 V or 2.5 V, whichever is greater; V_EN = 0.9 V, I_OUT = 10 mA, C_IN = C_OUT = 1 μF unless otherwise noted. Typical values are at TJ = +25°C. (Note 4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Input Voltage</td>
<td></td>
<td>VIN</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Range (Adjustable)</td>
<td></td>
<td>V_OUT</td>
<td>0.8</td>
<td>5.5−</td>
<td>V</td>
<td>V_DO</td>
</tr>
<tr>
<td>Undervoltage Lock-out</td>
<td>V_IN rising</td>
<td>UVLO</td>
<td>1.2</td>
<td>1.6</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Accuracy</td>
<td>V_OUT + 0.5 V ≤ V_IN ≤ 5.5 V, I_OUT = 0 – 500 mA</td>
<td>V_OUT</td>
<td>−2</td>
<td>+2</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td></td>
<td>V_REF</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Voltage Accuracy</td>
<td></td>
<td>I_OUT</td>
<td>10 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>V_OUT + 0.5 V ≤ V_IN ≤ 4.5 V, I_OUT = 10 mA</td>
<td>RegLINE</td>
<td>550</td>
<td>750</td>
<td>μV/V</td>
<td></td>
</tr>
<tr>
<td>Load Regulation</td>
<td>I_OUT = 0 mA to 500 mA</td>
<td>RegLOAD</td>
<td>12</td>
<td></td>
<td>μV/mA</td>
<td></td>
</tr>
<tr>
<td>Load Transient</td>
<td>I_OUT = 1 mA to 500 mA or 500 mA to 1 mA in 1 μs, C_OUT = 1 μF</td>
<td>TrnLOAD</td>
<td>±120</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage (Note 5)</td>
<td>I_OUT = 500 mA, V_OUT(NOM) = 2.8 V</td>
<td>VDO</td>
<td>230</td>
<td>350</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Output Current Limit</td>
<td>V_OUT = 90% V_OUT(nom)</td>
<td>I_CL</td>
<td>510</td>
<td>750</td>
<td>950</td>
<td>mA</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td></td>
<td>I_Q</td>
<td>13</td>
<td>25</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Ground Current</td>
<td>I_OUT = 500 mA</td>
<td>I_GND</td>
<td>260</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>V_EN ≤ 0.4 V, TJ = +25°C</td>
<td>I_DIS</td>
<td>0.12</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>V_EN ≤ 0 V, V_IN = 2.0 to 4.5 V, TJ = −40 to +85°C</td>
<td>I_DIS</td>
<td>0.55</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>EN Pin Threshold Voltage</td>
<td>V_EN Voltage increasing</td>
<td>V_EN_HI</td>
<td>0.9</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High Threshold</td>
<td>V_EN Voltage decreasing</td>
<td>V_EN_LO</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Pin Input Current</td>
<td>V_EN = 5.5 V</td>
<td>I_EN</td>
<td>100</td>
<td>500</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>ADJ Pin Current</td>
<td>V_ADJ = 0.8 V</td>
<td>I_ADJ</td>
<td>1</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Turn−On Time</td>
<td>C_OUT = 1.0 μF, from assertion EN pin to 98% V_OUT(nom)</td>
<td>I_ON</td>
<td>150</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>V_IN = 3.8 V, V_OUT = 2.8 V (Fixed), I_OUT = 500 mA</td>
<td>PSRR</td>
<td>73</td>
<td>71</td>
<td>56</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>f = 100 Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 1 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 10 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Noise Voltage</td>
<td>V_OUT = 2.5 V (Fixed), V_IN = 3.5 V, I_OUT = 500 mA</td>
<td>VN</td>
<td>12</td>
<td></td>
<td>μV rms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100 Hz to 100 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Temperature</td>
<td>Temperature increasing from TJ = +25°C</td>
<td>T_SD</td>
<td>160</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>Temperature falling from T_SD</td>
<td>T_SDH</td>
<td>−</td>
<td>20</td>
<td>–</td>
<td>°C</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at TJ = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible. Characterized when V_OUT falls 100 mV below the regulated voltage at V_IN = V_OUT(NOM) + 0.5 V. (Note 4)
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Figure 3. Output Voltage Noise Spectral Density for $V_{\text{OUT}} = 0.8 \text{V}$, $C_{\text{OUT}} = 1 \mu\text{F}$

<table>
<thead>
<tr>
<th>$I_{\text{OUT}}$</th>
<th>RMS Output Noise ($\mu\text{V}$)</th>
<th>10 Hz – 100 kHz</th>
<th>100 Hz – 100 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 mA</td>
<td>19.06</td>
<td>18.21</td>
<td></td>
</tr>
<tr>
<td>100 mA</td>
<td>19.99</td>
<td>15.04</td>
<td></td>
</tr>
<tr>
<td>300 mA</td>
<td>14.42</td>
<td>13.39</td>
<td></td>
</tr>
<tr>
<td>500 mA</td>
<td>13.70</td>
<td>12.60</td>
<td></td>
</tr>
</tbody>
</table>

Figure 4. Output Voltage Noise Spectral Density for $V_{\text{OUT}} = 0.8 \text{V}$, $C_{\text{OUT}} = 10 \mu\text{F}$

<table>
<thead>
<tr>
<th>$I_{\text{OUT}}$</th>
<th>RMS Output Noise ($\mu\text{V}$)</th>
<th>10 Hz – 100 kHz</th>
<th>100 Hz – 100 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 mA</td>
<td>16.17</td>
<td>15.28</td>
<td></td>
</tr>
<tr>
<td>100 mA</td>
<td>16.41</td>
<td>15.65</td>
<td></td>
</tr>
<tr>
<td>300 mA</td>
<td>14.94</td>
<td>14.10</td>
<td></td>
</tr>
<tr>
<td>500 mA</td>
<td>14.08</td>
<td>13.11</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5. Output Voltage Noise Spectral Density for $V_{\text{OUT}} = 3.3 \text{V}$, $C_{\text{OUT}} = 1 \mu\text{F}$

<table>
<thead>
<tr>
<th>$I_{\text{OUT}}$</th>
<th>RMS Output Noise ($\mu\text{V}$)</th>
<th>10 Hz – 100 kHz</th>
<th>100 Hz – 100 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 mA</td>
<td>18.12</td>
<td>15.39</td>
<td></td>
</tr>
<tr>
<td>100 mA</td>
<td>16.42</td>
<td>13.50</td>
<td></td>
</tr>
<tr>
<td>300 mA</td>
<td>16.35</td>
<td>12.47</td>
<td></td>
</tr>
<tr>
<td>500 mA</td>
<td>16.00</td>
<td>12.10</td>
<td></td>
</tr>
</tbody>
</table>
**TYPICAL CHARACTERISTICS**

Figure 6. Output Voltage Noise Spectral Density for $V_{OUT} = 3.3$ V, $C_{OUT} = 10 \mu$F

<table>
<thead>
<tr>
<th>$I_{OUT}$</th>
<th>RMS Output Noise ($\mu$V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mA</td>
<td>17.35 14.07</td>
</tr>
<tr>
<td>100 mA</td>
<td>17.43 14.29</td>
</tr>
<tr>
<td>300 mA</td>
<td>16.55 13.33</td>
</tr>
<tr>
<td>500 mA</td>
<td>16.48 13.20</td>
</tr>
</tbody>
</table>

Figure 7. Output Voltage Noise Spectral Density for Adjustable Version – Different Output Voltage

<table>
<thead>
<tr>
<th>$V_{OUT}$</th>
<th>RMS Output Noise ($\mu$V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5 V</td>
<td>31.40 30.33</td>
</tr>
<tr>
<td>3.3 V</td>
<td>49.14 44.30</td>
</tr>
</tbody>
</table>

Figure 8. Output Voltage Noise Spectral Density for Adjustable Version for Various $C_{1}$

<table>
<thead>
<tr>
<th>$C_{1}$</th>
<th>RMS Output Noise ($\mu$V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>50.17 43.85</td>
</tr>
<tr>
<td>100 pF</td>
<td>46.90 40.39</td>
</tr>
<tr>
<td>1 nF</td>
<td>36.92 27.99</td>
</tr>
<tr>
<td>10 nF</td>
<td>27.02 18.31</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Figure 9. Ground Current vs. Output Current

Figure 10. Ground Current vs. Output Current from 0 mA to 2 mA

Figure 11. Ground Current vs. Output Current at Temperatures

Figure 12. Ground Current vs. Output Current 0 mA to 2 mA at Temperature

Figure 13. Quiescent Current vs. Temperature

Figure 14. Dropout Voltage vs. Output Current at Temperature (2.5 V)
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Figure 15. Dropout Voltage vs. Output Current at Temperatures (3.3 V)

Figure 16. Dropout Voltage vs. Temperature (2.5 V)

Figure 17. Dropout Voltage vs. Temperature, (3.3 V)

Figure 18. Input Voltage vs. Output Voltage

Figure 19. Output Voltage vs. Temperature, (0.8 V)

Figure 20. Output Voltage vs. Temperature, (2.5 V)
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Figure 21. Output Voltage vs. Temperature, (3.3 V)

Figure 22. Line Regulation vs. Temperature, (1.8 V)

Figure 23. Line Regulation vs. Temperature, (3.3 V)

Figure 24. Load Regulation vs. Temperature, (1.8 V)

Figure 25. Load Regulation vs. Temperature, (3.3 V)

Figure 26. Disable Current vs. Temperature
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Figure 27. Enable Current vs. Temperature

Figure 28. Current Limit vs. Temperature

Figure 29. Short-Circuit vs. Temperature

Figure 30. Short-Circuit Current vs. Temperature

Figure 31. Enable Threshold (High)

Figure 32. Enable Threshold (Low)
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Figure 33. Discharge Resistance vs. Temperature

Figure 34. Start-up Time vs. Temperature

Figure 35. Power Supply Rejection Ratio, $V_{OUT} = 1.8$ V

Figure 36. Power Supply Rejection Ratio, $V_{OUT} = 2.8$ V

Figure 37. Power Supply Rejection Ratio, $V_{OUT} = 3.3$ V

Figure 38. Power Supply Rejection Ratio, $V_{OUT} = 3.3$ V, $I_{OUT} = 10$ mA – Different $C_{OUT}$
TYPICAL CHARACTERISTICS

Figure 39. Power Supply Rejection Ratio, $V_{OUT} = 3.3 \, V$, $I_{OUT} = 500 \, mA$ – Different $C_{OUT}$

Figure 40. Power Supply Rejection Ratio, $V_{OUT} = 3.3 \, V$, $I_{OUT} = 500 \, mA$ – Different $C_{OUT}$

Figure 41. Output Capacitor ESR vs. Output Current

Figure 42. Enable Turn–on Response, $C_{OUT} = 1 \, \mu F$, $I_{OUT} = 10 \, mA$

Figure 43. Enable Turn–on Response, $C_{OUT} = 1 \, \mu F$, $I_{OUT} = 500 \, mA$
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Figure 44. Enable Turn–on Response, 
$C_{OUT} = 10 \mu F$, $I_{OUT} = 10 mA$

Figure 45. Enable Turn–on Response, 
$C_{OUT} = 10 \mu F$, $I_{OUT} = 500 mA$

Figure 46. Line Transient Response – Rising 
Edge, $V_{OUT} = 0.8 V$, $I_{OUT} = 10 mA$

Figure 47. Line Transient Response – Falling 
Edge, $V_{OUT} = 0.8 V$, $I_{OUT} = 10 mA$

Figure 48. Line Transient Response – Rising 
Edge, $V_{OUT} = 3.3 V$, $I_{OUT} = 10 mA$

Figure 49. Line Transient Response – Falling 
Edge, $V_{OUT} = 3.3 V$, $I_{OUT} = 10 mA$
TYPICAL CHARACTERISTICS

Figure 50. Line Transient Response − Rising Edge, V\text{OUT} = 3.3 V, I\text{OUT} = 500 mA

Figure 51. Line Transient Response − Falling Edge, V\text{OUT} = 3.3 V, I\text{OUT} = 500 mA

Figure 52. Load Transient Response − Rising Edge, V\text{OUT} = 0.8 V, I\text{OUT} = 1 mA to 500 mA, C\text{OUT} = 1 \mu F, 10 \mu F

Figure 53. Load Transient Response − Falling Edge, V\text{OUT} = 0.8 V, I\text{OUT} = 1 mA to 500 mA, C\text{OUT} = 1 \mu F, 10 \mu F

Figure 54. Load Transient Response − Rising Edge, V\text{OUT} = 0.8 V, I\text{OUT} = 1 mA to 500 mA, t_{\text{RISE, IOUT}} = 10 \mu s, 1 \mu s

Figure 55. Load Transient Response − Falling Edge, V\text{OUT} = 0.8 V, I\text{OUT} = 1 mA to 500 mA, t_{\text{FALL, IOUT}} = 1 \mu s, 10 \mu s

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TYPICAL CHARACTERISTICS

Figure 56. Load Transient Response – Rising Edge, $V_{OUT} = 3.3\, V$, $I_{OUT} = 1\, mA$ to $500\, mA$, $C_{OUT} = 1\, \mu F$, $10\, \mu F$

$V_{IN} = 3.8\, V$
$V_{OUT} = 3.3\, V$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

5 $\mu s$/div

200 mA/div

100 mV/div

$C_{OUT} = 10\, \mu F$
$C_{OUT} = 1\, \mu F$

Figure 57. Load Transient Response – Falling Edge, $V_{OUT} = 3.3\, V$, $I_{OUT} = 1\, mA$ to $500\, mA$, $C_{OUT} = 1\, \mu F$, $10\, \mu F$

$V_{IN} = 3.8\, V$
$V_{OUT} = 3.3\, V$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

50 $\mu s$/div

200 mA/div

50 mV/div

$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

Figure 58. Load Transient Response – Rising Edge, $V_{OUT} = 3.3\, V$, $I_{OUT} = 1\, mA$ to $500\, mA$, $t_{RISE\_IOUT} = 1\, \mu s$, $10\, \mu s$

$V_{IN} = 3.8\, V$
$V_{OUT} = 3.3\, V$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$ (MLCC)

10 $\mu s$/div

200 mA/div

50 mV/div

$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

Figure 59. Load Transient Response – Falling Edge, $V_{OUT} = 3.3\, V$, $I_{OUT} = 1\, mA$ to $500\, mA$, $t_{FALL\_IOUT} = 1\, \mu s$, $10\, \mu s$

$V_{IN} = 3.8\, V$
$V_{OUT} = 3.3\, V$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$ (MLCC)

50 $\mu s$/div

200 mA/div

50 mV/div

$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

Figure 60. Turn–on/off, Slow Rising $V_{IN}$

$V_{IN} = 3.3\, V$
$I_{OUT} = 1\, mA$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$ (MLCC)

5 $ms$/div

600 mV/div

500 mV/div

$C_{OUT} = 1\, \mu F$
$C_{OUT} = 10\, \mu F$

Figure 61. Short–Circuit and Thermal Shutdown

$V_{IN} = 5.5\, V$
$V_{OUT} = 3.3\, V$
$C_{IN} = 1\, \mu F$ (MLCC)
$C_{OUT} = 1\, \mu F$ (MLCC)

20 ms/div

1 V/div

Short–Circuit

Thermal Shutdown

$V_{OUT}$

$V_{IN}$

$I_{OUT}$
**TYPICAL CHARACTERISTICS**

**Figure 62. Short−Circuit Current Peak**

- **VIN = 5.5 V**
- **VOUT = 3.3 V**
- **CIN = 1 μF (MLCC)**
- **COUT = 1 μF (MLCC)**

**Figure 63. Enable Turn−off**

- **VIN = 5.5 V**
- **VOUT = 3.3 V**
- **CIN = 1 μF (MLCC)**
- **COUT = 1 μF (MLCC)**
- **COUT = 10 μF**
- **COUT = 1 μF**
APPLICATIONS INFORMATION

General
The NCV8705 is a high performance 500 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 13 μA of quiescent current at no-load condition. The regulator features ultra-low noise of 12 μVRMS, PSRR of 71 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor. A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (CIN)
It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (COUT)
The NCV8705 requires an output capacitor connected as close as possible to the output pin of the regulator. The minimal capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8705 is designed to remain stable with minimum effective capacitance of 1 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias. Refer to the Figure 64, for the capacitance vs. package size and DC bias voltage dependence.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the COUT but the maximum value of ESR should be less than 900 mΩ. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR as shown in typical characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

No-load Operation
The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Adjustable Operation
The output voltage range can be set from 0.8 V to 5.5 V−VDO by resistor divider network. Use Equations 1 and 2 to calculate appropriate values of resistors and output voltage. Typical current to ADJ pin is 1 nA. For output voltage 0.8 V ADJ pin can be tied directly to Vout pin.

\[ V_{OUT} = 0.8 \cdot \left(1 + \frac{R_1}{R_2}\right) + R_1 \cdot I_{ADJ} \quad \text{(eq. 1)} \]

\[ R_2 \approx \frac{1}{R_1} \cdot \frac{V_{OUT}}{0.8} - 1 \quad \text{(eq. 2)} \]

The resistor divider should be designed carefully to achieve the best performance. Recommended current through divider is 10 μA and more. Too high values of resistors (MΩ) cause increasing noise and longer start-up time. The suggested values of the resistors are in Table 5. To improve dynamic performance capacitor C1 should be at least 1 nF. Recommended range of capacity is between 10 nF and 100 nF. Higher value of capacitor C1 increasing start-up time.

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<thead>
<tr>
<th>VOUT</th>
<th>R1</th>
<th>R2</th>
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<tbody>
<tr>
<td>1.5 V</td>
<td>130k</td>
<td>150k</td>
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<tr>
<td>3.3 V</td>
<td>256k</td>
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<td>5.0 V</td>
<td>430k</td>
<td>82k</td>
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Enable Operation
The NCV8705 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.
If the EN pin voltage > 0.9 V the device is guaranteed to be enabled. The NCV8705 regulates the output voltage and the active discharge transistor is turned-off.
The EN pin has internal pull-down current source with typ. value of 110 nA which assures that the device is turned-off when the EN pin is not connected. Build in 2 mV hysteresis into the EN prevents from periodic on/off oscillations that can occur due to noise.
In the case where the EN function isn’t required the EN should be tied directly to IN.

Undervoltage Lockout
The internal UVLO circuitry assures that the device becomes disabled when the VIN falls below typ. 1.5 V. When the VIN voltage ramps-up the NCV8705 becomes enabled, if VIN rises above typ. 1.6 V. The 100 mV hysteresis prevents from on/off oscillations that can occur due to noise on VIN line.

Output Current Limit
Output Current is internally limited within the IC to a typical 750 mA. The NCV8705 will source this amount of current measured with a voltage drops on the 90% of the nominal VOUT. If the Output Voltage is directly shorted to ground (VOUT = 0 V), the short circuit protection will limit the output current to 800 mA (typ). The current limit and short circuit protection will work properly up to VIN = 5.5 V at TA = 125°C. There is no limitation for the short circuit duration.

Internal Soft–Start circuit
NCV8705 contains an internal soft–start circuitry to protect against large inrush currents which could otherwise flow during the start–up of the regulator. Soft–start feature protects against power bus disturbances and assures a controlled and monotonic rise of the output voltage.

Thermal Shutdown
When the die temperature exceeds the Thermal Shutdown threshold (TSD = 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (TSDU = 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation
As power dissipated in the NCV8705 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.
The maximum power dissipation the NCV8705 can handle is given by:

\[ P_{D(\text{MAX})} = \frac{[T_{J(\text{MAX})} - T_A]}{\theta_{JA}} \]  
\hspace{1cm} (eq. 3)

The power dissipated by the NCV8705 for given application conditions can be calculated from the following equations:

\[ P_D = V_{IN}(I_{GND}@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \]  
\hspace{1cm} (eq. 4)
Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that \( V_{\text{OUT}} > V_{\text{IN}} \). Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Load Regulation

The NCV8705 features very good load regulation of maximum 2 mV in 0 mA to 500 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 50 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.75 mV/V measured from \( V_{\text{IN}} = V_{\text{OUT}} + 0.5 \) V to 5.5 V. For battery operated applications it may be important that the line regulation from \( V_{\text{IN}} = V_{\text{OUT}} + 0.5 \) V up to 4.5 V is only 0.55 mV/V.

Power Supply Rejection Ratio

The NCV8705 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of \( C_{\text{OUT}} \) capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra–low noise output voltage without external noise filter capacitor (\( C_{\text{nr}} \)). Figures 3 – 6 shows NCV8705 noise performance. Generally the noise performance in the indicated frequency range improves with increasing output current.

Turn–On Time

The turn–on time is defined as the time period from \( \text{EN} \) assertion to the point in which \( V_{\text{OUT}} \) will reach 98% of its nominal value. This time is dependent on various application conditions such as \( V_{\text{OUT}}(\text{NOM}), C_{\text{OUT}}, T_A \).

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place \( C_{\text{IN}} \) and \( C_{\text{OUT}} \) capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 4).
## ORDERING INFORMATION

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<th>Marking</th>
<th>Package</th>
<th>Feature</th>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 511BR
ISSUE B

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICES CONTAINING WETTABLE FLANK OPTION, DETAIL A ALTERNATE CONSTRUCTION A-2 AND DETAIL B ALTERNATE CONSTRUCTION B-2 ARE NOT APPLICABLE.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DIMENSIONS: MILLIMETERS

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**PACKAGE DIMENSIONS**

DFN8, 3x3, 0.65P
CASE 506DB
ISSUE A

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS. DIMENSION B APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

PACKAGE DIMENSIONS

DFNW6 3x3, 0.65P
CASE 507AD
ISSUE O

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