NCV8664

Linear Regulator, Low Dropout, Very Low Iq

The NCV8664 is a precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 22 μA.

NCV8664 is pin and functionally compatible with NCV4264 and NCV4264–2, and it could replace these parts when very low quiescent current is required.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features
• 3.3 V, 5.0 V Fixed Output
• ±2.0% Output Accuracy, Over Full Temperature Range
• 30 μA Maximum Quiescent Current at IOUT = 100 μA
• 600 mV Maximum Dropout Voltage at 150 mA Load Current
• Wide Input Voltage Operating Range of 4.5 V to 45 V
• Internal Fault Protection
  ♦ –42 V Reverse Voltage
  ♦ Short Circuit/Overcurrent
  ♦ Thermal Overload
• NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
• EMC Compliant
• These are Pb–Free Devices
Figure 1. Block Diagram

**PIN FUNCTION DESCRIPTION**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPAK/SOT–223</td>
<td>SOIC–8</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>VIN</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>VOUT</td>
</tr>
<tr>
<td>TAB</td>
<td>–</td>
<td>GND</td>
</tr>
<tr>
<td>–</td>
<td>1, 5–8</td>
<td>NC</td>
</tr>
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</table>

**OPERATING RANGE**

<table>
<thead>
<tr>
<th>Pin Symbol, Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, DC Input Operating Voltage</td>
<td>VIN</td>
<td>4.5</td>
<td>+45</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature Operating Range</td>
<td>TJ</td>
<td>–40</td>
<td>+150</td>
<td>°C</td>
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</table>

**MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>VIN, DC Voltage</td>
<td>VIN</td>
<td>–42</td>
<td>+45</td>
<td>V</td>
</tr>
<tr>
<td>VOUT, DC Voltage</td>
<td>VOUT</td>
<td>–0.3</td>
<td>+18</td>
<td>V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>–55</td>
<td>+150</td>
<td>°C</td>
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</table>

ESD Capability, Human Body Model (Note 1) 

<table>
<thead>
<tr>
<th>ESD Capability, Machine Model (Note 1)</th>
<th>VESDHB</th>
<th>4000</th>
<th>–</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Capability, Machine Model (Note 1)</td>
<td>VESDMM</td>
<td>200</td>
<td>–</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC–Q100–002 (EIA/JESD22–A 114C)
   ESD MM tested per AEC–Q100–003 (EIA/JESD22–A 115C)

**THERMAL RESISTANCE**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Junction–to–Ambient</td>
<td>RJA</td>
<td>DPAK SOT–223 SOIC–8 Fused</td>
<td>–</td>
<td>101 (Note 2) 99 (Note 2) 145</td>
<td>°C/W</td>
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<tr>
<td></td>
<td>RJC</td>
<td>DPAK SOT–223 SOIC–8 Fused</td>
<td>–</td>
<td>9.0 17</td>
<td>°C/W</td>
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</table>

2. 1 oz., 100 mm² copper area.
LEAD SOLDERING TEMPERATURE AND MSL

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 3)</td>
<td>T_{sld}</td>
<td>-</td>
<td>265 pk</td>
<td>°C</td>
</tr>
<tr>
<td>Moisture Sensitivity Level</td>
<td>SOT223 DPAK SOIC–8 Fused</td>
<td>MSL</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>-</td>
</tr>
</tbody>
</table>

3. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

ELECTRICAL CHARACTERISTICS (Vin = 13.5 V, TJ = -40°C to +150°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Output Voltage 5.0 V Version</td>
<td>V_{OUT}</td>
<td>0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 6.0 V ≤ Vin ≤ 28 V</td>
<td>4.900</td>
<td>5.000</td>
<td>5.100</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage 5.0 V Version</td>
<td>V_{OUT}</td>
<td>0 mA ≤ I_{OUT} ≤ 150 mA 5.5 V ≤ Vin ≤ 28 V -40°C ≤ TJ ≤ 125°C</td>
<td>4.900</td>
<td>5.000</td>
<td>5.100</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage 3.3 V Version</td>
<td>V_{OUT}</td>
<td>0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 4.5 V ≤ Vin ≤ 28 V</td>
<td>3.234</td>
<td>3.300</td>
<td>3.366</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation 5.0 V Version</td>
<td>ΔV_{OUT} vs. Vin</td>
<td>I_{OUT} = 5.0 mA 6.0 V ≤ Vin ≤ 28 V</td>
<td>-25</td>
<td>5.0</td>
<td>+25</td>
<td>mV</td>
</tr>
<tr>
<td>Line Regulation 3.3 V Version</td>
<td>ΔV_{OUT} vs. Vin</td>
<td>I_{OUT} = 5.0 mA 4.5 V ≤ Vin ≤ 28 V</td>
<td>-25</td>
<td>5.0</td>
<td>+25</td>
<td>mV</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>ΔV_{OUT} vs. I_{OUT}</td>
<td>1.0 mA ≤ I_{OUT} ≤ 150 mA (Note 4)</td>
<td>-35</td>
<td>5.0</td>
<td>+35</td>
<td>mV</td>
</tr>
<tr>
<td>Dropout Voltage 5.0 V Version</td>
<td>V_{IN}−V_{OUT}</td>
<td>I_{Q} = 100 mA (Notes 4 &amp; 5) I_{Q} = 150 mA (Notes 4 &amp; 5)</td>
<td>–</td>
<td>265</td>
<td>500</td>
<td>mV</td>
</tr>
<tr>
<td>Dropout Voltage 3.3 V Version</td>
<td>V_{IN}−V_{OUT}</td>
<td>I_{Q} = 100 mA (Notes 4 &amp; 7) I_{Q} = 150 mA (Notes 4 &amp; 7)</td>
<td>–</td>
<td>–</td>
<td>1.266</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>I_{Q}</td>
<td>I_{OUT} = 100 μA T_{J} = 25°C T_{J} = -40°C to +85°C</td>
<td>–</td>
<td>21</td>
<td>29</td>
<td>μA</td>
</tr>
<tr>
<td>Active Ground Current</td>
<td>I_{G(ON)}</td>
<td>I_{OUT} = 50 mA (Note 4) I_{OUT} = 150 mA (Note 4)</td>
<td>–</td>
<td>1.3</td>
<td>3</td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>PSRR</td>
<td>V_{RIPPLE} = 0.5 V p-p F = 100 Hz</td>
<td>–</td>
<td>67</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Output Capacitor for Stability 5.0 V Version</td>
<td>C_{OUT} ESR</td>
<td>I_{OUT} = 0.1 mA to 150 mA (Note 4)</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>μF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>9.0</td>
<td>Ω</td>
</tr>
<tr>
<td>Output Capacitor for Stability 3.3 V Version</td>
<td>C_{OUT} ESR</td>
<td>I_{OUT} = 0.1 mA to 150 mA (Note 4)</td>
<td>22</td>
<td>–</td>
<td>–</td>
<td>μF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>18</td>
<td>Ω</td>
</tr>
</tbody>
</table>

PROTECTION

| Current Limit | I_{OUT(LIM)} | V_{OUT} = 4.5 V (5.0 V Version) (Note 4) V_{OUT} = 3.0 V (3.3 V Version) (Note 4) | 150 | – | 500 | mA |
| Short Circuit Current Limit | I_{OUT(SC)} | V_{OUT} = 0 V (Note 4) | 150 | – | 500 | mA |
| Thermal Shutdown Threshold | T_{TSD} | V_{OUT} = 0 V (Note 4) | 150 | – | 200 | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Use pulse loading to limit power dissipation.
5. Dropout voltage = (V_{IN} − V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with Vin = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.
7. V_{DO} = V_{IN} − V_{OUT}. For output voltage set to < 4.5 V, V_{DO} will be constrained by the minimum input voltage.
NCV8664

Figure 2. Measurement Circuit

Figure 3. Applications Circuit
Typical Curves

Figure 4. ESR Characterization, 5.0 V Version

Figure 5. Output Voltage vs. Input Voltage, 5.0 V Version

Figure 6. Current Consumption vs. Output Load, 5.0 V Version

Figure 7. Current Consumption vs. Output Load (Low Load), 5.0 V Version

Figure 8. Quiescent Current vs. Temperature, 5.0 V Version

Figure 9. Quiescent Current vs. Temperature, 5.0 V Version
Typical Curves

Figure 10. Dropout Voltage vs. Output Load, 5.0 V Version

Figure 11. Current Consumption vs. Input Voltage, 5.0 V Version

Figure 12. Output Current vs. Input Voltage, 5.0 V Version

Figure 13. Output Voltage vs. Temperature, 5.0 V Version

Figure 14. Current Limit vs. Temperature, 5.0 V Version
Typical Curves

Figure 15. ESR Stability, 3.3 V Version

Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version

Figure 17. Current Consumption vs. Output Load, 3.3 V Version

Figure 18. Current Consumption vs. Output Load (Low Load), 3.3 V Version

Figure 19. Quiescent Current vs. Temperature, 3.3 V Version

Figure 20. Quiescent Current vs. Temperature, 3.3 V Version
Typical Curves

**Figure 21. Dropout Voltage, 3.3 V Version**

**Figure 22. Current Consumption vs. Input Voltage, 3.3 V Version**

**Figure 23. Output Voltage vs. Temperature, 3.3 V Version**

**Figure 24. Short Circuit Current Limit vs. Temperature, 3.3 V Version**
Circuit Description
The NCV8664 is a precision trimmed 3.3 V and 5.0 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 22 μA. The device has current capability of 150 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator
The error amplifier compares the reference voltage to a sample of the output voltage (Vout) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature–stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8664 is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

Regulator Stability Considerations
The input capacitor Cin in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with Cin. The output or compensation capacitor, Cout helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information. The value for the output capacitor Cout shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values Cout ≥ 10 μF and ESR ≤ 9 Ω for 5.0 V version, and Cout ≥ 22 μF and ESR ≤ 18 Ω for 3.3 V version, within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator
The maximum power dissipation for a single output regulator (Figure 3) is:

\[
P_D(\text{max}) = (V_{\text{IN(max)}} - V_{\text{OUT(min)}}) \cdot I_Q(\text{max}) + V_I(\text{max}) \cdot I_q
\]  

(eq. 1)

Where:
- \(V_{\text{IN(max)}}\) is the maximum input voltage,
- \(V_{\text{OUT(min)}}\) is the minimum output voltage,
- \(I_Q(\text{max})\) is the maximum output current for the application,
- \(I_q\) is the quiescent current the regulator consumes at \(I_Q(\text{max})\).

Once the value of \(P_D(\text{Max})\) is known, the maximum permissible value of \(R_{\text{θJA}}\) can be calculated:

\[
R_{\text{θJA}} = \frac{150°C - T_A}{P_D}
\]

(eq. 2)

The value of \(R_{\text{θJA}}\) can then be compared with those in the package section of the data sheet. Those packages with \(R_{\text{θJA}}\)'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks
For proper heat sinking of the SOIC–8 Lead device, connect pins 5 – 8 to the heat sink.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of \(R_{\text{θJA}}\):

\[
R_{\text{θJA}} = R_{\text{θJC}} + R_{\text{θCS}} + R_{\text{θSA}}
\]

(eq. 3)

Where:
- \(R_{\text{θJC}}\) is the junction-to-case thermal resistance,
- \(R_{\text{θCS}}\) is the case-to-heat sink thermal resistance, and
- \(R_{\text{θSA}}\) is the heat sink-to-ambient thermal resistance.

\(R_{\text{θJA}}\) appears in the package section of the data sheet. Like \(R_{\text{θJA}}\), it too is a function of package type. \(R_{\text{θCS}}\) and \(R_{\text{θSA}}\) are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.
EMC–Characteristics: Conducted Susceptibility
All EMC–Characteristics are based on limited samples and not part of production testing, according to 47A/658/CD IEC62132–4 (Direct Power Injection)

Direct Power Injection: 33 dBm forward power CW
Acceptance Criteria: Amplitude Dev. max 2% of Output Voltage

Test Conditions
Supply Voltage $V_{IN} = 12$ V
Temperature $T_A = 23^\circ$C ±5°C
Load $R_L = 35$ Ω

![Figure 25. Test Circuit](image)

![Figure 26. Typical $V_{IN}$–pin Susceptibility](image)

![Figure 27. Typical $V_{OUT}$–pin Susceptibility](image)
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device*</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping†</th>
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<tbody>
<tr>
<td>NCV8664D50R2G</td>
<td>V6645</td>
<td>SOIC–8 Fused</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV8664D50G</td>
<td>V6645</td>
<td>SOIC–8 Fused</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>NCV8664DT50RKG</td>
<td>V66450G</td>
<td>DPAK (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV8664DT33RKG</td>
<td>V66433G</td>
<td>DPAK (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
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<tr>
<td>NCV8664ST50T3G</td>
<td>V6645</td>
<td>SOT–223 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
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<tr>
<td>NCV8664ST33T3G</td>
<td>V6643</td>
<td>SOT–223 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

NOTES:
2. CONTROLLING DIMENSION MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. AI IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>DIM</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>1.50</td>
<td>1.63</td>
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<td>0.02</td>
<td>0.06</td>
<td>0.10</td>
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<tr>
<td>b</td>
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<td>0.89</td>
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<tr>
<td>b1</td>
<td>2.90</td>
<td>3.06</td>
<td>3.20</td>
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<td>c</td>
<td>0.24</td>
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<tr>
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<td>6.50</td>
<td>6.70</td>
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<td>E</td>
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<td>3.70</td>
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</tr>
<tr>
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<tr>
<td>L</td>
<td>0.20</td>
<td>---</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>1.50</td>
<td>1.75</td>
<td>2.00</td>
<td></td>
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<tr>
<td>He</td>
<td>6.70</td>
<td>7.00</td>
<td>7.30</td>
<td></td>
</tr>
<tr>
<td>θ</td>
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<td>10°</td>
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</tbody>
</table>

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SOT–223 (TO–261)
CASE 318E–04
ISSUE R
DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. SOURCE

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*

AYW
XXXXX

A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
* = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, “G” or microdot “*”, may or may not be present. Some products may
not follow the Generic Marking.

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**DPAK (SINGLE GAUGE)**
CASE 369C
ISSUE F

**DATE 21 JUL 2015**

**NOTES:**
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS L3 and L4.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

**SCALE 3:1**

**SOLDERING FOOTPRINT**

*This information is generic. Please refer to device data sheet for actual part marking.*

**MARKING DIAGRAM**

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**DOCUMENT NUMBER:** 98AON10527D
**STATUS:** ON SEMICONDUCTOR STANDARD
**NEW STANDARD:** REF TO JEDEC TO−252
**DESCRIPTION:** DPAK SINGLE GAUGE SURFACE MOUNT

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<td>O</td>
<td>RELEASED FOR PRODUCTION. REQ. BY L. GAN</td>
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<td>A</td>
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<td>C</td>
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<td>D</td>
<td>RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.</td>
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<td>E</td>
<td>ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.</td>
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<td>ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.</td>
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24 SEP 2001

06 AUG 2008

16 JAN 2009

09 JUN 2009

29 JUN 2010

06 FEB 2014

21 JUL 2015
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “•”, may or may not be present. Some products may not follow the Generic Marking.

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